

MC100EP58

2:1 Multiplexer

The MC100EP58 is a 2:1 multiplexer. The device is pin and functionally equivalent to the EL58 and LVEL58 devices.

- 275ps Typical Propagation Delay
- High Bandwidth to 3 Ghz Typical
- PECL mode: 3.0V to 5.5V V_{CC} with $V_{EE} = 0V$
- ECL mode: 0V V_{CC} with $V_{EE} = -3.0V$ to $-5.5V$
- 75k Ω Internal Input Pulldown Resistors
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack.
For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8",
Oxygen Index 28 to 34
- Transistor Count = 41 devices

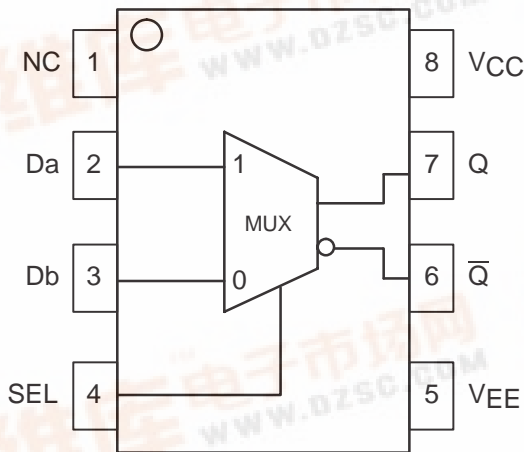


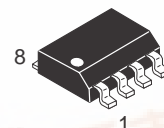
Figure 1. 8-Lead Pinout (Top View) and Logic Diagram



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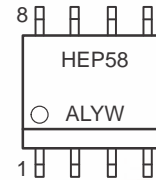
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SO-8
D SUFFIX
CASE 751

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION

PIN	FUNCTION
Da, Db	ECL Data Inputs
SEL	ECL Select Inputs
Q, \bar{Q}	ECL Data Outputs

TRUTH TABLE

SEL	Data
H	a
L	b

ORDERING INFORMATION

Device	Package	Shipping
MC100EP58D	SOIC	98 Units/Rail
MC100EP58DR2	SOIC	2500 Tape & Reel



MC10EP58

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply ($V_{CC} = 0V$)	-6.0 to 0	VDC
V_{CC}	Power Supply ($V_{EE} = 0V$)	6.0 to 0	VDC
V_I	Input Voltage ($V_{CC} = 0V$, V_I not more negative than V_{EE})	-6.0 to 0	VDC
V_I	Input Voltage ($V_{EE} = 0V$, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
T_A	Operating Temperature Range	-40 to +85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	41 to 44 \pm 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

DC CHARACTERISTICS, ECL/LVECL ($V_{CC} = 0V$; $V_{EE} = -5.5V$ to $-3.0V$) (Note 3.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current (Note 1.)	20	28	37	20	30	39	22	31	40	mA
V_{OH}	Output HIGH Voltage (Note 2.)	-1135	-1060	-885	-1070	-945	-820	-1010	-885	-760	mV
V_{OL}	Output LOW Voltage (Note 2.)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
V_{IH}	Input HIGH Voltage Single Ended	-1210		-885	-1145		-820	-1085		-760	mV
V_{IL}	Input LOW Voltage Single Ended	-1935		-1610	-1870		-1545	-1810		-1485	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current \overline{D}	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. $V_{CC} = 0V$, $V_{EE} = V_{EEmin}$ to V_{EEmax} , all other pins floating.
2. All loading with 50 ohms to V_{CC} -2.0 volts.
3. Input and output parameters vary 1:1 with V_{CC} .

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DC CHARACTERISTICS, LVPECL ($V_{CC} = 3.3V \pm 0.3V$, $V_{EE} = 0V$) (Note 6.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 4.)	20	28	37	20	30	39	22	31	40	mA
VOH	Output HIGH Voltage (Note 5.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
VOL	Output LOW Voltage (Note 5.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
VIH	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
VIL	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current D D̄	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

4. $V_{CC} = 3.3V$, $V_{EE} = 0V$, all other pins floating.

5. All loading with 50 ohms to V_{CC} -2.0 volts.

6. Input and output parameters vary 1:1 with V_{CC} .

DC CHARACTERISTICS, PECL ($V_{CC} = 5.0V \pm 0.5V$, $V_{EE} = 0V$) (Note 9.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 7.)	20	28	37	20	30	39	22	31	40	mA
VOH	Output HIGH Voltage (Note 8.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
VOL	Output LOW Voltage (Note 8.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
VIH	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
VIL	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current D D̄	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

7. $V_{CC} = 5.0V$, $V_{EE} = 0V$, all other pins floating.

8. All loading with 50 ohms to V_{CC} -2.0 volts.

9. Input and output parameters vary 1:1 with V_{CC} .

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AC CHARACTERISTICS ($V_{CC} = 0V$; $V_{EE} = -3.0V$ to $-5.5V$) or ($V_{CC} = 3.0V$ to $5.5V$; $V_{EE} = 0V$)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency (Note 10.)		3.0			3.0			3.0		GHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential D→Q, \overline{Q} SEL→Q, \overline{Q}	170 170	250 250	350 350	190 190	275 275	375 375	210 210	300 300	400 400	ps
t_{SKEW}	Duty Cycle Skew (Note 11.)		5.0			5.0	20		5.0	20	ps
t_{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times (20% – 80%)	60	120	190	60	130	200	70	150	220	ps

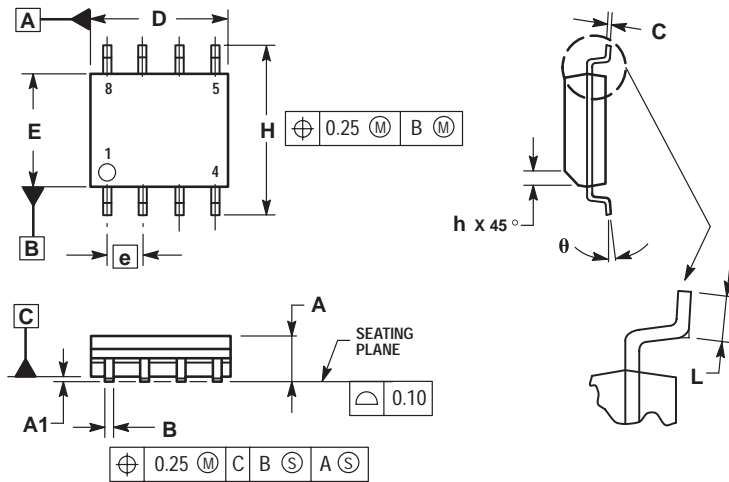
10. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.

11. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

MC10EP58

PACKAGE DIMENSIONS

SO-8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-06
ISSUE T



NOTES:


1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

Notes

Notes

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