MC100EPT622

3.3V LVTTL/LVCMOS to LVPECL Translator

The MC100EPT622 is a 10-Bit LVTTL/LVCMOS to LVPECL translator. Because LVPECL (Positive ECL) levels are used only +3.3 V and ground are required. The device has an OR-ed enable input which can accept either LVPECL (ENPECL) or TTL/LVCMOS inputs (ENTTL). If the inputs are left open, they will default to the enable state. The device design has been optimized for low channel-to-channel skew

- 450 ps Typical Propagation Delay
- Maximum Frequency > 1.5 GHz Typical
- PECL Mode
- Operating Range: V_{CC} = 3.0 V to 3.8 V with V_{EE} = 0 V
- PNP LVTTL Inputs for Minimal Loading
- Q Output Will Default HIGH with Inputs Open
- The 100 Series Contains Temperature Compensation.

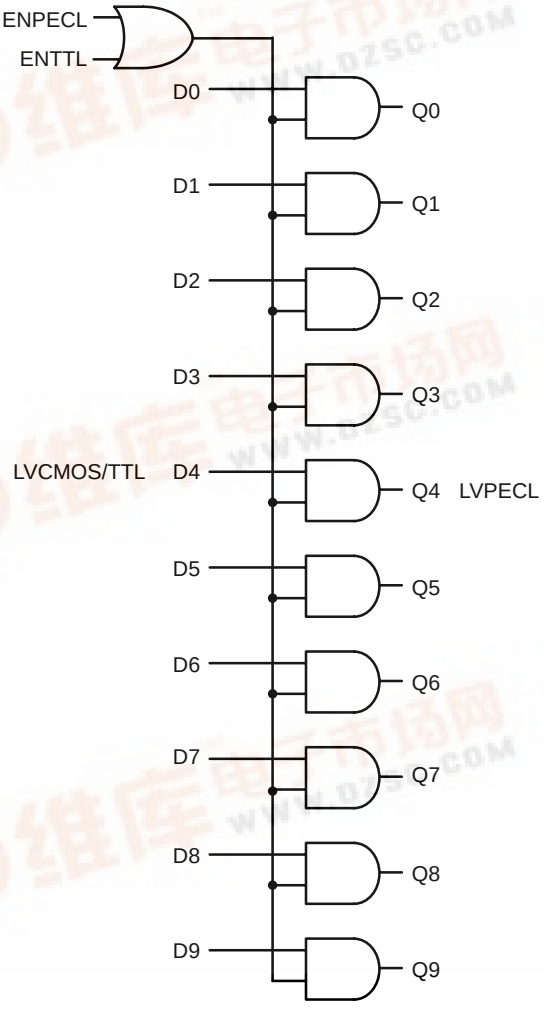

Figure 1. Logic Symbol

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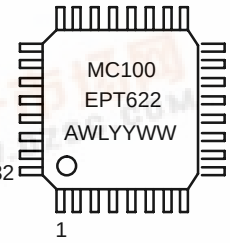
LQFP-32
FA SUFFIX
CASE 873A

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

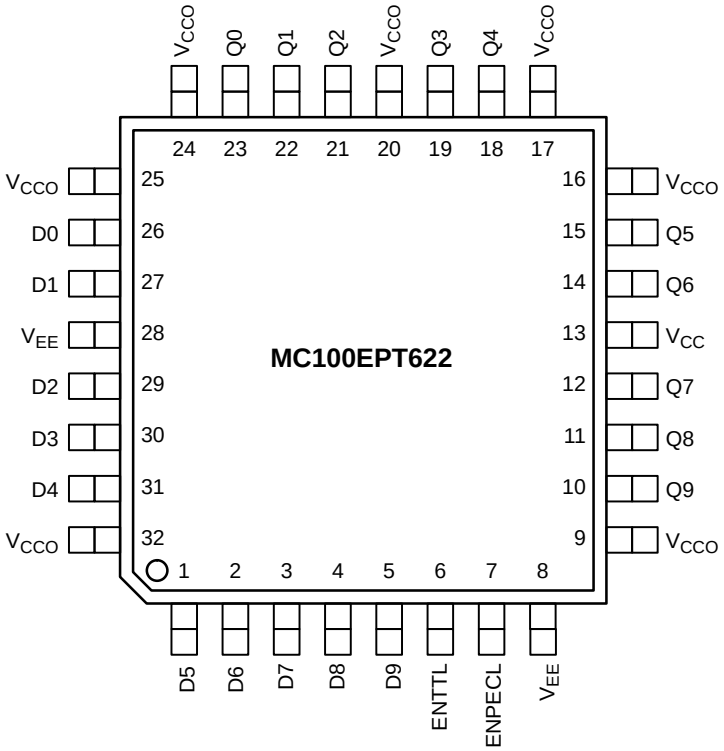
ORDERING INFORMATION

Device	Package	Shipping
MC100EPT622FA	LQFP32	250 Unit Trays
MC100EPT622FAR2	LQFP32	2000 Tape & Reel

TRUTH TABLE

ENPECL	ENTTL	D	Q
H	X	H	H
H	X	L	L
X	H	H	H
X	H	L	L
L	L	X	L

Publication Order Number:



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 32-Lead LQFP Pinout (Top View)

PIN DESCRIPTION

PIN	FUNCTION
D0:9	Data Input (TTL)
Q0:9	Data Output (PECL)
ENTTL	Enable Control (TTL)
ENPECL	Enable Control (PECL)
V_{CC}	Positive Supply
V_{EE}	Ground

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		N/A
Internal Input Pullup Resistor		N/A
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 150 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack		Level 2
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		596 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Power Supply	V_{EE} = 0 V		5	V
V_I	Input Voltage	V_{EE} = 0 V	$V_I \leq V_{CC}$	5 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	32 LQFP 32 LQFP	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	std bd	32 LQFP	12 to 17	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

TTL INPUT DC CHARACTERISTICS V_{CC} = 3.3 V, GND= 0.0 V, T_A = -40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current	V_{IN}= 2.7 V			25	μA
I_{IHH}	Input HIGH Current MAX	V_{IN}= V_{CC}			100	μA
I_{IL}	Input LOW Current	V_{IN}= 0.5 V			-0.6	mA
V_{IK}	Input Clamp Voltage	I_{IN}= -18 mA	-1.2	-0.9		V
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V

PECL INPUT DC CHARACTERISTICS V_{CC} = 3.3 V, GND= 0.0 V, T_A = -40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current	V_{IN}= 2420 mV			150	μA
I_{IL}	Input LOW Current	V_{IN}= 1490 mV			200	μA
V_{IH}	Input HIGH Voltage		2075		2420	mV
V_{IL}	Input LOW Voltage		1490		1675	mV

PECL OUTPUT DC CHARACTERISTICS V_{CC} = 3.3 V, GND = 0.0 V (Note 2)

		-40 °C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current	85	115	145	90	120	155	95	130	155	mA
V_{OH}	Input High Voltage (Note 3)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Input Low Current (Note 3)	1355	1520	1700	1355	1520	1700	1355	1520	1700	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

2. Input and output parameters vary 1:1 with V_{CC}.
3. All loading with 50 Ω to V_{CC}- 2.0 V.

AC CHARACTERISTICS V_{CC} = 3.0 V to 3.8 V (Note 4)

		-40 °C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Frequency (See Figure 2)	1.0	1.5		1.0	1.5		1.0	1.5		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output (Figure 3, Note 5)										ps
	D to Q	100	450	800	100	500	875	100	500	800	
	ENPECL to Q	150	500	875	150	500	875	200	550	925	
	ENTTL to Q	300	450	800	300	500	800	300	500	800	
t_{JITTER}	Random Clock Jitter (RMS) (See Figure 2)		0.7	3.0		0.7	3.0		0.7	3.0	ps
t_r / t_f	Output Rise/Fall Times (20% - 80%)	100	200	450	100	200	250	100	200	300	ps
T_{SKEW}	Duty Cycle Skew (Note 6)										ps
	D to Q Channel 0-7		120	375		120	375		120	375	
	D to Q Channel 8-9		200	775		200	775		200	775	
	ENPECL to Q		120	400		120	400		120	400	
	ENTTL to Q		100	275		100	275		100	275	

4. Measured using a 2.4 V source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}-2.0 V.
5. 1.5 V to 50% point of the output.
6. Duty cycle skew $|t_{PLH} - t_{PHL}|$ on the specific path.

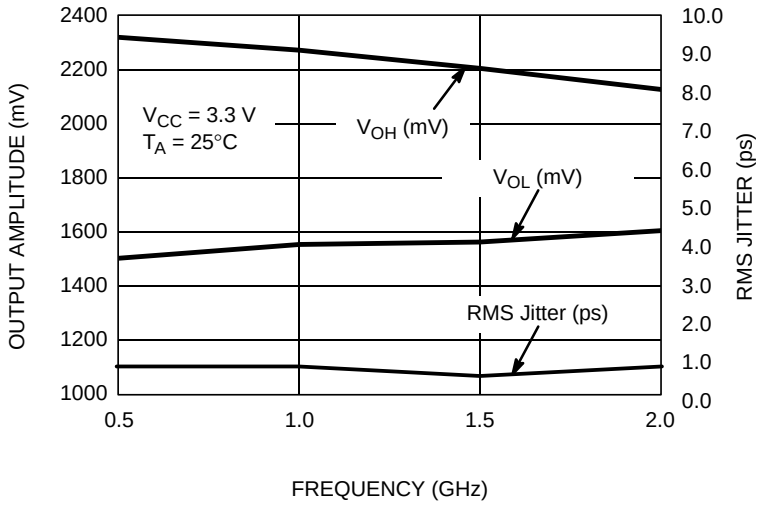


Figure 2. Average Output Amplitude/Jitter (3.3 V, 25°C)

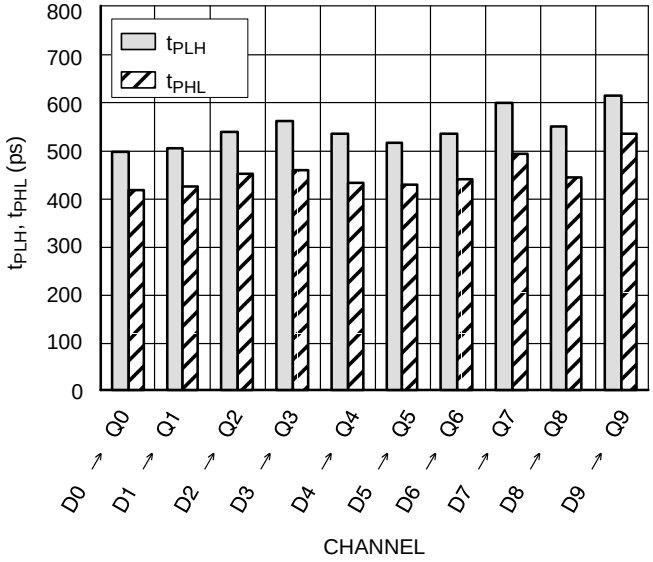
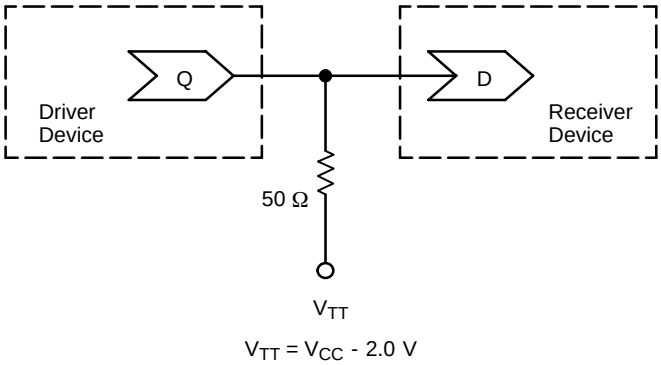


Figure 3. Average Propagation Delay (3.3 V, 25°C)



$V_{TT} = V_{CC}$ - 2.0 V

Figure 4. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 - Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 - ECLinPS Circuit Performance at Non-Standard V_{IH} Levels

AN1405 - ECL Clock Distribution Techniques

AN1406 - Designing with PECL (ECL at +5.0 V)

AN1504 - Metastability and the ECLinPS Family

AN1568 - Interfacing Between LVDS and ECL

AN1650 - Using Wire-OR Ties in ECLinPS Designs

AN1672 - The ECL Translator Guide

AND8001 - Odd Number Counters Design

AND8002 - Marking and Date Codes

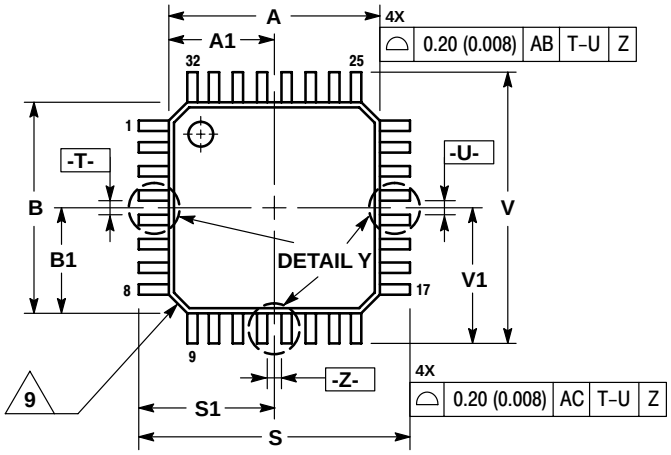
AND8009 - ECLinPS Plus™ Spice I/O Model Kit

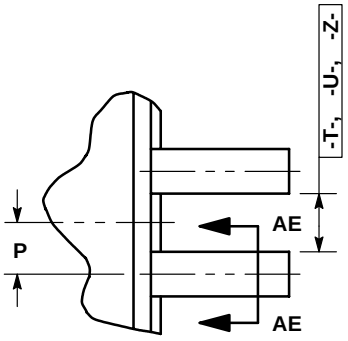
AND8020 - Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at http://onsemi.com.

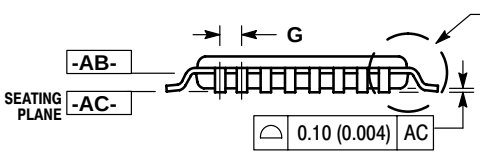
PACKAGE DIMENSIONS

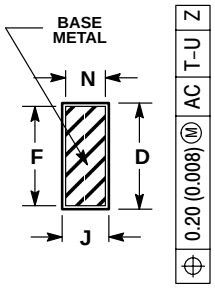
LQFP
FA SUFFIX
32-LEAD PLASTIC PACKAGE
CASE 873A-02
ISSUE A



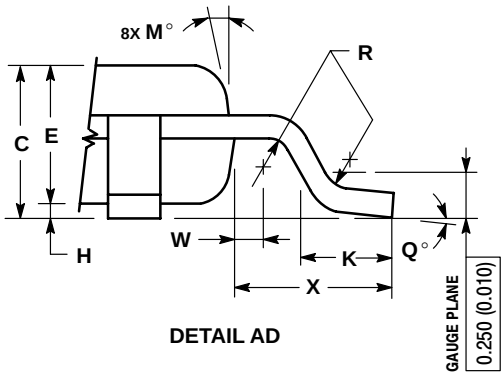


DETAIL Y





SECTION AE-AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

Notes

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