

ePVP6810

VFD Controller

Product Specification

VERSION
1.23

ELAN MICROELECTRONICS CORP.

Nov 2004



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Specification Revision History		
Version	Revision Description	Date
1.0	Initial version	2004/5/26
1.1	ADD Relevant Pins assignment Revices DC Electrical Characteristic Revices cpu Feature Describe Application notes	2004/06/23
1.2	additional remark Application notes	2004/9/16
1.21	Revised CONT register describe Updata Pckage Information	2004/9/24
1.22	IC Name change	2004/11/4
1.23	Revised Feature register describe additional remark Application notes Revised Operation Voltage VS PLL Operation frequency	2004/11/28



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Read Me First!

Before using the chip, spare a few minutes to take a look at the following important notes.

1. Some bits in the registers are undefined. The values in these bits are unknown and should not be used. These bits are designated with a dash “-” symbol as its bit name in this specification.
2. The following table shows the definitions of the various register designations used to identify bit types, bit name, and bit number. Some definitions will appear quite frequently in the specification.

Bit number	7	6	5	4	3	2	1	0
Bit name	RAB7	RAB6	BAB5	RAB4	-	RAB2	RAB1	RAB0
Bit type	R/W-0	R/W-0	R-1	R/W-1	(undefined) not allowed to use	R	R-0	R/W
Register name and its page		read/write (default value=0)	read only (default value=1)	read/write (default value=1)		read only (w/o default value)	read only (default value=0)	read/write (w/o default value)

RA
 PAGE0



1 General Description

The ePVP6810 is an 8-bit RISC type vacuum fluorescent display (VFD) controller equipped with low power consumption and high speed CMOS technology. This integrated single chip features on-chip watchdog timer (WDT), one time programming ROM (OTP), data RAM, programmable real time clock/counter, internal interrupt, power down mode, 10-bit A/D converter, IR detector, and high voltage output for VFD application.

2. Feature

2.1 CPU

- **Clock source** : Crystal Oscillator
- Crystal Oscillator (32.768KHz): with a external crystal
- 4k x 13 on chip Program ROM.
- 128 x 8 on chip data RAM
- 144 x 8 general purpose registers
- 16 level stack for subroutine nesting
- **5 channel 8-bit counters**: real time clock/counter (TCC) ,COUNTER1, COUNTER3, COUNTER4, COUNTER5
- **1 channel 16-bit counter**: COUNTER2
- On-chip watchdog timer (WDT)
- 99.9% single instruction cycle commands
- Four operation modes

Mode	CPU Status	Main Clock	32.768kHz Clock Status	Description
Sleep mode	Turn off	Turn off	Turn off	RA(6) = 0 RA(7) = 0 + "SLEP" instruction
Idle mode	Turn off	Turn off	Turn on	RA(6) = 0 RA(7) = 1 + "SLEP" instruction.
Green mode	Turn on	Turn off	Turn on	RA(6) = 0
Normal mode	Turn on	Turn on	Turn on	RA(6) = 1

* Main clock can be programmed from 447.829k to 17.91MH by internal PLL

* **8 main clocks**: 447.829K, 895.658K, 1.791M , 3.582M , 7.165M , 10.747M , 14.331M and 17.91MHz

- 12 interrupt source, 5 external (IR , INT1~INT4) , 8 internal (ADC, TCC, COUNTER1~5)

2.2 GPIO

- GPIO 9 Port(8 bit): general purpose input/output; LED output ; interrupt function
- GPIO B Port(7 bit): general purpose input/output for power down/MPEG power/Reset control
- GPIO C Port(4 bit): general purpose input/output for switch and key scanning (6x4 matrix)

2.3 ADC



- 6 channel 10-bit successive approximation A/D converter
- Internal (VDD) or external voltage reference

2.4 VFD

- Multiple display modes (6-segment & 12-digit to 9-segment & 9-digit)
- External resistor not necessary for driver outputs.(P-ch open-drain + pull-down resistor output)

2.5 POR

2.0V voltage detector for Power-on reset

2.6 PACKAGE

44-pin LQFP

3 Application

VFD controller

4 Pin Configuration

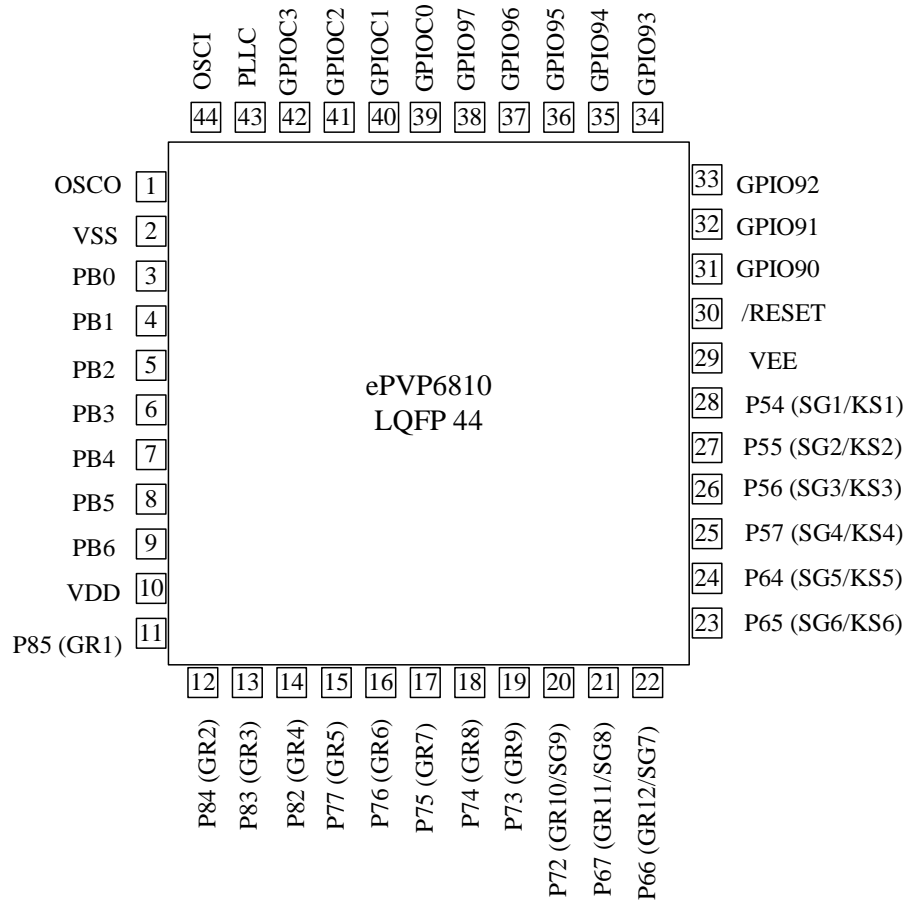


Fig. 1 Pin Assignment



5 Functional Block Diagram

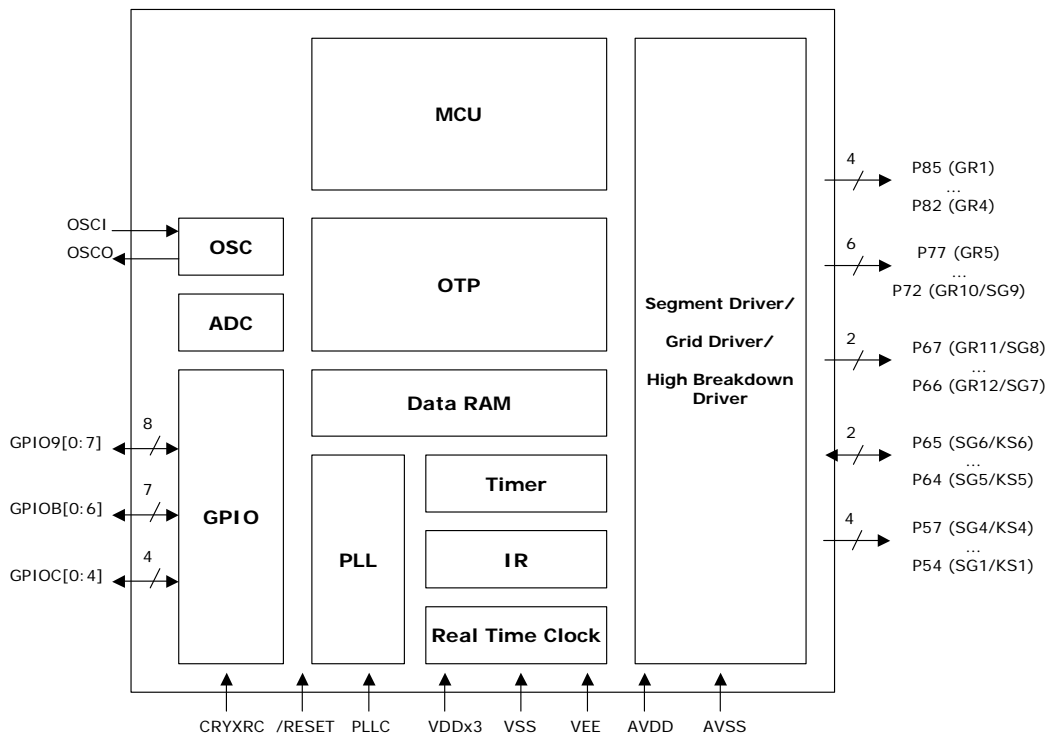


Fig. 2a Block Diagram

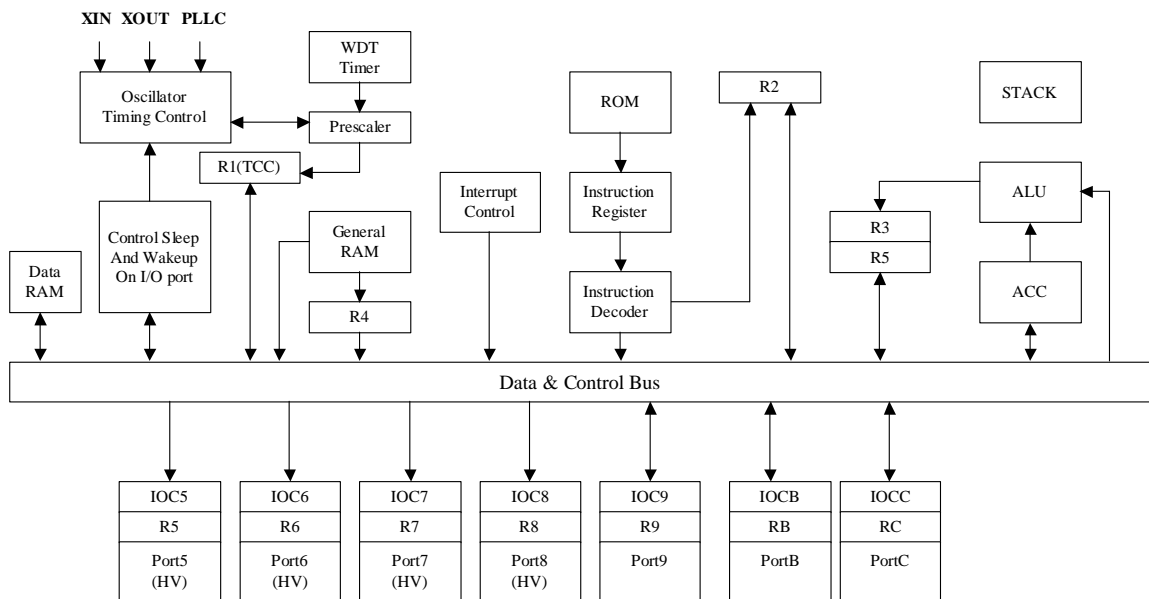


Fig. 2b Block Diagram



5.1 Ports Mapping for HV and GPIO

5.1.1 HV Port Mapping

Port	HV	Port	HV	Port	HV	Port	HV
-	-	P60	-	P70	-	P80	-
-	-	P61	-	P71	-	P81	-
-	-	P62	-	P72	GR10/SEG9	P82	GR4
-	-	P63	-	P73	GR9	P83	GR3
P54	SG1/KS1	P64	SEG5/KS5	P74	GR8	P84	GR2
P55	SG2/KS2	P65	SEG6/KS6	P75	GR7	P85	GR1
P56	SG3/KS3	P66	GR12/SEG7	P76	GR6	P86	-
P57	SG4/KS4	P67	GR11/SEG8	P77	GR5	P87	-

5.1.2 GPIO Port Mapping

Port	GPIO	Port	GPIO	Port	GPIO
P90	GPIO90/LED0/IR	PB0	GPIOB0/VREF	PC0	GPIOC0/Key1
P91	GPIO91/LED1/INT1	PB1	GPIOB1/AD1	PC1	GPIOC1/Key2
P92	GPIO92/LED2/INT2	PB2	GPIOB2/AD2	PC2	GPIOC2/Key3
P93	GPIO93/LED3/INT3	PB3	GPIOB3/AD3	PC3	GPIOC3/Key4
P94	GPIO94/LED4/INT4	PB4	GPIOB4/AD4		
P95	GPIO95/LED5	PB5	GPIOB5/AD5		
P96	GPIO96/LED6	PB6	GPIOB6/AD6		
P97	GPIO97/LED7	-	-		

5.2 Relevant Pins for programming mode

OTP PIN NAME	MASK ROM PIN NAME
VDD	AVDD
VPP	/RESTER
DINCK	PC3
ACLK	PC2
PGMB	P92
OEB	P91
DATA	P90
GND	GND



6 Pin Descriptions

Pin No.	Pin Name	I/O	#	Description	Note
10	VDD	-	1	Logic power supply	
40 – 42	GPIOC0 – GPIOC3	I/O	4	General Purpose I/O pins: 1. Key data input to these pins is latched at the end of display cycle. 2. These pins constitute 4-bit general-purpose input/output port. 3. Programmable Internal Pull-High 4. Wake-up Function	Schmitt Pull-up
11-14 (B Cell)	GR1 – GR4	O	4	1. High voltage grid output	
15-19 (B Cell)	GR5 – GR9	O	5	1. High voltage grid output 2. High voltage segment output	
20-22 (B Cell)	GR10/SG19 – GR12/SG7	O	3	1. High voltage grid output 2. High voltage segment output	
23-24 A Cell	SG6/KS6 – SG5/KS5	O	2	1. High voltage grid output 2. High voltage segment output 3. Matrix key scan output	
25 ~28 C Cell	SG4/KS4 – SG1/KS1	I/O	4	1. High voltage segment output 2. Matrix key scan output 3. General Purpose Input pins: p54~p57	~
31 38	GPIO90/LED0 – GPIO97/LED7	I/O	8	1. General Purpose I/O pins 2. LED output pin (20mA) 3. IR Detector 4. Interrupt Function 5. Programmable Internal Pull-High	Schmitt Pull-up
43	PLLC	I	1	Phase Lock Loop Capacitor (connect a Capacitor 0.01 to 0.047u to the Ground).	
44	OSCI	I	1	Crystal Oscillator input pin (32, 768Hz)	
1	OSCO	O	1	Crystal Oscillator output pin (32, 768Hz)	
2	VSS	-	1	Connect this pin to GND of the system	
30	/RESET	I	1	Low active RESET signal input	Schmitt
29	VEE	-	1	Pull-down level (VDD-(-40V)max)	



7 Function Descriptions

7.1 Operation Registers Configuration

Addr	R PAGE Registers		
	R PAGE0	R PAGE1	R PAGE2
00	Indirect addressing		
01	TCC		
02	PC		
03	Page, Status		
04	RAM bank, RSR		
05	Port5 Output data	Program ROM page	
06	Port6 Output data		
07	Port7 Output data	ADC control	Counter1 data
08	Port8 Output data	Data RAM address	Counter2 LB data
09	Port9 I/O data	Data RAM data buffer	Counter2 HB data
0A	PLL, Main clock,WDTE	ADC output data buffer	Counter3 data
0B	PortB I/O data	Port9 pull high	Counter4 data
0C	PortC I/O data	PortC pull high	Counter5 data
0D	Interrupt flag		
0E	Interrupt flag, Wake-up control		
0F	Interrupt flag		
10 : 1F	16 bytes Common registers		
20 : 3F	Bank0 ~ Bank3 Common registers (32x8 for each bank)		

Addr	IOC PAGE Registers	
	IOC PAGE0	IOC PAGE1
00		
01		
02		
03		
04		
05		Port5 switch
06		
07		
08		Clock source (CN2,CN1) Prescaler (CN2,CN1)
09	Port9 I/O control	Clock source (CN4,CN3) Prescaler (CN4,CN3)
0A		Clock source (CN5) Prescaler (CN5)
0B	PortB I/O control	PortB switch
0C	PortC I/O control	
0D	Interrupt mask	
0E	Interrupt mask	
0F	Interrupt mask	



"TBL" allows a relative address to be added to the current PC, and the contents of the ninth and tenth bits do not change. The most significant bit (A10~A13) will be loaded with the contents of bit PS0~PS3 in the status register (R5 PAGE 1) upon execution of a "JMP," "CALL," "ADD R2, A." or "MOV R2, A" instruction.

If an interrupt is triggered, PROGRAM ROM will jump to address 0x08 at Page0. The CPU will automatically store ACC, R3 status, and R5 PAGE 1, and they will be restored after execution of instruction RETI.

7.2.4 R3 (Status, Page Selection)

(Status Flag, Page Selection Bits)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RPAGE1	RPAGE0	IOCPAGE	T	P	Z	DC	C
R/W-0	R/W-0	R/W-0	R	R	R/W	R/W	R/W

Bit 0 (C) : Carry flag

The carry flag is affected by following operation :

- Addition : CF as a carry out indicator, when the addition operation has a carry-out, CF will be "1", in another word, if the operation has no carry-out, CF will be "0".
- Subtraction : CF as a borrow-in indicator, when the subtraction operation must has a borrow-in, the CF will be "0", in another word, if no borrow-in, CF will be "1".
- Comparison : CF is as a borrow-in indicator for Comparison operation as the same as subtraction operation.
- Rotation : CF shifts into the empty bit of accumulator for the rotation and holds the shift out data after rotation.

Bit 1 (DC) : Auxiliary carry flag

Bit 2 (Z) : Zero flag

ZF is affected by the result of ALU, if the ALU operation generate a "0" result, the ZF will be "1", otherwise, the ZF will be "0".

Bit 3 (P) : Power down bit

Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 4 (T) : Time-out bit

Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

Event	T	P	Remarks
WDT wake up from sleep mode	0	0	
WDT time out (not sleep mode)	0	1	
/RESET wake up from sleep	1	0	
Power up	1	1	
Low pulse on /RESET	x	X	x : don't care



Bit 5 (IOCPAGE) : Change IOC5 ~ IOCE to another page
0/1 → IOC page0 / IOC page1

Bit 6 (RPAGE0 ~ RPAGE1) : Change R5 ~ RC to another page (see Section 7.1 *Operation Registers Configuration* for details.)

(RPAGE1, RPAGE0)	R page # selected
(0,0)	R page 0
(0,1)	R page 1
(1,x)	R page 2



7.2.5 R4 (RAM Selection For Common Registers R20 ~ R3F)

(RAM Selection Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RB1	RB0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W-0	R/W-0	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 5 (RSR0 ~ RSR5) : Indirect address for common Registers R20 ~ R3F.

RSR bits are used to select up to 32 registers (R20 to R3F) in the indirect address mode.

Bit 6 ~ Bit 7 (RB0 ~ RB1) : Bank selection bits for common Registers R20 ~ R3F.

These selection bits are used to determine which bank is activated among the 4 banks for 32 register (R20 to R3F). Refer to Section 7.1 *Operation Registers Configuration* for details.

7.2.6 R5 (PORT5 Output Data, Program Page Selection)

a) **PAGE 0 (PORT5 Output Data Register for HV, General Purpose Input pins: p54~p57)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P57	P56	P55	P54	-	-	-	-
W-0	W-0	W-0	W-0	-	-	-	-

b) **PAGE 1 (Program ROM Page Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD9	AD8	-	-	-	-	PS1	PS0
R	R	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 3 (PS0 ~ PS3) : Program page selection bits

PS1	PS0	Program Memory Page (Address)
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

PAGE instruction is used to select the program page to be accessed. The selected program page is maintained by Elan compiler. PAGE instruction will change your program by inserting the instruction within program.



7.2.7 R6 (PORT6 Output Data)

a) PAGE 0 (PORT6 Output Data Register for HV)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	-	-	-	-
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

7.2.8 R7 (PORT7 Output Data, ADC , Counter1 Data)

a) PAGE 0 (PORT7 Output Data Register for HV)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P77	P76	P75	P74	P73	P72	-	-
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

b) PAGE 1 (ADC Control Bit)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IN2	IN1	IN0	ADCLK1	ADCLK0	ADPWR	ADRES	ADST
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0(ADST) : AD converter start to sample

By setting to "1," the AD will start to sample the data. This bit is automatically cleared by hardware after a sampling.

Bit 1(ADRES) : Resolution selection for ADC

0 → ADC is an 8-bit resolution

When 8-bit resolution is selected, the most significant (MSB) 8-bit data output of the internal 10-bit ADC will be mapped to RA PAGE1. Therefore, R5 PAGE1 Bit 6 ~ 7 will be of no use.

1 → ADC is 10-bit resolution

When 10-bit resolution is selected, 10-bit data output of the internal 10-bit ADC will be exactly mapped to RA PAGE1 and R5 PAGE1 Bit 6 ~7.

Bit 2(ADPWR) : AD converter power control, 1/0 → enable/disable

Bit 3 ~ Bit 4 (ADCLK0 ~ ADCLK1) : AD circuit 's sampling clock source.

For PLL Clock = 895.658kHz ~ 17.9MHz (CLK2~CLK0 = 001 ~ 110)

ADCLK1	ADCLK0	Sampling Rate	Operation Voltage
0	0	74.6K	>=3.5V
0	1	37.4K	>=3.0V
1	0	18.7K	>=2.5V
1	1	9.3K	>=2.5V

For PLL Clock = 447.829kHz (CLK2~CLK0 = 000)

ADCLK1	ADCLK0	Sampling rate	Operation voltage
0	0	37.4K	>=3.0V
0	1	18.7K	>=3.0V
1	0	9.3K	>=2.5V
1	1	4.7K	>=2.5V

This is a CMOS multi-channel 10-bit successive approximation A/D converter.

Features:

- 74.6kHz maximum conversion speed at 5V
- Adjusted full scale input
- External reference voltage input or internal (VDD) reference voltage
- 6 analog inputs multiplexed into one A/D converter
- Power down mode for power saving
- A/D conversion complete interrupt
- Interrupt register, A/D control and status register, and A/D data register

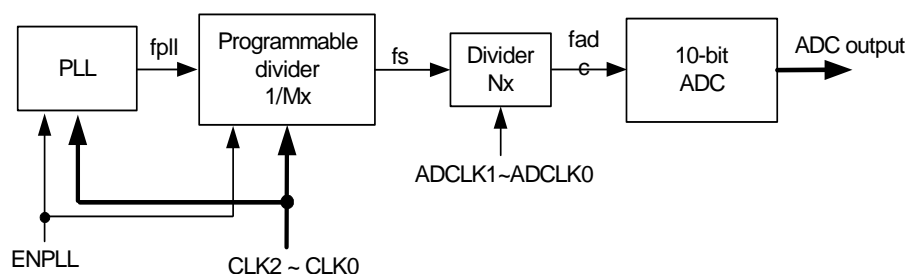


Fig. 4 ADC Voltage Control Logic

fpll	Mx	fs	fadcon = fadc / 12			
			Nx = 1	Nx = 2	Nx = 4	Nx = 8
14.331MHz	16	895.658kHz	74.638kHz	37.391kHz	18.659kHz	9.329kHz
10.747MHz	12	895.658kHz	74.638kHz	37.391kHz	18.659kHz	9.329kHz
7.165MHz	8	895.658kHz	74.638kHz	37.391kHz	18.659kHz	9.329kHz
3.582MHz	4	895.658kHz	74.638kHz	37.391kHz	18.659kHz	9.329kHz
1.791MHz	2	895.658kHz	74.638kHz	37.391kHz	18.659kHz	9.329kHz
895.658kHz	1	895.658kHz	74.638kHz	37.391kHz	18.659kHz	9.329kHz
447.829kHz	1	447.829kHz	37.391kHz	18.659kHz	9.329kHz	4.665kHz

Bit 5 ~ Bit 7 (IN0 ~ IN2) : Input channel selection of AD converter



These two bits can choose one of the three AD inputs.

IN2	IN1	IN0	Input
0	0	0	AD1
0	0	1	AD2
0	1	0	AD3
0	1	1	AD4
1	0	0	AD5
1	0	1	AD6

c) PAGE 2 (Counter 1 Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN17	CN16	CN15	CN14	CN13	CN12	CN11	CN10
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CN10 ~ CN17) : Counter1 buffer that you can read and write.

Counter1 is an 8-bit up-counter with 8-bit prescaler that allows you to use R7 PAGE2 to preset and read the counter (write → preset). After an interruption, it will reload the preset value.

7.2.9 R8 (PORT8 Output data, Data RAM address) , Counter2_LB data

a) PAGE 0 (PORT8 Output Data Register for HV)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P85	P84	P83	P82	-	-
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

b) PAGE 1 (Data RAM Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM_A7	RAM_A6	RAM_A5	RAM_A4	RAM_A3	RAM_A2	RAM_A1	RAM_A0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (RAM_A0 ~ RAM_A7) : data RAM address

c) PAGE 2 (Counter2 Low Byte Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN27	CN26	CN25	CN24	CN23	CN22	CN21	CN20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (CN20 ~ CN27) : Counter2_LB's buffer that you can read and write.

Counter2 is a 16-bit up-counter with 8-bit prescaler that allows you to use R8 PAGE2 to preset and read the counter.(write → preset). After an interruption, it will reload the preset value.



7.2.10 R9 (PORT9 I/O Data, Data RAM Data Buffer) ,Counter2_HB Data

a) PAGE 0 (PORT9 I/O Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P97	P96	P95	P94	P93	P92	P91	P90
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (P90 ~ P97) : 8-bit PORT9(0~7) I/O data register

You can use IOC register to define input or output each bit, and to define the pull high condition.

Bit 0:

1. P90 : can be defined as Input/Output
2. LED0 : can be defined as Output
3. IR Input : can be defined as Input and IR is enabled (when IOCF Bit7 is set to 1)

Bit 1 ~ Bit4:

1. P91~P94 : can be defined as Input/Output
2. LED1~LED4 : can be defined as Output
3. INT1~INT4 : can be defined as Input

Bit 5 ~ Bit7:

1. P95~P97 : can be defined as Input/Output
2. LED5~LED7 : can be defined as Output

b) PAGE 1 (Data RAM Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM_D7	RAM_D6	RAM_D5	RAM_D4	RAM_D3	RAM_D2	RAM_D1	RAM_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (RAM_D0 ~ RAM_D7) : Data RAM's data

c) PAGE 2 (Counter2 High Byte Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN215	CN214	CN213	CN212	CN211	CN210	CN29	CN28
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (CN28 ~ CN215) : Counter2_HB's buffer that you can read and write.

Counter2 is a 16-bit up-counter with 8-bit prescaler that allows you to use R9 PAGE2 to preset and read the counter (write → preset). After an interruption, it will reload the preset value.



**7.2.11 RA (PLL, Main Clock Selection, Watchdog Timer),
ADC Output Data Buffer , Counter3 Data**

**a) PAGE 0 (PLL Enable Bit, Main Clock Selection Bits,
Watchdog Timer Enable Bit)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IDLE	PLLEN	CLK2	CLK1	CLK0	-	-	WDTEN
R/W-0	R/W-0	R/W-0	R/W-1	R/W-1			R/W-0

Bit 0 (WDTEN) : Watch dog control bit

You can use WDTCLR instruction to clear watch dog counter. The counter clock source is 32768/2 Hz. If the prescaler is assigned to TCC, Watch dog will time out by $(1/32768) * 2 * 256 = 15.616mS$. If the prescaler is assigned to WDT, the time out interval will be longer depending on the prescaler. Ratio.

0/1 → disable/enable

Bit 1~Bit 2 : Unused

Bit 3 ~ Bit 5 (CLK0 ~ CLK2) : MAIN clock selection bits

You can select different frequencies for the main clock with CLK1 and CLK2. All the available clock selections are listed below.

PLLEN	CLK2	CLK1	CLK0	Sub clock	MAIN clock	CPU clock
1	0	0	0	32.768kHz	447.829kHz	447.829kHz (Normal mode)
1	0	0	1	32.768kHz	895.658kHz	895.658kHz (Normal mode)
1	0	1	0	32.768kHz	1.791MHz	1.791MHz (Normal mode)
1	0	1	1	32.768kHz	3.582MHz	3.582MHz (Normal mode)
1	1	0	0	32.768kHz	7.165MHz	7.165MHz (Normal mode)
1	1	0	1	32.768kHz	10.747MHz	10.747MHz (Normal mode)
1	1	1	0	32.768kHz	14.331MHz	14.331MHz (Normal mode)
1	1	1	1	32.768kHz	17.91MHz	17.91MHz (Normal mode)
0	Don't care	Don't care	Don't care	32.768kHz	Don't care	32.768kHz (Green mode)

Bit 6 (PLLEN) : PLL's power control bit which is CPU mode control register

0/1 → disable PLL/enable PLL

If PLL is enabled, CPU will operate at normal mode (high frequency).

Otherwise, it will run at green mode (low frequency, 32768 Hz).

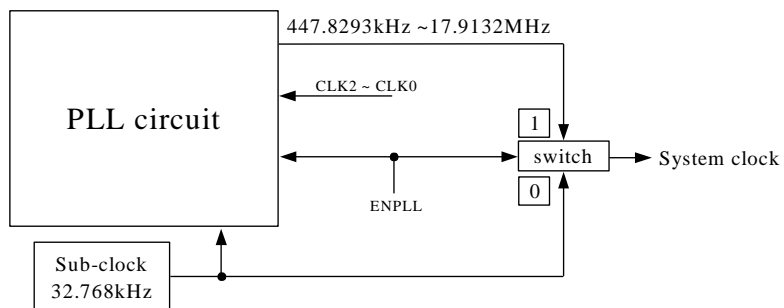


Fig. 5 The Relation Between 32.768kHz and PLL



Bit 7 (IDLE) : SLEEP or IDLE mode control as set by SLEP instruction.

0/1 → SLEEP mode/IDLE mode.

This bit allows SLEP instruction to decide which power saving mode to execute. The status after wake-up and the wake-up source list is as the shown below.

Wakeup Signal	SLEEP Mode	IDLE Mode
	RA(7,6)=(0,0) + SLEP	RA(7,6)=(1,0) + SLEP
TCC time out IOCF Bit0=1	No function	1) Wake-up 2) Jump to next instruction after SLEP
COUNTER1 time out IOCF Bit1=1	No function	1) Wake-up 2) Jump to next instruction after SLEP
COUNTER2 time out IOCF Bit2=1	No function	1) Wake-up 2) Jump to next instruction after SLEP
COUNTER3 time out IOCD Bit0=1	No function	1) Wake-up 2) Jump to next instruction after SLEP
COUNTER4 time out IOCD Bit1=1	No function	1) Wake-up 2) Jump to next instruction after SLEP
COUNTER5 time out IOCD Bit2=1	No function	1) Wake-up 2) Jump to next instruction after SLEP
PORT90(IR function) IOCF Bit3=1	Reset and jump to Address 0	1) Wake-up 2) Jump to next instruction after SLEP
WDT time out	Reset and jump to Address 0	1) Wake-up 2) Next instruction
PORTC(0~3)(Key1~Key4) RE PAGE0 Bit3 or Bit4 or Bit5 or Bit6 = 1	Reset and Jump to Address 0	1) Wake-up 2) Jump to next instruction after SLEP
PORT9(1~4) IOCF Bit4 or Bit5 or Bit6 =1 or Bit7=1	Reset and Jump to Address 0	1) Wake-up 2) Jump to next instruction after SLEP

- NOTES:**
1. PORT90 wakeup function is controlled by IOCF Bit 3. It is a falling edge or rising edge trigger (controlled by CONT register Bit7).
 2. PORT91 wakeup function is controlled by IOCF Bit 4. It is a falling edge trigger.
 3. PORT92 ~ PORT94 wakeup functions are controlled by IOCF. They are falling edge triggers.
 4. PORTC0 ~ PORTC3 wakeup functions are controlled by RE PAGE0 Bit 0 ~ Bit 3. They are falling edge triggers.

b) PAGE 1 (ADC Output Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
R	R	R	R	R	R	R	R

Bit 0 ~ Bit 7 (AD01~ AD7) : These 8 bits are full ADC data buffer



c) PAGE 2 (Counter3 Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN37	CN36	CN35	CN34	CN33	CN32	CN31	CN30
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CN30 ~ CN37) : Counter3's buffer that you can read and write.

Counter3 is an 8-bit up-counter with 8-bit prescaler that allows you to use RA PAGE2 to preset and read the counter (write → preset). After an interruption, it will reload the preset value.

7.2.12 RB (PORTB I/O Data Buffer, PORT9 Switches)

a) PAGE 0 (PORTB I/O Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R-0	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 6 (PB0 ~ PB6) : 7-bit PORTB (0~6) I/O data register

You can use IOC register to define each bit as input or output.

When the PORTB is switched to ADC–

Bit 0: is defined as VREF

Bit 1 ~ Bit 6: is defined as AD1~AD6

b) PAGE 1 (PORT9, Pull High)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH97	PH96	PH95	PH94	PH93	PH92	PH91	PH90
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (PH90 ~ PH97) : PORT9 Bit0 ~ Bit7 pull high control register

0 → disable pull high function.

1 → enable pull high function

c) PAGE 2 (Counter4 Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN47	CN46	CN45	CN44	CN43	CN42	CN41	CN40
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CN40 ~ CN47) : Counter4 buffer that you can read and write.

Counter 4 is an 8-bit up-counter with 8-bit prescaler that allows you to use RB PAGE2 to preset and read the counter.(write → preset). After an interruption, it will reload the preset value.



7.2.13 RC (PORTC I/O Data , Counter5 Data)

a) PAGE 0 I/O Data Buffer/Serial Signal

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
-	-	-	-	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 3 :1. PC0 ~ PC3 are defined as Input/Output
2. KEY1 ~ KEY4 are defined as Keyscan Input

n

b) PAGE 1 (PORTC, Pull High)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	PHC3	PHC2	PHC1	PHC0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (PHC0 ~ PHC7) : PORTC Bit0 ~ Bit7 pull high control register
0 → disable pull high function.
1 → enable pull high function

d) PAGE 2 (Counter5 Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN57	CN56	CN55	CN54	CN53	CN52	CN51	CN50
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CN50 ~ CN57) : Counter5 buffer that you can read and write.
Counter5 is an 8-bit up-counter with 8-bit prescaler that allows you to use RC PAGE2 to preset and read the counter (write → preset). After an interruption, it will reload the preset value.

7.2.14 RD (Interrupt Flag,)

a) PAGE 0 (Interrupt Flags Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	CNT5	CNT4	CNT3
-	-	-	-	-	R/W-0	R/W-0	R/W-0

NOTE: "1" means interrupt request, "0" means non-interrupt

Bit 0 (CNT3) : Counter3 timer overflow interrupt flag. Set when counter3 timer overflows.

Bit 1 (CNT4) : Counter4 timer overflow interrupt flag. Set when counter4 timer overflows.

Bit 2 (CNT5) : Counter5 timer overflow interrupt flag. Set when counter5 timer overflows.



7.2.15 RE (Interrupt Flags, Wake-up)

a) PAGE 0 (Interrupt Flags, Wake-up Control Bits)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	ADI	-	/WUPC3	/WUPC2	/WUPC1	/WUPC0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

- Bit 0 (/WUPC0) : PORTC0 wake-up control,
0/1 → disable/enable PC0 pin wake-up function
- Bit 1 (/WUPC1) : PORTC1 wake-up control, 0/1 → disable/enable PC1 pin wake-up function
- Bit 2 (/WUPC2) : PORTC2 wake-up control,
0/1 → disable/enable PC2 pin wake-up function
- Bit 3 (/WUPC3) : PORTC3 wake-up control,
0/1 → disable/enable PC3 pin wake-up function
- Bit 4(-) : Not used
- Bit 5 (ADI) : ADC interrupt flag after sampling
- Bit 6 (-) : Not used
- Bit 7(-) : Not used

7.2.16 RF (Interrupt Flags)

a) PAGE 0 (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT4	INT3	INT2	INT1	IR	CNT2	CNT1	TCIF
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

NOTE: "1" means interrupt request, "0" means non-interrupt

- Bit 0 (TCIF) : TCC timer overflow interrupt flag, Set when TCC timer overflows.
- Bit 1 (CNT1) : Counter1 timer overflow interrupt flag. Set when Counter1 timer overflows.
- Bit 2 (CNT2) : Counter2 timer overflow interrupt flag. Set when Counter2 timer overflows.
- Bit 3 (IR) : External INT pin interrupt flag. If PORT90 contains a falling /rising edge (controlled by CONT register) trigger signal, CPU will set this bit.
- Bit 4 (INT1) : External INT1 pin interrupt flag, If PORT91 contains a falling edge trigger signal, CPU will set this bit.
- Bit 5 (INT2) : External INT2 pin interrupt flag. If PORT92 has a falling edge trigger signal, CPU will set this bit.
- Bit 6 : (INT3) : External INT3 pin interrupt flag. If PORT93 has a falling edge trigger signal, CPU will set this bit.
- Bit 7 (INT4) : External IR interrupt flag. If PORT94 has a falling edge trigger signal, CPU will set this bit.



Trigger edge is as shown below:

Signal	Trigger
TCC	Time out
COUNTER1	Time out
COUNTER2	Time out
COUNTER3	Time out
COUNTER4	Time out
COUNTER5	Time out
IR	Falling Rising edge
INT1	Falling edge
INT2	Falling edge
INT3	Falling edge
INT4	Falling edge

7.2.17 R10~R3F (General Purpose Registers)

R10 ~ R1F, R20 ~ R3F (Banks 0 ~ 3) : all are general purpose registers.

7.3 Special Purpose Registers

7.3.1 A (Accumulator)

Internal data transfer, or instruction operand holding. It is not an addressable register.

7.3.2 CONT (Control Register)

CONT register is readable (CONTR) and writable (CONTW).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P90EG	INT	TS	RETBK	PAB	PSR2	PSR1	PSR0

Bit 0 ~ Bit 2 (PSR0 ~ PSR2) : TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

- Bit 3 (PAB) : Prescaler assignment bit
 0/1 → TCC/WDT
 When in WDT mode (Bit 3 = 1), the prescaler is cleared by the WDTC and SLEP instructions. Likewise, when in TCC mode (Bit 3 = 0), the prescaler will can NOT be cleared by SLEP instructions.
 An 8-bit counter is provided as prescaler for the TCC or WDT. The prescaler is available for the TCC only or for the WDT only at a given time. An 8 bit counter is made available for TCC or WDT as determined by the status of Bit 3 (PAB) of the CONT register.
 Both TCC and prescaler are cleared each time a write to TCC instruction is executed. (See the table above for the prescaler ratio under CONT register and Fig.6 below for the TCC/WDT block diagram.)
- Bit 4 (RETBK) : Return value backup control for interrupt routine
 0/1 → disable/enable
 When this bit is set to 1, the CPU will store ACC, R3 status, and R5 PAGE 1 automatically after an interrupt is triggered. It will be restored after instruction RETI. When this bit is set to 0, you need to store ACC, R3, and R5 PAGE 1 in you program.
- Bit 5 (TS) : TCC signal source
 0 → internal instruction cycle clock
 $\text{timing} = (2 / \text{system clock}) * \text{prescaler} * (256 - \text{count vaule})$
 1 → 16.384kHz
 $\text{timing} = (1 / 16.384k) * \text{prescaler} * (256 - \text{count vaule})$
- Bit 6 (INT) : INT enable flag
 0 → interrupt masked by DISI or hardware interrupt
 1 → interrupt enabled by ENI/RETI instructions
- Bit 7 (P90EG) : Interrupt edge type of P90
 0 → P90 interruption source is a rising edge signal.
 1 → P90 interruption source is a falling edge signal.

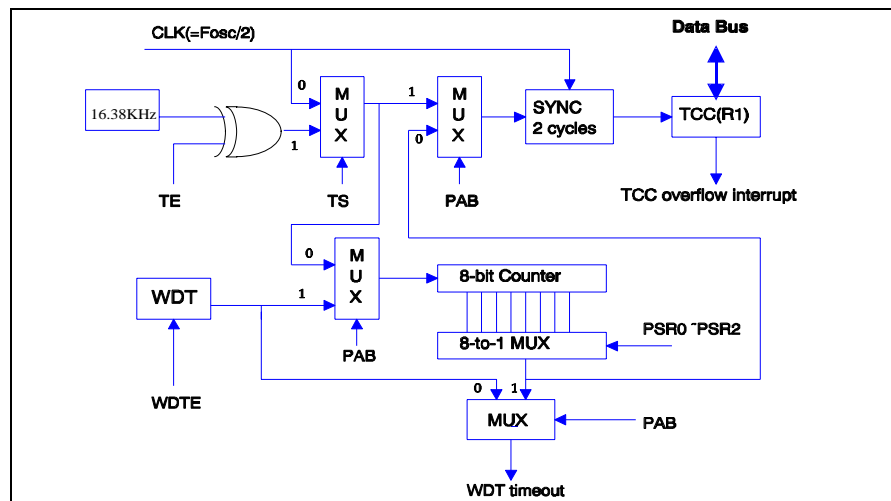


Fig. 6 TCC & WDT Block Diagram



7.3.3 IOC 5 (PORT5 Switches)

a) Page 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P57S	P56S	P55S	P54S				
R/W-0	R/W-0	R/W-0	R/W-0				

Bit 4 ~ Bit 7 (P54S~P57S) : Port5 I/O direction control register

0 → set the relative I/O pin as output HV

1 → set the relative I/O pin into high impedance

7.3.4 IOC 8

a) PAGE 1 (Clock Source and Prescaler for COUNTER1 and COUNTER2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT2S	C2_PSC2	C2_PSC1	C2_PSC0	CNT1S	C1_PSC2	C1_PSC1	C1_PSC0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 2 (C1_PSC0 ~ C1_PSC2) : COUNTER1 prescaler ratio

C1_PSC2	C1_PSC1	C1_PSC0	COUNTER1
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (CNT1S) : COUNTER1 clock source

0 → 16.384kHz

timing = (1 / 16.384k) * prescaler * (256 – count vaule)

1 → system clock

timing = (2 / system clock) * prescaler * (256 – count vaule)

Bit 4 ~ Bit 6 (C2_PSC0 ~ C2_PSC2) : COUNTER2 prescaler ratio

C2_PSC2	C2_PSC1	C2_PSC0	COUNTER2
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256



Bit 7 (CNT2S) : COUNTER2 clock source

0 → 16.384kHz

timing = (1 / 16.384k) * prescaler * (256 – count vaule)

1 → system clock

timing = (2 / system clock) * prescaler* (256 – count vaule)

7.3.5 IOC9 (PORT9 I/O Control)

a) PAGE 0 (PORT9 I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC90 ~ IOC97) : PORT9 (0~7) I/O direction control register

0 → set the relative I/O pin as output

1 → set the relative I/O pin into high impedance

b) PAGE 1 (Clock Source and Prescaler for COUNTER3 and COUNTER4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT4S	C4_PSC2	C4_PSC1	C4_PSC0	CNT3S	C3_PSC2	C3_PSC1	C3_PSC0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 2 (C3_PSC0 ~ C3_PSC2) : COUNTER3 prescaler ratio

C3_PSC2	C3_PSC1	C3_PSC0	COUNTER3
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (CNT3S) : COUNTER3 clock source

0 → 16.384kHz

timing = (1 / 16.384k) * prescaler * (256 – count vaule)

1 → system clock

timing = (2 / system clock) * prescaler* (256 – count vaule)

Bit 4 ~ Bit 6 (C4_PSC0 ~ C4_PSC2) : COUNTER4 prescaler ratio

C4_PSC2	C4_PSC1	C4_PSC0	COUNTER4
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32



1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 7 (CNT4S) : COUNTER4 clock source

0 → 16.384kHz

timing = (1 /16.384k) * prescaler * (256 – count vaule)

1 → system clock

timing = (2 / system clock) * prescaler* (256 – count vaule)

7.3.6 IOCA

a) PAGE 1 (Clock Source and Prescaler for COUNTER5)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	CNT5S	C5_PSC2	C5_PSC1	C5_PSC0
-	-	-	-	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 2 (C5_PSC0 ~ C5_PSC2) : COUNTER5 prescaler ratio

C5_PSC2	C5_PSC1	C5_PSC0	COUNTER4
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (CNT5S) : COUNTER5 clock source

0/1 → 16.384kHz/system clock

7.3.7 IOCB (PORTB I/O Control, PORTB Switch)

a) PAGE 0 (PORTB I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0
R-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 6 (IOCB0 ~ IOCB 6) : PORTB (0~6) I/O direction control register

0 → set the relative I/O pin as output

1 → set the relative I/O pin into high impedance

b) PAGE 1 (PORTB Switches)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	PB6S	PB5S	PB4S	PB3S	PB2S	PB1S	PB0S
-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0



- Bit 0 (PB0S) : Select between AD Voltage Reference pin or I/O PORTB0 pin
 0 → PB0 (I/O PORTB0) pin is selected and ADC reference voltage sourced from internal VDD
 1 → VREF (ADC external reference voltage input) pin is selected
- Bit 1 (PB1S) : Select between normal I/O PORTB1 pin or ADC Channel 1 input AD1 pin
 0 → PB1 (I/O PORTB1) pin is selected
 1 → AD1 (ADC Channel 1 input) pin is selected
- Bit 2 (PB2S) : Select between normal I/O PORTB2 pin or ADC Channel 2 input AD2 pin
 0 → PB2 (I/O PORTB2) pin is selected
 1 → AD2 (ADC Channel 2 input) pin is selected
- Bit 3 (PB3S) : Select between normal I/O PORTB3 pin or ADC Channel 3 input AD3 pin
 0 → PB3 (I/O PORTB3) pin is selected
 1 → AD3 (ADC Channel 3 input) pin is selected
- Bit 4 (PB4S) : Select between normal I/O PORTB4 pin or ADC Channel 4 input AD4 pin
 0 → PB4 (I/O PORTB4) pin is selected
 1 → AD4 (ADC Channel 4 input) pin is selected
- Bit 5 (PB5S) : Select between normal I/O PORTB5 pin or ADC Channel 5 input AD5 pin
 0 → PB5 (I/O PORTB5) pin is selected
 1 → AD5 (ADC Channel 5 input) pin is selected
- Bit 6 (PB6S) : Select between normal I/O PORTB5 pin or ADC Channel 6 input AD6 pin
 0 → PB6 (I/O PORTB6) pin is selected
 1 → AD6 (ADC Channel 6 input) pin is selected

7.3.8 IOCC (PORTC I/O Control)

a) PAGE 0 (PORTC I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	IOCC3	IOCC2	IOCC1	IOCC0
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

- Bit 0 ~ Bit 7 (IOCC0 ~ IOCC7) : PORTC(0~7) I/O direction control register
 0 → set the relative I/O pin as output
 1 → set the relative I/O pin into high impedance

b) PAGE 1 (PORTC Switches)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7S	PC6S	PC5S	PC4S	-	-	-	-
R/W-1	R/W-1	R/W-1	R/W-1	-	-	-	-

7.3.9 IOCD (Interrupt Mask, Prescaler of CN3 ~ CN5)

a) PAGE 0 (Interrupt Mask)



Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	CNT5	CNT4	CNT3
-	-	-	-	-	R/W-0	R/W-0	R/W-0

Bit 0 ~ 3 : Interrupt enable bit
 0 → disable interrupt
 1 → enable interrupt

7.3.10 IOCE (Interrupt Mask)

a) PAGE 0 (Interrupt Mask)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	ADI	-	-	-	-	-
-	-	R/W-0	-	-	-	-	-

Bit 4 (STB) : Not used

Bit 5 (ADI) : ADC interrupt flag after a sampling
 0/1 → disable/enable interrupt

Bit 6 (RBF) : Not used

7.3.11 IOCF (Interrupt Mask)

a) PAGE 0 (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT4	INT3	INT2	INT1	IR	CNT2	CNT1	TCIF
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ 7: Interrupt enable bit
 0 → disable interrupt
 1 → enable interrupt

The status after interrupt and the interrupt source lists are as shown in the table below.

Interrupt Signal	IDLE Mode	GREEN Mode	NORMAL Mode
	RA(7,6)=(1,0) + SLEP	RA(7,6)=(x,0) no SLEP	RA(7,6)=(x,1) no SLEP
TCC time out IOCF bit0=1 And "ENI"	1) Wake-up 2) Interrupt (jump to Address 8 on Page0) 3) After RETI instruction, jump to SLEP Next instruction	Interrupt (jump to Address 8 on Page0)	Interrupt (jump to Address 8 on Page0)
COUNTER1 time out IOCF bit1=1 And "ENI"	1) Wake-up 2) Interrupt (jump to Address 8 on Page0) 3) After RETI instruction, jump to SLEP Next instruction	Interrupt (jump to Address 8 on Page0)	Interrupt (jump to Address 8 on Page0)
COUNTER2 time out IOCF bit2=2 And "ENI"	1) Wake-up 2) Interrupt (jump to Address 8 on Page0) 3) After RETI instruction, jump to SLEP Next instruction	Interrupt (jump to Address 8 on Page0)	Interrupt (jump to Address 8 on Page0)



COUNTER3 time out IOCD bit0=1 And "ENI"	1) Wake-up 2) Interrupt (jump to Address 8 on Page0) 3) After RETI instruction, jump to SLEP Next instruction	Interrupt (jump to Address 8 on Page0)	Interrupt (jump to Address 8 on Page0)
COUNTER4 time out IOCD bit1=1 And "ENI"	1) Wake-up 2) Interrupt (jump to Address 8 on Page0) 3) After RETI instruction, jump to SLEP Next instruction	Interrupt (jump to Address 8 on Page0)	Interrupt (jump to Address 8 on Page0)
COUNTER5 time out IOCD bit2=1 And "ENI"	1) Wake-up 2) Interrupt (jump to Address 8 on Page0) 3) After RETI instruction, jump to SLEP Next instruction	Interrupt (jump to Address 8 on Page0)	Interrupt (jump to Address 8 on Page0)
INT1~4 IOCF bit4=1 or IOCF bit5=1 IOCF bit6 = 1 or IOCF bit7= 1 And "ENI"	1) Wake-up 2)Interrupt (jump to Address 8 on Page0) 3) after RETI instruction, jump to SLEP Next instruction	Interrupt (jump to Address 8 on Page0)	Interrupt (jump to Address 8 on Page0)
IR IOCF bit3= 1 And "ENI"	1) Wake-up 2) Interrupt (jump to Address 8 on Page0) 3) After RETI instruction, jump to SLEP Next instruction	Interrupt (jump to Address 8 on Page0)	Interrupt (jump to Address 8 on Page0)
ADI IOCE bit5 = 1 And "ENI"	No function	Interrupt (jump to Address 8 on Page0)	Interrupt (jump to Address 8 on Page0)

NOTES: 1. PORT90 interrupt function is controlled by IOCF Bit 3. It is a falling edge or rising edge trigger (controlled by CONT register Bit7).
2. PORT9 (1~4) interrupt functions are controlled by IOCF Bits 4, 5, 6, & 7). They are falling edge triggers

7.4 Application notes

1、 Call-table instruction: :

Because the call-table instruction can only change the Program Counter's bit7 ~ bit0 at each time, only 256 addresses can be searched once.

But each program page contains 1024 addresses, if call each 256 addresses as a zone, Then each page constitutes by four zones.

When a table overlaps two zones, a bug would occur during address searching.

So the member of program must examine the .LST file at any time, the .LST file will jot down the information that Assembler generated, for example source code, the coding of instruction , instruction address, error message etc.

2、 Operation requirement for the CPU :

The system frequency must adds a latency time (14.33 MHz about 250 ms ; 17.91 MHz about 450 ms.). After RA register was setting, it will offer the stable system frequency for the operation.

3、 The register initial sets to suggest

The IOC page 0 & page 1 0X0C register initial sets suggestion as follows

0x0C register value = 0B0000xxxx

The R page 0 0X0C register initial sets suggestion as follows

0x0C register value =0B0000xxxx

7.5 I/O Port

The I/O registers are bi-directional tri-state I/O ports. The I/O ports can be defined as "input" or "output" pins by the I/O control registers under program control. The I/O data registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig.7.

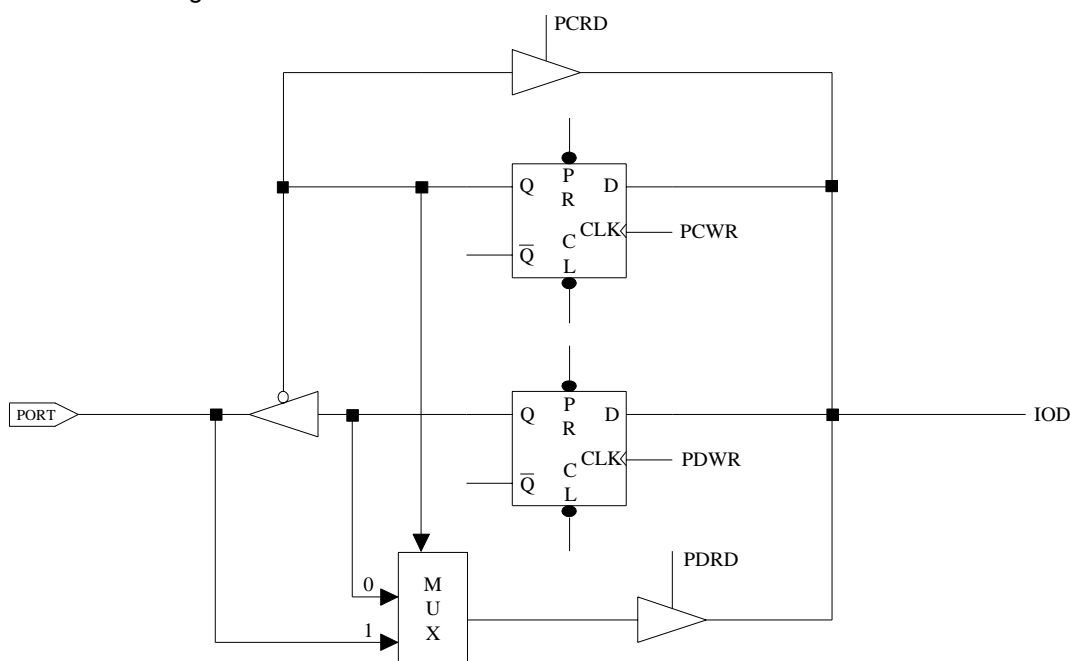


Fig. 7 The Circuit of I/O Port and I/O Control Register

7.6 RESET

A RESET can be caused by any of the following:

1. Power on reset
2. WDT timeout (if enabled and in GREEN or NORMAL mode)
3. /RESET pin pull low

Once a RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- When power on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
- The Watchdog timer and prescaler counter are cleared.
- The Watchdog timer is disabled.
- The CONT register is set to all "1"



The other registers' (Bit 7 ~ Bit 0) default values are as follows.

Address	R Register PAGE 0	R Register PAGE 1	R Register PAGE 2	R Register PAGE 3	IOC Register PAGE 0	IOC Register PAGE 1
0x4	00xxxxxx					
0x5	0000xxxx	xxxx0000	00000000			
0x6	00000000		xxxxxxx			
0x7	00000000	00000000	xxxxxxx			
0x8	00000000	00000000	xxxxxxx			00000000
0x9	00000000	xxxxxxx	xxxxxxx		11111111	00000000
0xA	00011xx0	xxxxxxx	xxxxxxx			00000000
0xB	00000000	00000000	xxxxxxx		x1111111	x0000000
0xC	1011xxxx	00000000	xxxxxxx		1111xxxx	1111xxxx
0xD	xxxxx000				xxxxx000	
0xE	X0000000				x000xxxx	
0xF	00000000				00000000	

7.7 Wake Up

The controller features two types of sleep mode for power saving:

7.7.1 SLEEP Mode, RA(6 ;7) = 0 + "SLEP" Instruction

Under this mode, the controller turns off all the CPU and crystal. However, other circuits with power control like key tone control or PLL control (with register enabled), has to be turned off through software.

7.7.2 IDLE mode, RA(6 ;7) = 1 + "SLEP" Instruction.

With this mode, the controller only turns the CPU off. The crystal remains running.

7.7.3 Wake-up from SLEEP Mode

1. WDT time out
2. External interrupt
3. /RESET pull low

Any of these cases will reset the controller and run the program from address zero. The status is just like the power-on-reset condition. Be sure to enable circuit after cases 1 or 2 occurs.



7.7.4 Wake-up from IDLE Mode

1. WDT time out
2. External interrupt
3. Internal interrupt like counters

All these cases requires you to enable the circuit before entering IDLE mode. All the registers values are preserved when "SLEP" instruction is executed and restored after wake-up.

During execution of case 2 or 3, controller will wake up and jump to address 0x08 for interruption sub-routine. After performing the sub-routine ("RETI" instruction), the program will jump to the next instruction following the "SLEP" instruction.

7.8 Interrupts

RD, RE, and RF are the interrupt status registers which record the interrupt request in flag bit. IOCD, IOCE, & IOCF are their interrupt mask registers respectively. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) is generated, it will cause the next instruction to be fetched from address 008H. Once in the interrupt service routine, the source of the interrupt can be determined by polling the flag bits in their respective (RD, RE, and RF) registers.

The interrupt flag bit must be cleared in the software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

7.9 Instruction Set

The Instruction set has the following features:

1. Every bit of any register can be set, cleared, or tested directly.
2. The I/O register can be treated as a general register. That is, the same instruction can operates on I/O register.

The symbol "R" represents a register designator which specifies which one of the 64 registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator which selects the number of the bit located in the Register "R," and affected by the operation. "k" represents an 8 or 10-bit constant or literal value.

Instruction Binary	HEX	Mnemonic	Operation	Status Affected	Instruction Cycle
0 0000 0000 0000	0000	NOP	No Operation	None	1
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C	1
0 0000 0000 0010	0002	CONTW	A → CONT	None	1
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P	1
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P	1
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None	1



0 0000 0001 0000	0010	ENI	Enable Interrupt	None	1
0 0000 0001 0001	0011	DISI	Disable Interrupt	None	1
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None	2
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None	2
0 0000 0001 0100	0014	CONTR	CONT → A	None	1
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None	1
0 0000 0010 0000	0020	TBL	R2+A → R2 bits 9,10 do not clear	Z,C,DC	2
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None	1
0 0000 1000 0000	0080	CLRA	0 → A	Z	1
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z	1
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC	1
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC	1
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z	1
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z	1
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z	1
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z	1
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z	1
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z	1
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z	1
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z	1
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC	1
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC	1
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z	1
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z	1
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z	1
0 0100 11rr rrrr	04rr	COM R	/R → R	Z	1
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z	1
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z	1
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None	2 if skip
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None	2 if skip
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C	1
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C	1
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C	1
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C	1
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None	1



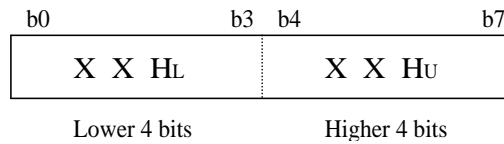
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None	1
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None	2 if skip
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None	2 if skip
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None	1
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None	1
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None	2 if skip
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None	2 if skip
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None	2
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None	2
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None	1
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z	1
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z	1
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z	1
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None	2
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC	1
1 1110 0000 0001	1E01	INT	PC+1 → [SP] 001H → PC	None	1
1 1110 100k kkkk	1E8k	PAGE k	K->R5(4:0)	None	1
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC	1



8 Segment Data Buffers

The ePVP6810 chip provides a total of 128 bytes data RAM. On the other hand, display Segment Data Buffers can be stored either in the data RAM of 128 bytes sizes (00h~40h) or in the common registers of Bank 2 and Bank 3 (20h~3Fh).

These buffers store display RAM. The display RAM stores the data transmitted from an external device to the ePVP6810 through the serial interface and is assigned addresses as follows, in units of 8 bits:



c) Display Memory Addresses:

Seg1	Seg4	Seg8	Seg9	
00 HL	00 HU	01 HL	01 HU	DIG1
02 HL	02HU	03 HL	03 HU	DIG2
04 HL	04 HU	05 HL	05 HU	DIG3
06 HL	06 HU	07 HL	07 HU	DIG4
08 HL	08 HU	09 HL	09 HU	DIG5
0A HL	0A HU	0BHL	0BHU	DIG6
0C HL	0C HU	0D HL	0D HU	DIG7
15 HL	15 HU	16 HL	16 HU	DIG8
0E HL	0E HU	0F HL	0F HU	DIG9
10 HL	10 HU	11 HL	11 HU	DIG10
12 HL	12HU	13 HL	13 HU	DIG11
14 HL	14 HU	15 HL	15 HU	DIG12

b) Key Scanning Data Buffers:

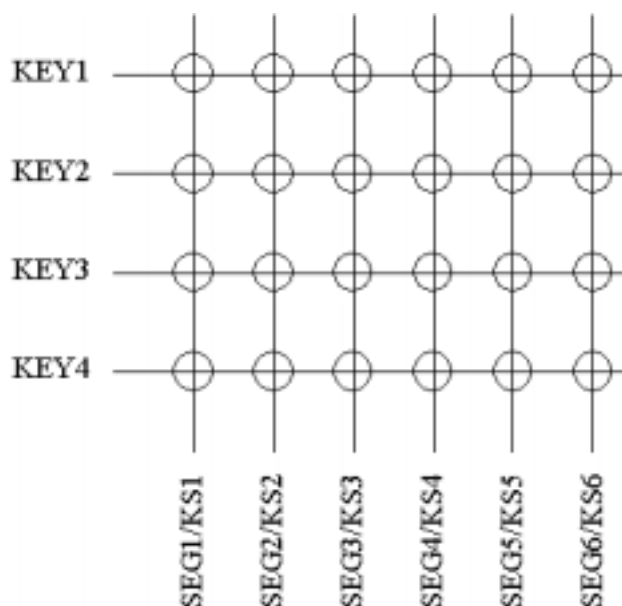


Fig. 8 6 x 4 Configuration Key Matrix

The key matrix is of 6 x 4 configuration is as shown in the above figure.

The data of each key is stored as illustrated below, and is read by a read command, starting from the least significant bit.

KEY1....KEY4	KEY1....KEY4
SEG1/KS1	SEG2/KS2
SEG3/KS3	SEG4/KS4
SEG5/KS5	SEG6/KS6
b0 -- -- b3	b4 -- -- b7

When the most significant bit of data (SEG6, b7) has been read, the least significant bit of the next data (SEG1, b0) is read.

Fig. 9 Display Mode Setting Command Selection

9 Crystal OSC

9.1 General Description

This oscillator is designed for the ePVP6810 chip as clock source.

9.2 Features

- RC oscillator: 32.768K Hz
- Operating voltage: 2.2~5.5V.
- Operating temperature: -20 °C ~ 70 °C

9.3 Block Diagram

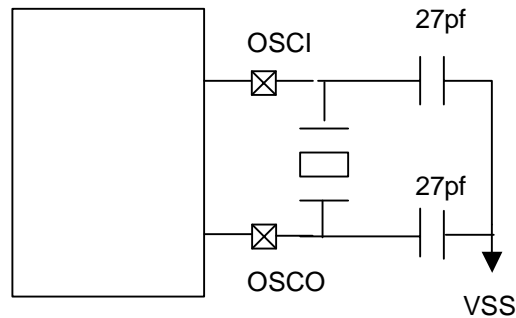


Fig. 13 Crystal OSC Block Diagram

9.4 Pin Description

Name	I/O Type	Description	Remarks
XIN	I	Crystal oscillator connection pin	
XOUT	O	Crystal oscillator output pin	
VDD	-	Power supply (+) pin	
VSS	-	Power supply (-) pin	

9.5 Electrical

(Condition : VDD = 4.5 to 5.5V, Ta = -20°C to 70°C)

Parameters	Sym.	Min.	Typ.	Max.	Unit	Conditions
Starting oscillation voltage	Vs	-	2.0	3.2	V	
Stable time	Ts	-	5	10	clk	Vdd = 5.0V
Current consumption	Idd	-	2	3	mA	Vdd = 5.0V
Duty cycle		45	50	55	%	
Frequency/Voltage deviation	$\partial f/\partial V$	-	1	1.5	%	
Frequency/Temperature deviation	Δf	-	1	2	%	
Frequency vs. Process deviation		-	± 6	± 10	%	



10 Absolute Operation Maximum Ratings

Absolute maximum ratings ($T_a = 25^\circ\text{C}$, $V_{ss} = 0\text{ V}$)

Parameter	Symbol	Ratings	Unit
Logic supply voltage	V_{DD}	-0.5 to + 6	V
Driver supply voltage	V_{EE}	$V_{DD} + 0.5$ to $V_{DD} - 45$	V
Logic input voltage	V_I	-0.5 to $V_{DD} + 0.5$	V
VFD driver output voltage	V_O	$V_{EE} - 0.5$ to $V_{DD} + 0.5$	V
LED driver output current	I_{O1}	+25	mA
VFD driver output current	I_{O2}	-40 (Grid) -15 (Segment)	mA
Operating ambient temperature	T_{opt}	-40 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}	-65 to +150	$^\circ\text{C}$

11 DC Electrical Characteristic

($T_a = -20$ to $+70^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{ss} = 0\text{V}$, $V_{EE} = V_{DD} - 45\text{V}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Digital Input Voltage High	V_{IH}	$0.8V_{DD}$	-	V_{DD}	V	GPIOB
Digital Input Voltage Low	I_{OL}	V_{SS}	-	$0.2V_{DD}$	V	
Schmitt Trigger Negative Going Threshold Voltage	V_{T-}	1.5	1.8	2.1		GPIOC, GPO9, /RESET, GPIOB
Schmitt Trigger Positive Going Threshold Voltage	V_{T+}	2.9	3.2	3.5	V	
Input Leakage Current	I_{IN}	-	-	± 1	μA	GPIOB, $V_{IN} = V_{DD}$ or V_{SS}
Pull Up Resister	R_{PU}	50	75	100	K	GPIOC, GPO9 and /RESET @ $V_{DD}=5\text{V}$
Digital Output Voltage High	V_{OH}	$0.8V_{DD}$	-	V_{DD}	V	GPIOB, GPIOC
Digital Output Voltage Low	V_{OL}	V_{SS}	-	$0.2V_{DD}$	V	
Digital Output High Current	I_{OH1}	-2	-4	-5	mA	$V_{OH}=2.4\text{V}$, GPIOB, GPIOC
Digital Output Low Current	I_{OL1}	2	4	5	mA	$V_{OL}=0.4\text{V}$, GPIOB, GPIOC
Digital Output High Current	I_{OH2}	-15	-18	-25	mA	$V_{OH}=2.4\text{V}$ / GPIO9
Digital Output Low Current	I_{OL2}	15	18	25	mA	$V_{OL}=0.4\text{V}$ / GPIO9
HV Output Current	I_{OH1}	- 6	- 4	- 3	mA	$V_o = V_{DD} - 2\text{V}$, ($V_{DD}=5\text{V}$) SEG1/KS1 to SEG6/KS6
HV Output Current	I_{OH2}	-15	-13	-11	mA	$V_o = V_{DD} - 2\text{V}$, ($V_{DD}=5\text{V}$) GR1 to GR9, GR10/SG9, GR12/SG7
HV leakage current	I_{HVLEAK}	5	8	10	μA	$V_o = V_{DD} - 45\text{V}$, driver off
HV Output pull-down resistor	R_L	40	80	120	K Ω	Driver output ($V_{EE} = -25\text{V}$)



Power down current (SLEEP mode)	I _{SB1}		-	1.5	μA	All input and I/O pin at VDD, output pin floating, WDT disabled
Low clock current (GREEN mode) Crystal oscillation operating mode	I _{SB2}		30	60	μA	VDD =3V CLK=32.768KHz, all analog circuits disabled, all input and I/O pin at VDD, output pin floating
			65	90	μA	VDD =5V CLK=32.768KHz, all analog circuits disabled, all input and I/O pin at VDD, output pin floating
Low clock current (IDLE mode) Crystal oscillation operating mode	I _{SB3}		30	45	μA	VDD =3V CLK=32.768KHz, all analog circuits disabled, all input and I/O pin at VDD, output pin floating
			45	60	μA	VDD =5V CLK=32.768KHz, all analog circuits disabled, all input and I/O pin at VDD, output pin floating
Operating supply current (Normal mode) Crystal oscillation operating mode	I _{CC}		1.3	2	mA	/RESET=High, CLK=3.582MHz, all analog circuits disabled, output pin floating

12 AC Electrical Characteristic

11.1 CPU Instruction Timing (Ta = -20°C ~ 70°C, VDD=5V, VSS=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input CLK duty cycle	Dclk		45	50	55	%
Instruction cycle time	Tins	32.768kHz		60		us
		3.582MHz		550		ns
Device delay hold time	Tdrh			16		ms
TCC input period	Ttcc	Note 1	(Tins+20)/N			ns
Watchdog timer period	Twdt	Ta = 25°C		16		ms

NOTE: N= selected prescaler ratio

12.2 AC Timing Characteristic (VDD=5V, Ta=+25°C)

Description	Symbol	Min	Typ	Max	Unit
Oscillator timing characteristic					
OSC start up	32.768kHz	Tosc	400	1500	ms
	3.579MHz PLL		5	10	us

12.3 ePVP6810 Operating Voltage VS main clock

(X Axis → Min VDD ; Y Axis → Main CLK)

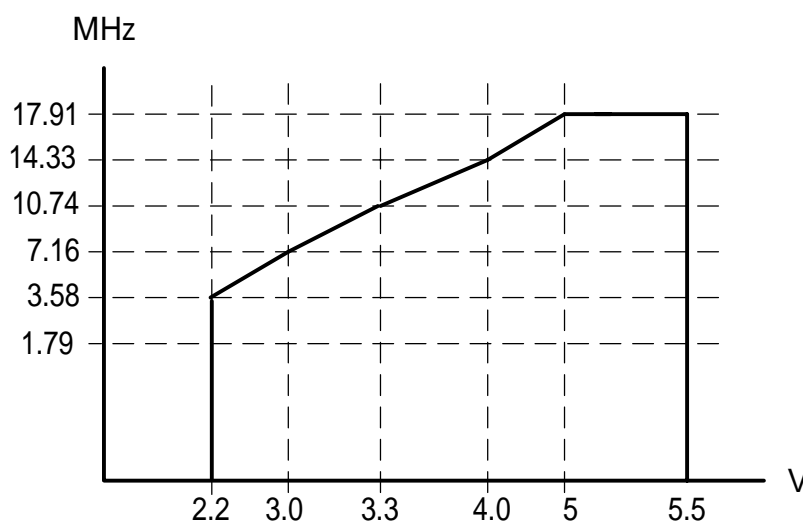
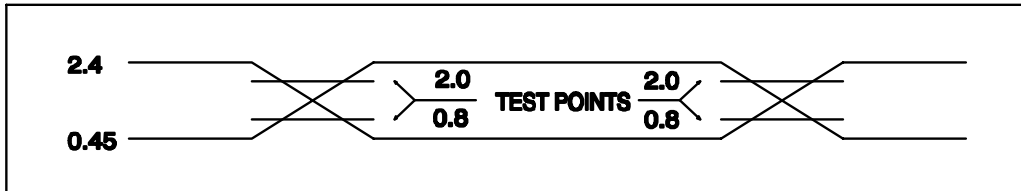


Fig. 14 Operation Voltage XY Axis



12.4 AC Timing Diagrams

AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

Fig. 15a A/C Test Input/Output Waveform

RESET Timing

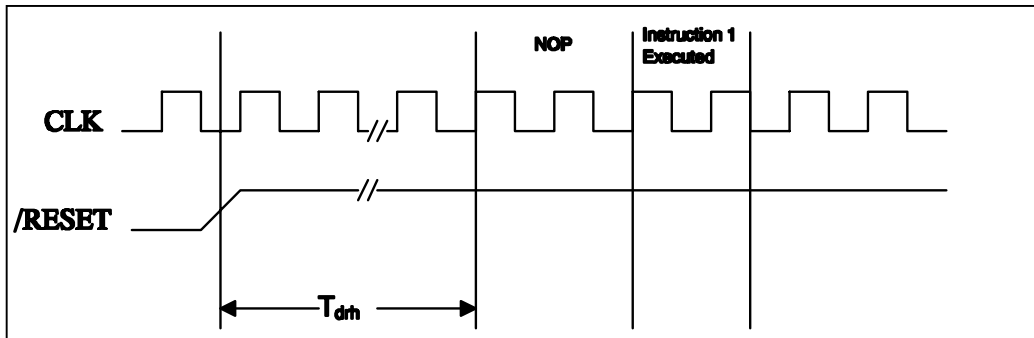


Fig. 15b RESET Timing Diagram

TCC Input Timing

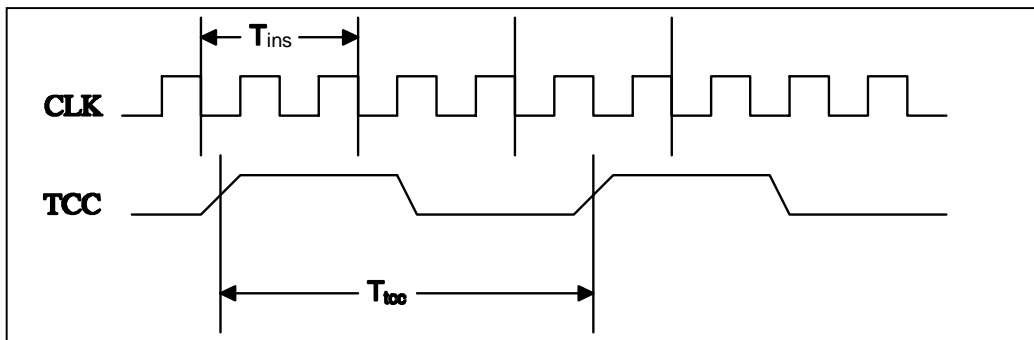


Fig. 15c TCC Input Timing Diagram

13 Key & Switch Scanning and Display Timing

The key & switch scanning and display timing diagram is given below. One cycle of key & switch scanning consists of 2 frames. The data of the 4 x 4 matrix is stored in the RAM.

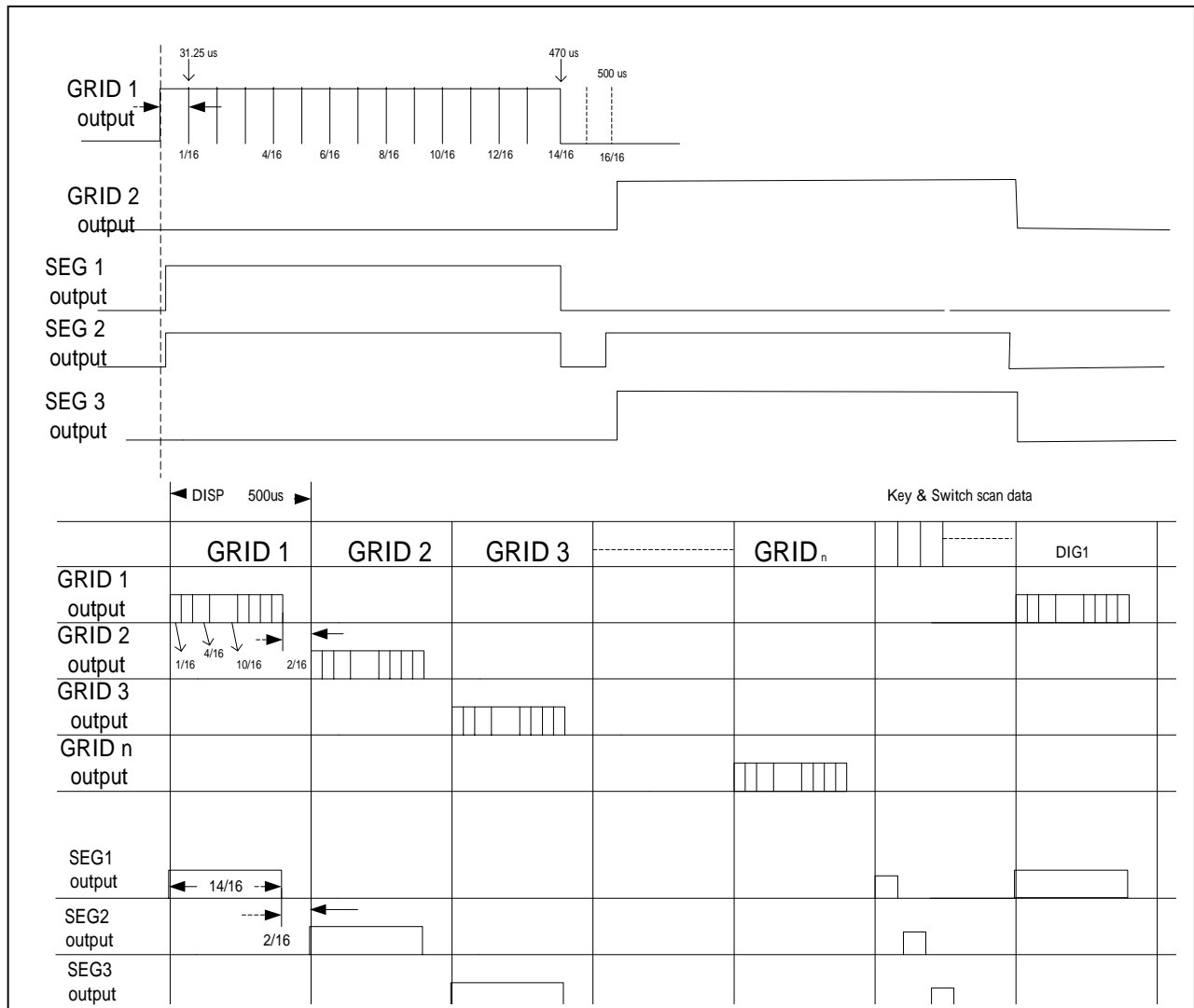


Fig. 16 Key & Switch Scanning and Display Timing Diagram

14 Switching Characteristic Waveform

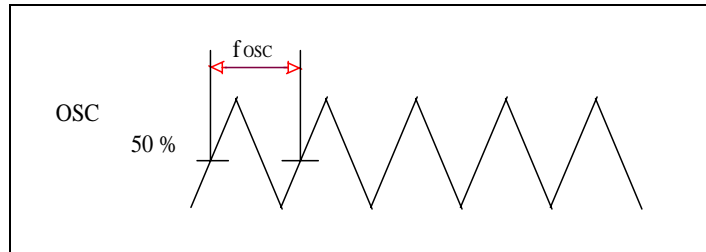
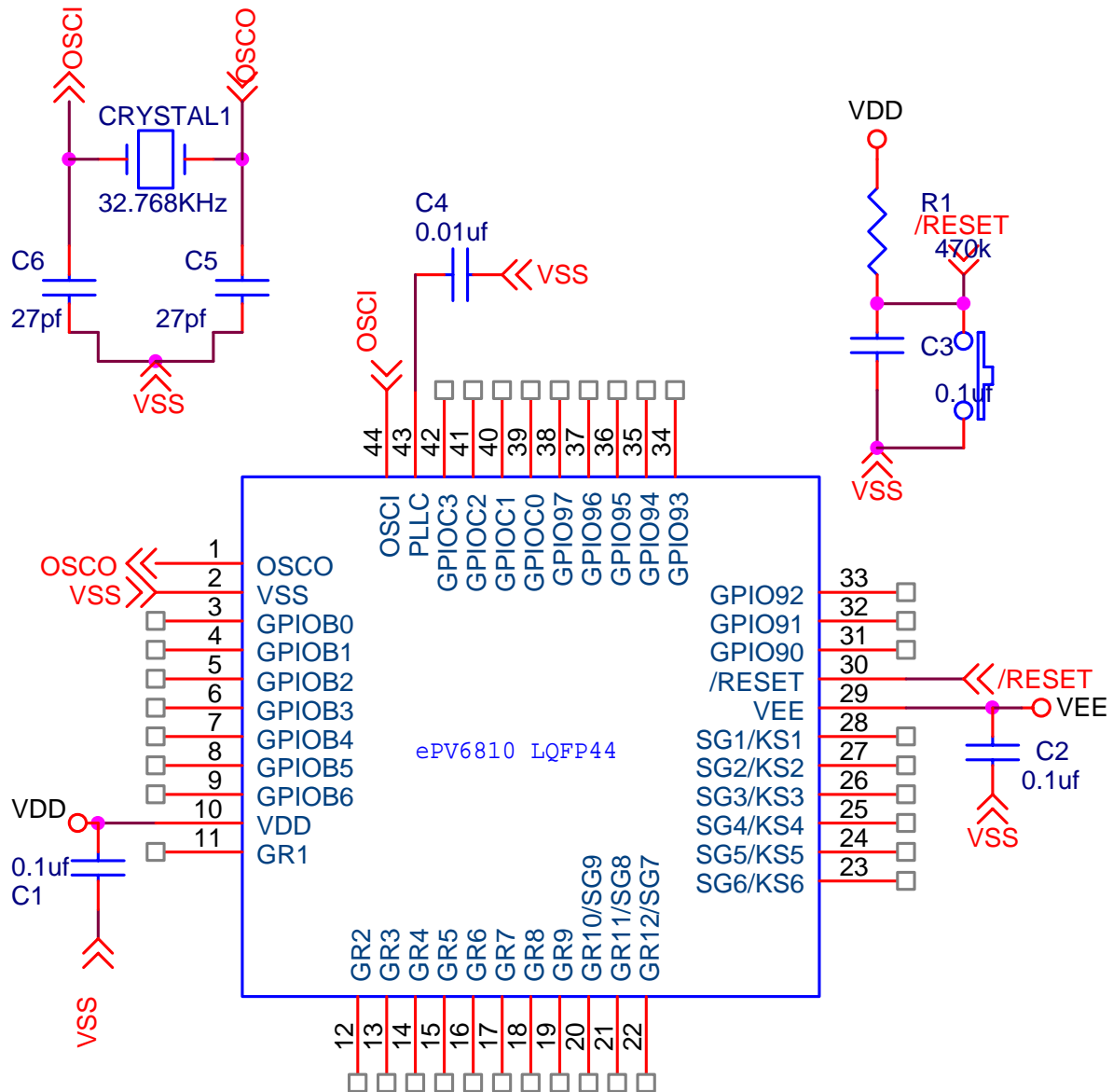


Fig. 19a Switching Characteristic Waveform

14.1 Switching Characteristics (Ta = - 20 to + 70°C, VDD = 4.5 to 5.5V, VEE = VDD - 45V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Oscillation frequency	tOSC	-	32.768	-	KHz	
Propagation delay time	tPLZ	-	-	300	ns	CLK→DOUT
	tPZL	-	-	100	ns	CL = 15pF, RL = 10KΩ
Rise time	tTZH1			2	us	CL = 100pF VEE = -25V SEG1/KS1 to SEG4/KS4, GR1 to GR9 GR10/SG9 to GR12/SG7
	tTZH2			0.5	μs	
Fall time	tTHZ	100	110	120	μs	CL = 100pF, VEE = -25V, SEGn, GRIDn

15.2、 Application circuit





15 .2、 Package Information

(1) Package Type: Plastic LQFP-44

