

512 Bit Electrically Alterable Read Only Memory

FEATURES

- 64 word x 8 bit organization
- 6 bit binary addressing
- +5, -28V power supplies
- Word Alterable
- 10 year data storage for ER2055 (at +70°C)
- 1 year data storage for ER2055 IR (at +85°C) and ER2055 HR (at +125°C)
- TTL compatible with pull-up resistors on inputs
- Tri-state outputs
- Read Time: 2 μ s (ER2055), 4 μ s (ER2055 IR and ER2055 HR)
- Write/Erase Time: 50ms (ER2055), 100ms (ER2055 HR)
- No voltage switching required
- 2 chip selects
- Two extended temperature ranges:
 - 40°C to +85°C (Industrial) Part # ER2055 IR
 - 55°C to +125°C (Hi-Rel) Part # ER2055 HR

DESCRIPTION

The ER2055 is a fully decoded 64 x 8 electrically erasable and reprogrammable ROM. Write, erase, and read voltages are switched internally via a 2-bit code applied to C1 and C2.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 512 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

OPERATION

Data is stored in a two transistor memory cell. After the cell is preconditioned by an erase signal (which causes a positive shift in the threshold of both transistors), data is written into one of the transistors making its threshold more negative. A sensing flip flop is used to read the memory cell and presents a logic high or low to the output depending on which transistor is "written".

The ER2055 EAROM may be operated with V_{SS} between +5 and +10 volts for either TTL or CMOS compatibility. The negative power supply, V_{GG} , should be adjusted so that the difference between V_{SS} and V_{GG} is always 33 volts.

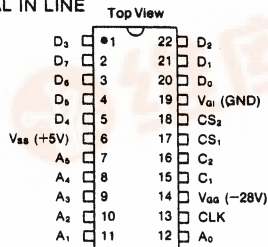
It is important to note two things: first, that an erase is required before a write to precondition the cell, and second, that after an erase, both transistors will have the same threshold voltage and valid data will not be present at the output.

PIN FUNCTIONS

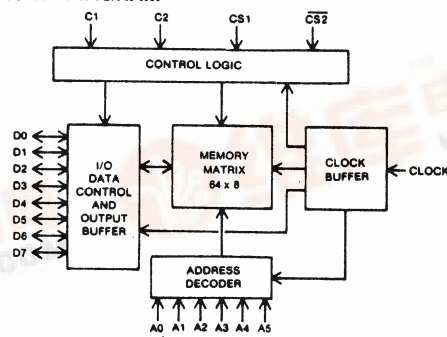
A_0 - A_5	6-Bit Word Address
D_0 - D_7	Data input and output pins
CS_1 , CS_2	Chip Selects Chip selected at logic "1" on CS_1 and logic "0" on CS_2 . When chip is not selected, outputs are open circuit, read; write and erase are disabled. Power is reduced.
C_1 , C_2	Mode Control Inputs
C_1 C_2	
0 1	Erase Mode: stored data is erased at addressed location.
1 0	Read Mode: addressed data read after clock pulse. Output data retained at output pins until next read operation.
0 0	Write Mode: input data written at addressed location. Clock not required.
CLK	Clock Input. Pulse to logic "1" for read operation. Data will remain valid for 20 to 60 seconds; the outputs will then become open circuit until another clock pulse is received.
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GG}	Ground Input.
V_{GG}	Power Supply Input. Normally at -28 volts.

PIN CONFIGURATION

22 LEAD DUAL IN LINE



BLOCK DIAGRAM

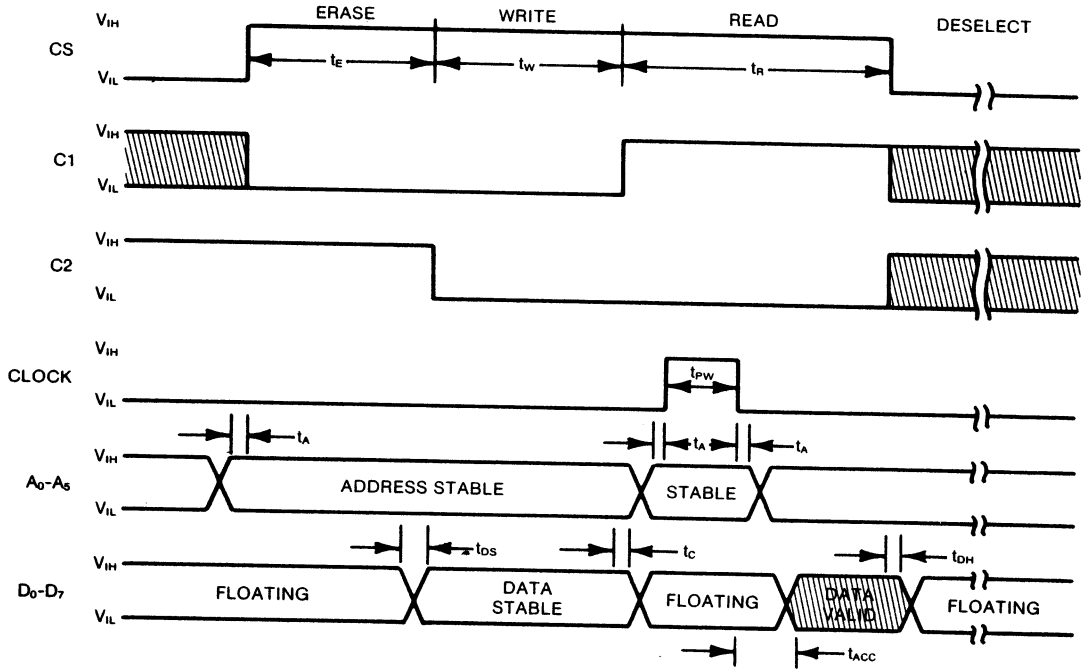


The ER2055 EAROM uses dynamic edge triggered circuits internally. This requires either a mode change, a clock or a transition of the chip selects between successive operations. Thus successive operations in the same mode must be separated by transition of one of these four lines. Clock pulses are not normally required during erase or write operations, but are needed for successive operations if the chip select is held high, i.e., applications where one EAROM is used.

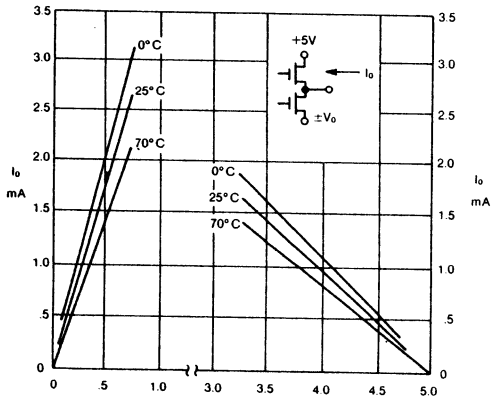
In using the read clock to refresh the outputs during a read operation a minimal frequency is recommended to insure that the read cycle lifetime between writes (N_{RA}) is kept to a maximum.

The ER2055 IR and ER2055 HR are screened to Mil Std. 883B/method 5004.1/level B, pre-cap visual inspection, environmental testing, burn-in and external visual. They are available in 28 lead ceramic dual in line packages.

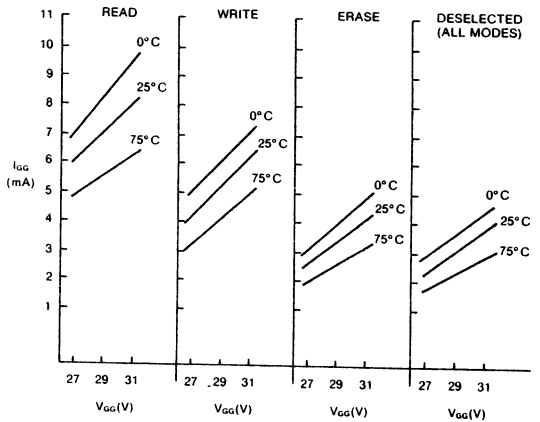
TIMING DIAGRAM



TYPICAL OUTPUT CHARACTERISTICS



TYPICAL SUPPLY CURRENT VS POWER SUPPLY VOLTAGE



ELECTRICAL CHARACTERISTICS**Maximum Ratings***

All inputs and outputs (with respect to V _{ss})	-35V to +0.3V
Storage temperature	-65°C to +150°C
Soldering temperature of leads (10 seconds)	+300°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (for TTL Compatibility)

V_{SS} = +5V ±5%

V_{GG} = -28V ±5%

V_{GI} = GND

Operating Temperature T_A = 0°C to +70°C for ER2055T_A = -40°C to +85°C for ER2055 IRT_A = -55°C to +125°C for ER2055 HR

Output Load = 100pF, 1 TTL load

Characteristics	Sym	ER2055			ER2055 IR/ER2055 HR			Units	Conditions
		Min.	Typ.**	Max.	Min.	Typ.**	Max.		
DC CHARACTERISTICS									
Input Logic "1"	V _{IH}	V _{SS} -1.5	—	V _{SS} +0.3	V _{SS} -1.5	—	V _{SS} +0.3	V	I _{OH} = 100μA I _{OL} = 1.6mA for V _{SS} = 5V V _{IH} = V _{SS} -15 Chip deselected
Input Logic "0"	V _{IL}	V _{SS} -15	—	0.8	V _{SS} -10	—	0.6	V	
Output Logic "1"	V _{OH}	V _{SS} -1.5	—	—	V _{SS} -1.5	—	—	V	
Output Logic "0"	V _{OL}	—	—	0.6	—	—	0.6	V	
Input Leakage	I _L	—	2	10	—	2	10	μA	
Output Leakage	I _O	—	2	10	—	2	10	μA	
Power Supply Current									
Read	I _{GG}	—	8	10	—	8	13	mA	I _{SS} approx. I _{GG}
Write	I _{GG}	—	6	7	—	6	9	mA	I _{SS} approx. I _{GG}
Erase	I _{GG}	—	4	6	—	4	8	mA	I _{SS} approx. I _{GG}
Deselected	I _{GG}	—	3	4	—	3	6	mA	I _{SS} approx. I _{GG}
AC CHARACTERISTICS									
Access Time	t _{ACC}	—	—	2.0	—	—	4.0	μs	
Clock Pulse width	t _{PW}	2.0	—	20.0	2.0	—	20.0	μs	
Erase Cycle Time	t _E	50	—	200.0	100	—	200.0	ms	
Write Cycle Time	t _W	50	—	200.0	100	—	200.0	ms	
Read Cycle Time	t _R	5.0	—	24.0	6.0	—	25.0	μs	
Address to Clock Time	t _A	50	—	—	50	—	—	ns	
Data Set Up Time	t _{DS}	50	—	—	50	—	—	ns	
Data Hold Time	t _{DH}	50	—	—	50	—	—	ns	
Control to Address & Data Change	t _C	0	—	—	0	—	—	ns	
Number of Reads/Word Refresh	N _{RA}	10 ¹¹	—	—	10 ¹¹	—	—	—	
Number of Erase/Write Cycles	N _W	10 ⁶	—	—	10 ⁵	—	—	—	
Input Capacitance, all pins	C _{IO}	—	6	10	—	6	10	pF	
Unpowered Data Storage Time	t _S	10	—	—	1	—	—	Years	at max. temperature
Power Dissipation Read Cycle	P _D	—	450	500	—	450	500	mW	at 25°C V _{SS} = +5, V _{GG} = -29
	P _D	—	not applicable	—	—	—	500	mW	at 125°C V _{SS} = +5, V _{GG} = -29
	P _D	—	not applicable	—	—	—	600	mW	at -55°C V _{SS} = +5, V _{GG} = -29
Pulse Rise, fall time	t _{R1} t _F	10	—	100	10	—	100	ns	

**Typical values are at +25°C and nominal voltages.