ESS Technology, Inc.

ES3880
Video CD MPEG Processor
Product Brief

DESCRIPTION

The ES3880 Video CD MPEG processor is ESS' third generation highly integrated, optimal quality, and cost-effective single chip solution for Video CD players. The ES3880 is the best quality available for both video and audio and easily passes the highest graded level for the China VCD standard. The ES3880 integrates MPEG-1 video and audio processing and a full-fledged MPEG system bit stream parser. The ES3880 can be used as a microcontroller to provide system control, while also performing such basic video operations as arbitrary scaling and video filtering. The MPEG-1 system layer bitstream is decoded at up to 9 Mb/s at Standard Intermediate Format (SIF) resolution with a picture rate of 30 frames per second. Two channels of MPEG-1 Layer 1 or Layer 2 audio are decoded simultaneously.

The ES3880 supports SmartScale advanced scaling techniques, along with SmartStream for audio and video error concealment, and SmartZoom for enabling in/out zooming of a particular area of a still picture or movie. Additional features include DiscScan, TrackScan, QuickScan, On-Screen-Display (OSD), Karaoke, Playback Control (PBC) for Video CD 2.0, and entertainment game software. System control and house-keeping functions (keypad and remote control) are also provided.

The ES3880 can be implemented with the ES3883 Video CD Video Encoder, which integrates most of the analog discrete components required for a Video CD player. Figure 1 shows a typical Video CD system using the ES3880 and the companion ES3883 video encoder. When the ES3880 and ES3883 are used in the design, enhanced support for 3DSound and SurroundSound is realized, along with support for interactive games.

The ES3880 is available in an industry-standard 100-pin Plastic Quad Flat Pack (PQFP) package.

FEATURES

- Programmable Multimedia Processor (PMP) architecture
- MPEG-1 audio/video decoder and system parser
- CD block decoder functions
- Video interlacing hardware
- Color Space Conversion (CSC)
- STC interpretation and video/audio Phase-lock Loop (PLL)
- Supports both 8- and 16-bit YUV output
- 256/384 frame sampling frequency for audio system clock
- Programmable master clock for external audio DAC
- Independent bit clock for audio transmit and receive
- SmartScale video scaling supports X- and Y-axis interpolation
- SmartZoom supports 4X picture enlargement and reduction
- SmartStream supports audio and video bit stream error concealment
- SmartVocal: cancels the vocal on an audio-CD
- Karaoke function
- Video Fader for fading video image (in and out)
- On-screen-Display (OSD)
- Playback Control (PBC) for Video CD 2.0
- Trick mode functions (Repeat, Goto, Set A-B, etc.)
- DiscScan, TrackScan, and QuickScan
- Video CD 1.1 and 2.0, and Audio CD compatible
- Power management
- 3.6 V power supply with 5 V tolerant I/O's
- 100-pin PQFP
- Can be used with either serial or parallel interfaces

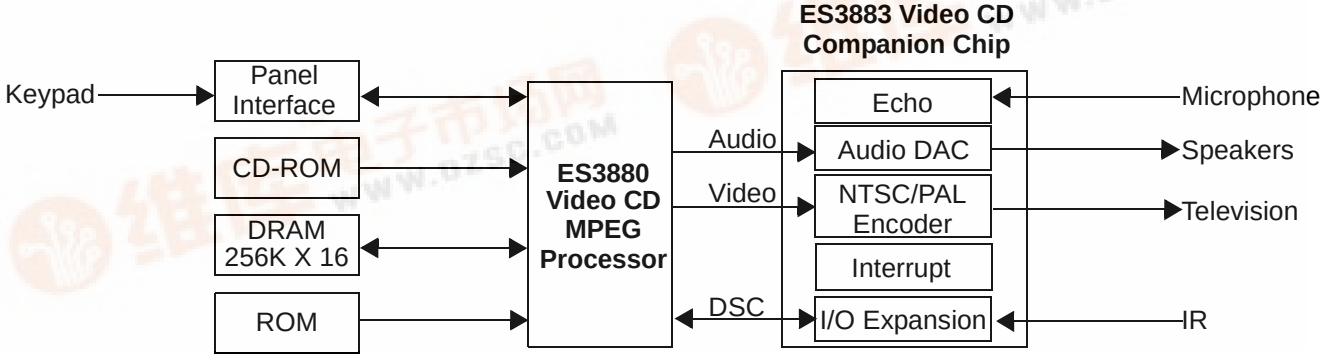

Figure 1 ES3880 System Block Diagram

ES3880 PINOUT

Figure 2 shows the ES3880 device pinout.

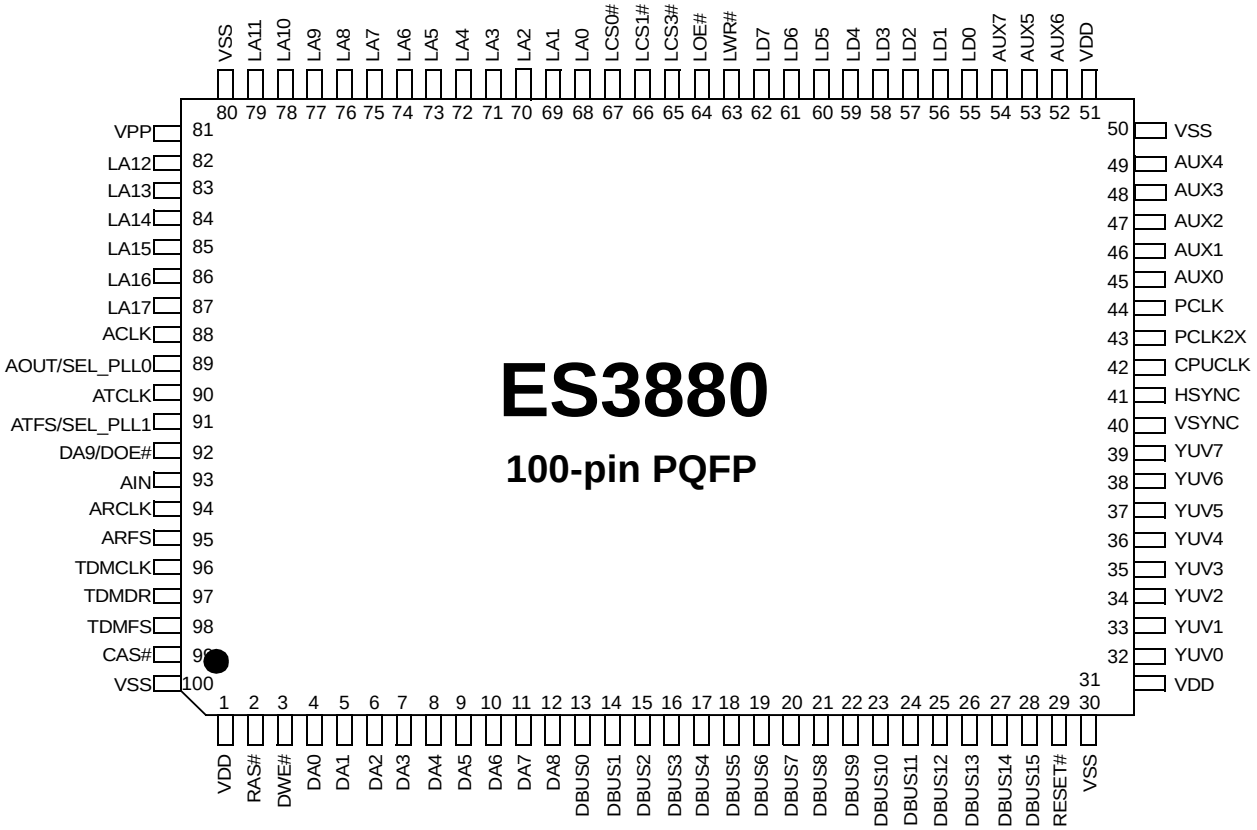

Figure 2 ES3880 Device Pinout

PIN DESCRIPTION

Table 1 lists the pin descriptions for the ES3880.

Table 1 ES3880 Pin Descriptions List

Name	Number	I/O	Definition
VDD	1, 31, 51	I	3.3V power supply.
RAS#	2	O	Row address strobe.
DWE#	3	O	DRAM write enable.
DA[8:0]	12:4	O	DRAM multiplexed row and column address bus.
DBUS[15:0]	28:13	I/O	DRAM data bus.
RESET#	29	I	System reset.
VSS	30, 50, 80, 100	I	Ground.
YUV[7:0]	39:32	O	YUV[7:0] 8-bit video data bus.
VSYNC	40	I/O	Vertical sync.
HSYNC	41	I/O	Horizontal sync.
CPUCLK	42	I	RISC and system clock input. CPUCLK is used only if SEL_PLL[1:0] = 00 to bypass PLL.
PCLK2X	43	I/O	Doubled 54 MHz pixel clock.
PCLK	44	I/O	27 MHz pixel clock.
AUX[7:0]	54:52, 49:45	I/O	Auxiliary control pins 7:0. AUX0 and AUX1 are open collectors.
LD[7:0]	62:55	I/O	RISC interface data bus.
LWR#	63	O	RISC interface write enable.
LOE#	64	O	RISC interface output enable.
LCS[3,1,0]#	65, 66, 67	O	RISC interface chip select.
LA[17:0]	87:82, 79:68	O	RISC interface address bus.
VPP	81	I	5.0V power supply.
ACLK	88	I/O	Master clock for external audio DAC.
AOUT	89	O	Audio interface serial data output when selected.
SEL_PLL0		I	System and DSCK output clock frequency selection at reset time. The matrix below lists the available clock frequencies and their respective PLL bit settings.
ATCLK	90	I/O	Audio transmit bit clock.
ATFS	91	O	Audio transmit frame sync.
SEL_PLL1		I	Refer to the description and matrix for SEL_PLL0 pin 89.
DA9	92	O	DRAM multiplexed row and column address line 9.
DOE#		O	DRAM output enable.
AIN	93	I	Audio serial data input.
ARCLK	94	I	Audio receive bit clock.
ARFS	95	I	Audio receive frame sync.
TDMCLK	96	I	TDM serial clock.

SEL_PLL1	SEL_PLL0	DCLK
0	0	Bypass PLL (input mode)
0	1	54 MHz (output mode) Default
1	0	67.5 MHz (output mode)
1	1	81.0 MHz (output mode)

Table 1 ES3880 Pin Descriptions List (Continued)

Name	Number	I/O	Definition
TDMDR	97	I	TDM serial data receive.
TDMFS	98	I	TDM frame sync.
CAS#	99	O	DRAM column address strobe.

BLOCK DIAGRAM

Figure 3 provides a functional block diagram of the ES3880.

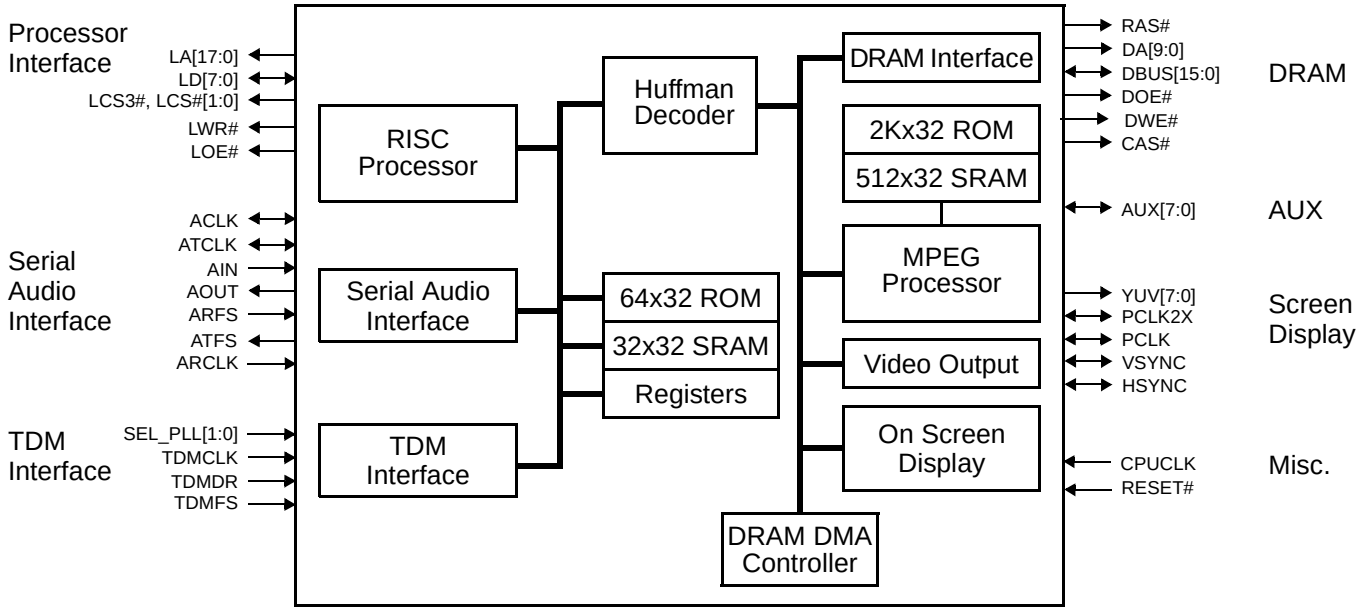

Figure 3 ES3880 Functional Block Diagram

ORDERING INFORMATION

Part Number	Description	Package
ES3880	Video CD MPEG Processor	100-pin PQFP

ESS Technology, Inc.
48401 Fremont Blvd.
Fremont, CA 94538
Tel: 510-492-1088
Fax: 510-492-1098