

Application Specific Discretes A.S.D.TM

APPLICATIONS

Where transient overvoltage protection in esd sensitive equipment is required, such as :

- COMPUTERS
- PRINTERS
- COMMUNICATION SYSTEMS

It is particulary recommended for RS232 I/O port protection where the line interface withstands 2 kV, ESD surges.

FEATURES

- 18 BIDIRECTIONAL TRANSIL[™] FUNCTIONS
- LOW CAPACITANCE : C = 30pF @ V_{RM} DZSC.COM
- 500 W peak pulse power (8/20 μs)

DESCRIPTION

The ESDA25DB3 is a dual monolithic voltage suppressor designed to protect components which are connected to data and transmission lines against ESD.

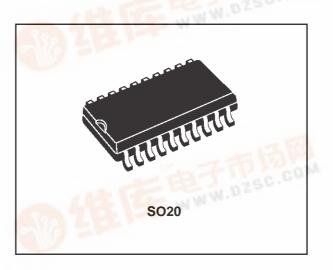
BENEFITS

High ESD protection level : up to 25 kV **High integration** Suitable for high density boards

COMPLIES WITH THE FOLLOWING STANDARDS :

IEC 1000-4-2: level 4

MIL STD 883C-Method 3015-6: class 3 (human body model)

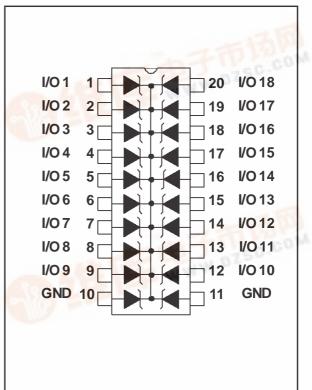


ESDA25DB3

TRANSIL[™] ARRAY

FOR ESD PROTECTION

FUNCTIONAL DIAGRAM





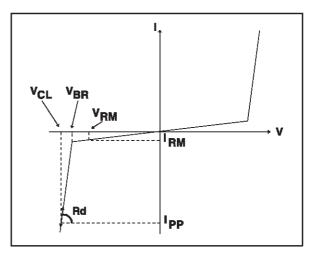
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ABSOLUTE MAXIMUM RATINGS ($T_{amb} = 25^{\circ}C$)

Symbol	Parameter	Value	Unit
Vpp	Electrostatic discharge MIL STD 883C - Method 3015-6	25	kV
P _{PP}	Peakpulse power (8/20µs)	500	W
T _{stg} T _j	Storage temperature range Maximum junction temperature	- 55 to + 150 125	°C ℃
ΤL	Maximum lead temperature for soldering during 10s	260	°C

ELECTRICAL CHARACTERISTICS (Tamb = 25°C)

Symbol	Parameter				
V _{RM}	Stand-off voltage				
Vbr	Breakdown voltage				
Vcl	Clamping voltage				
I _{RM}	Leakage current				
IPP	Peak pulse current				
ατ	Voltage temperature coefficient				
С	Capacitance				
Rd	Dynamic resistance				



Types	Vbr	@	I _R	I _{RM} @	Vrm	Rd	αΤ	С
	min.	max.		max.		typ.	max.	typ.
	note1		note1		note 2	note 3	0V bias	
	V	V	mA	μA	V	Ω	10 ⁻⁴ /°C	pF
ESDA25DB3	25	30	1	2	24	0.5	9.7	50

 $\begin{array}{l} \textbf{note 1}: Betwenn any I/O pin Groung\\ \textbf{note 2}: Square pulse, Ipp = 25A, tp=2.5 \mu s.\\ \textbf{note 3}: \ \Delta \ V_{BR} = \alpha T^* (Tamb - 25^\circ C)^* \ V_{BR} (25^\circ C) \end{array}$



CALCULATION OF THE CLAMPING VOLTAGE

USE OF THE DYNAMIC RESISTANCE

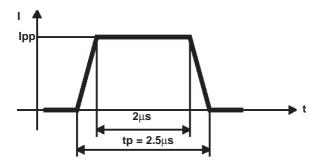
The ESDA family has been designed to clamp fast spikes like ESD. Generally the PCB designers need to calculate easily the clamping voltage V_{CL} . This is why we give the dynamic resistance in addition to the classical parameters. The voltage across the protection cell can be calculated with the following formula:

 $V_{CL} = V_{BR} + Rd I_{PP}$

Where Ipp is the peak current through the ESDA cell.

DYNAMIC RESISTANCE MEASUREMENT

The short duration of the ESD has led us to prefer a more adapted test wave, as below defined, to the classical $8/20\mu s$ and $10/1000\mu s$ surges.



2.5µs duration measurement wave.

As the value of the dynamic resistance remains stable for a surge duration lower than 20µs, the 2.5µs rectangular surge is well adapted. In addition both rise and fall times are optimized to avoid any parasitic phenomenon during the measurement of Rd.



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Fig. 1: Peak power dissipation versus initial junction tempearature.

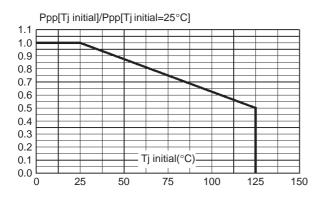


Fig. 3 : Clamping voltage versus peak pulse current (Tj initial = 25 °C). Rectangular waveform tp = $2.5 \,\mu$ s.

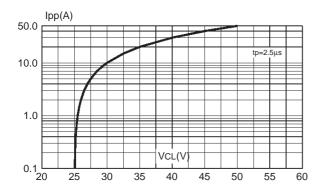
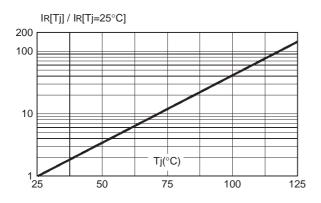
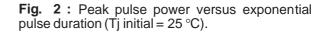


Fig. 5 : Relative variation of leakage current versus junction temperature (typical values).





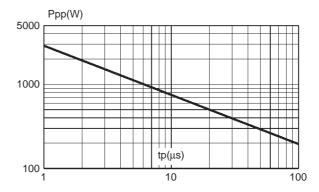
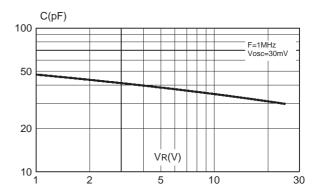
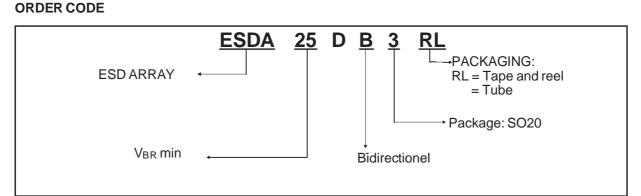


Fig. 4 : Capacitance versus reverse applied voltage (typical values).



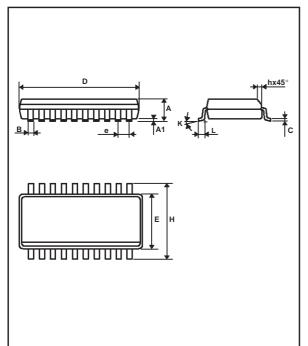
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MARKING : Logo, Date Code, E25DB3

PACKAGE MECHANICAL DATA

SO20 Plastic



	DIMENSIONS							
REF.	Millimetres			Inches				
	Min.	Тур.	Max.	Min.	Тур.	Max.		
Α			2.65			0.104		
A1	0.10		0.20	0.004		0.008		
В	0.33		0.51	0.013		0.020		
С	0.23		0.32	0.009		0.013		
D	12.6		13.0	0.484		0.512		
E	7.40		7.60	0.291		0.299		
е		1.27			0.050			
н	10.0		10.65	0.394		0.419		
h		0.50			0.020			
L	0.50		1.27	0.020		0.050		
К	8° (max)							

Packaging : Preferred packaging is tape and reel. **Weight :** 0.55g.

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