ESDA6V1-4F1

QUAD TRANSIL™ ARRAY FOR ESD PROTECTION

A.S.D.™

APPLICATIONS

Where transient overvoltage protection in ESD sensitive equipment is required, such as :

- Computers
- Printers
- Communication systems
- GSM handsets and accessories
- Other telephone sets
- Set top boxes

DESCRIPTION

The ESDA6V1-4F1 is a 4-bit wide monolithic suppressor designed to protect against ESD components which are connected to data and transmission lines.

It clamps the voltage just above the logic level supply for positive transients, and to a diode forward voltage drop below ground for negative transients.

FEATURES

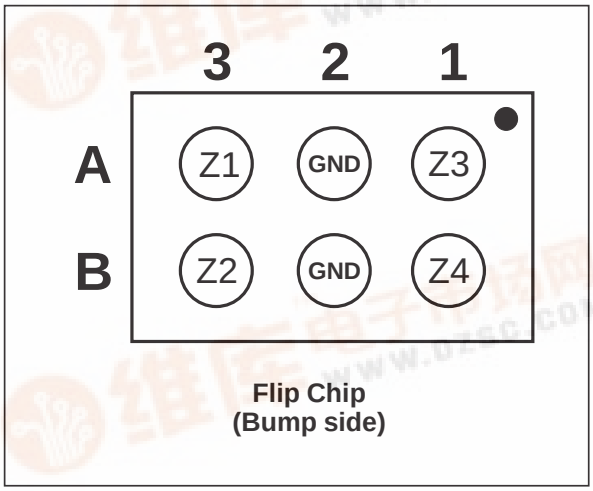
- 4 Unirectional transil functions
- Breakdown voltage: V_{BR} = 6.1Vmin
- Low leakage current < 10 µA
- Very low PCB space consuming

BENEFITS

- > ± 15kV ESD Protection
- High integration
- Suitable for high density boards

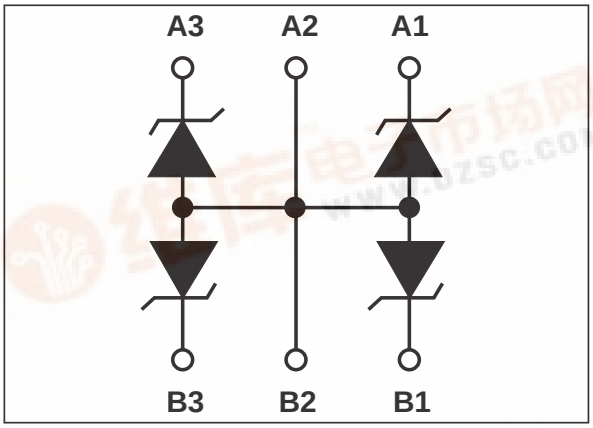
COMPLIES WITH THE FOLLOWING STANDARDS:

- IEC61000-4-2: Level 4
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883E-Method 3015-6: class3
  (Human body model)

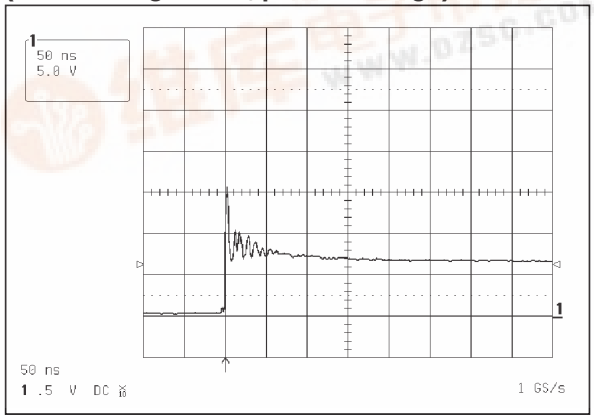


Flip Chip
(Bump side)

FUNCTIONAL DIAGRAM



ESD RESPONSE TO IEC61000-4-2 (air discharge 16kV, positive surge)

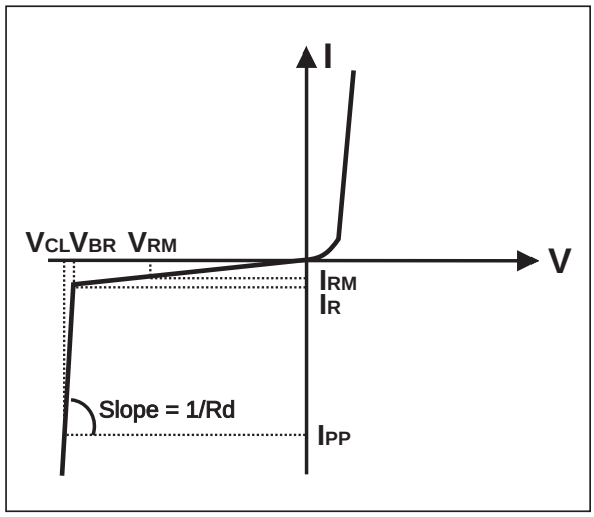


ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25°C)

Symbol	Test conditions	Value	Unit
V_{PP}	ESD discharge - MIL STD 883E - Method 3015-6 IEC61000-4-2 air discharge IEC61000-4-2 contact discharge	±25 ±15 ± 8	kV
P_{PP}	Peak pulse power (8/20µs)	150	W
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature range	-55 to +150	°C
T_L	Lead solder temperature (10 seconds duration)	260	°C
T_{op}	Operating temperature range	-40 to +85	°C

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current
I_{PP}	Peak pulse current
αT	Voltage temperature coefficient
C	Capacitance per line
Rd	Dynamic impedance
V_F	Forward voltage drop



Type	V_{BR} @ I_R			I_{RM} @ V_{RM}		Rd	αT	C
	min.	max.		max.		typ. note 1	max note 2	max 0V bias
	V	V	mA	µA	V	mΩ	10^{-4}/°C	pF
ESDA6V1- 4F1	6.1	7.2	1	10	5	350	6	250

Note 1: Square pulse I_{PP} = 15A, tp = 2.5µs

Note 2: $\Delta V_{BR} = \alpha T * (T_{amb} - 25) * V_{BR}(25°C)$

Fig. 1: Peak power dissipation versus initial junction temperature

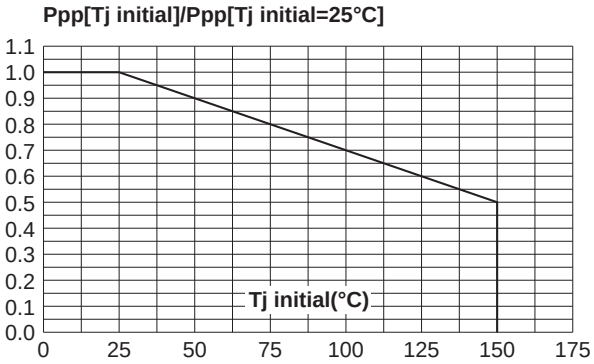


Fig. 2: Peak pulse power versus exponential pulse duration (Tj initial = 25°C)

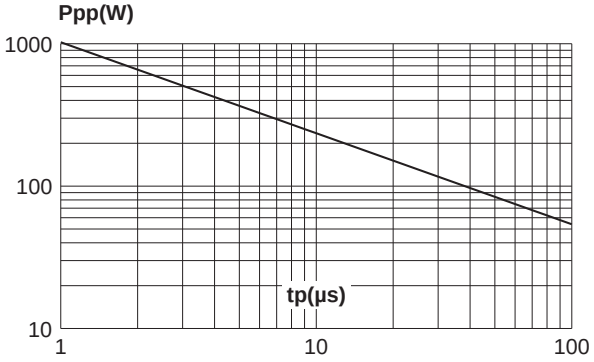


Fig. 3: Clamping voltage versus peak pulse current (Tj initial = 25°C). Rectangular waveform t_P = 2.5µs.

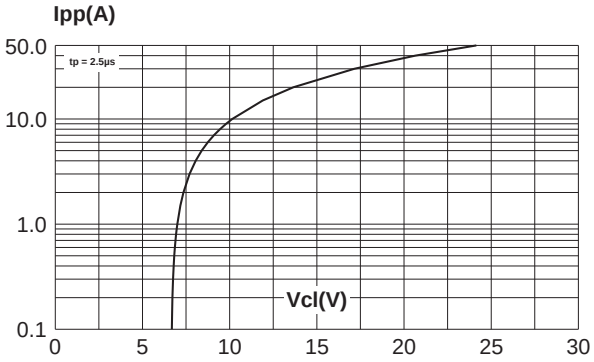


Fig. 4: Capacitance versus reverse applied voltage (typical values).

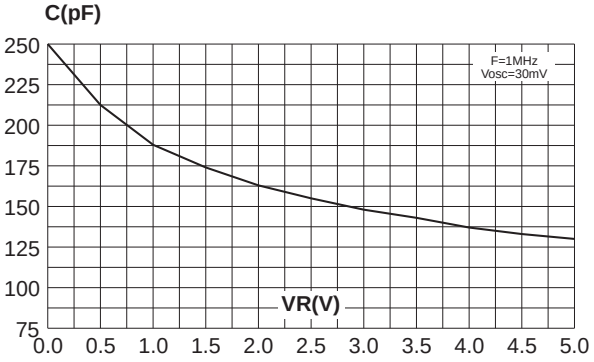
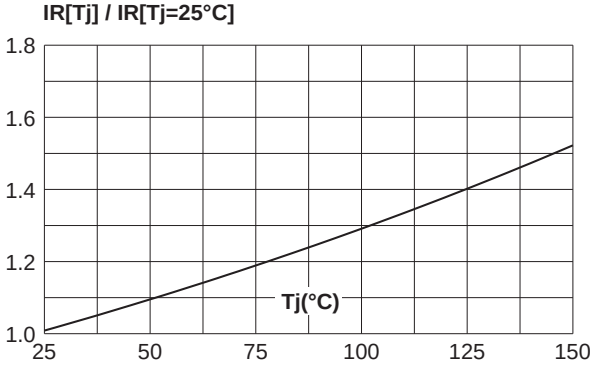


Fig. 5: Relative variation of leakage current versus junction temperature (typical values).



CALCULATION OF THE CLAMPING VOLTAGE

USE OF THE DYNAMIC RESISTANCE

The ESDA6V1-4F1 has been designed to clamp fast spikes like ESD. Generally the PCB designers need to calculate easily the clamping voltage V_{CL}. This is why we give the dynamic resistance in addition to the classical parameters.

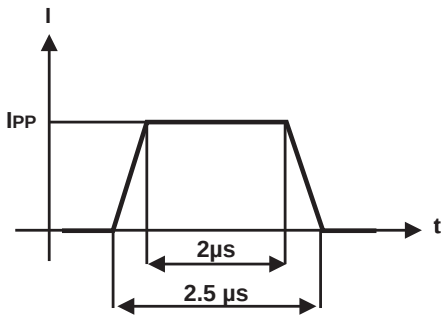
The voltage across the protection cell can be calculated with the following formula:

$$V_{CL} = V_{BR} + R_d \cdot I_{PP}$$

Where I_{PP} is the peak current through the ESDA cell.

DYNAMIC RESISTANCE MEASUREMENT

The short duration of the ESD has led us to prefer a more adapted test wave, as below defined, to the classical 8/20 µs and 10/1000 µs surges



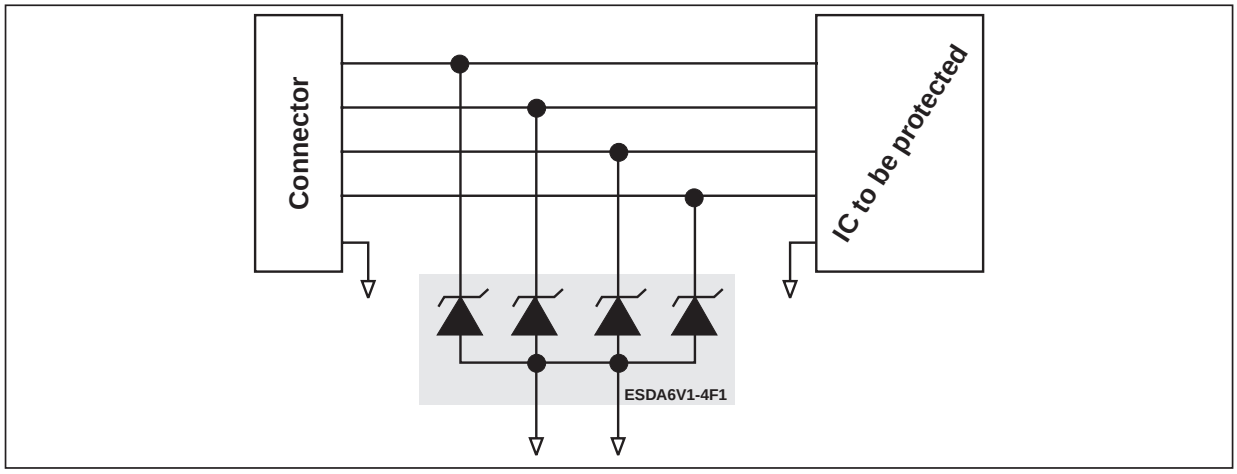
2.5 µs duration measurement wave

As the value of the dynamic resistance remains stable for a surge duration lower than 20µs, the 2.5µs rectangular surge is well adapted. In addition both rise and fall times are optimised to avoid any parasitic phenomenon during the measurement of Rd.

ESD PROTECTION WITH ESDA6V1-4F1

With the focus of lowering the operation levels, the problem of malfunction caused by the environment is critical. Electrostatic discharge (ESD) is a major cause of failure in electronic system.

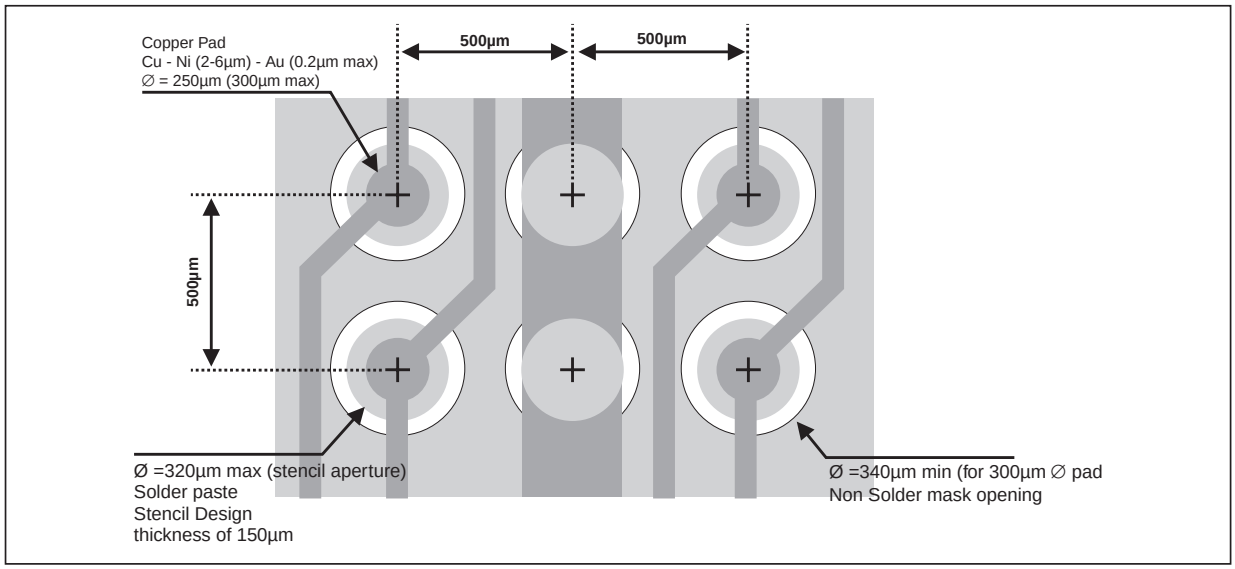
Transient Voltage Suppressors are an ideal choice for ESD protection and have proven capable in suppressing ESD events. They are capable of clamping the incoming transient to a low enough level such that damage to the protected semiconductor is prevented. Surface mount TVS arrays offer the best choice for minimal lead inductance. They serve as parallel protection elements, connected between the signal line to ground. As the transient rises above the operating voltage of the device, the TVS array becomes a low impedance path diverting the transient current to ground.



The ESDA6V1-4F1 array is the ideal product for use as board level protection of ESD sensitive semiconductor components.

The Flip Chip package makes the ESDA6V1-4F1 device some of the smallest ESD protection devices available. It also allows design flexibility in the design of “crowded” boards where the space saving is at a premium. This enables to shorten the routing and can contribute to improved ESD performance.

LAYOUT RECOMMENDATIONS

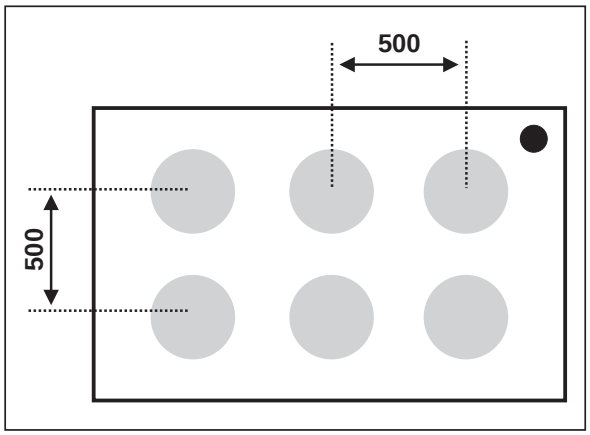


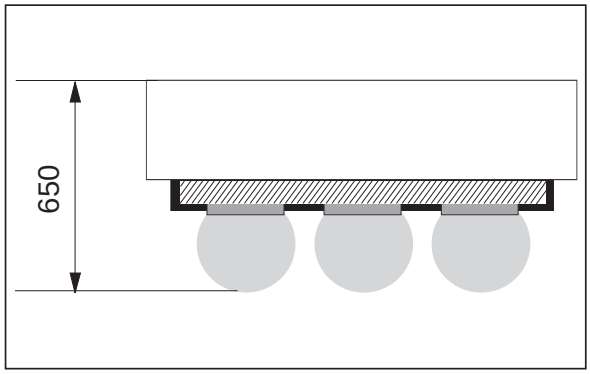
Circuit board layout is a critical design step in the suppression of ESD induced transients. The following guidelines are recommended :

- The ESDA6V1-4F1 should be placed as close as possible to the input terminals or connectors.
- Minimise the path length between the ESD suppressor and the protected device
- Minimise all conductive loops, including power and ground loops
- The ESD transient return path to ground should be kept as short as possible.
- Use ground planes whenever possible.

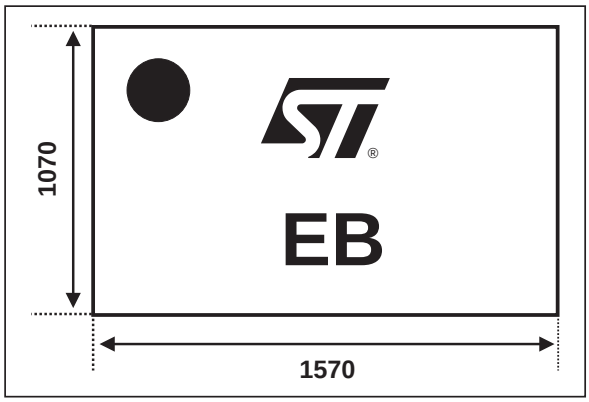
PACKAGE MECHANICAL DATA

Flip Chip (all dimensions in µm)





MARKING



Die size: (1570 ± 50) x (1070 ± 50)
Die height (including bumps): 650 ± 40
Bump diameter: 315 ± 50
Pitch: 500 ± 50

MARKING

Type	Marking	Delivery mode	Order Code	Base qty
ESDA6V1-4F1	EB	Tape & reel	ESDA6V1-4F1	5000

Note: For PCB design, assembly recommendations and packing information please refer to Application note AN1235. (“Flip-Chip: Package Description and recommendations for use”)