19-1907; Rev 1; 11/03

MAXIM

# Fault-Protected, Low-Voltage, Quad SPST Analog Switches



## General Description

The MAX4711/MAX4712/MAX4713 are fault-protected, Rail-to-Rail®, low-voltage analog switches featuring low on-resistance and guaranteed on-resistance flatness over the specified signal range. Due to the fault protection feature the analog switch input (NO_ or NC_) and output (COM_) pins are not symmetrical. The fault protection feature allows for the analog input to go beyond the plus or minus supplies without the device drawing excessive amounts of current from the analog inputs. When the analog inputs are driven beyond the supply rails when the switch is on, it will sense a fault and turn itself off and the analog switch output will be clamped to the same polarity supply as the input signal and will not go beyond the supply rails. This feature protects any electronic circuitry connected to the output from excessive voltages present on the analog inputs.

The MAX4711/MAX4712/MAX4713 are quad, single-pole/single-throw (SPST) analog switches. The MAX4711 has four normally closed switches (NC), the MAX4712 has four normally open switches (NO), and the MAX4713 has two NO and two NC switches. Switching times are less than 125ns for $t_{ON}$, and less than 80ns for $t_{OFF}$. These switches operate from a single +2.7V to +11V supply or from dual ±2.7V to ±5.5V supplies. All digital inputs have +0.8V to +2.4V logic thresholds, ensuring both TTL and CMOS logic compatibility when using ±4.5V to ±5.5V or single +4.5V to +11V supplies.

## Applications

Communication Systems
Battery-Operated Systems
Signal Routing
Test Equipment
Data-Acquisition
Industrial and Process Control Systems
Avionics
Redundant/Backup Systems

*Pin Configurations/Functional Diagrams/Truth Tables continued at end of data sheet.*

*Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.*

## Features

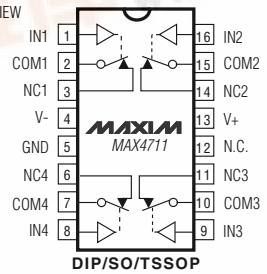
- ♦ Fault-Protected Analog Inputs
- ♦ ±12V Fault Protection with Power Off
- ♦ ±7V Fault Protection with ±5V Supplies
- ♦ +12V and -7V Fault Protection with +5V Supply
- ♦ +12V and -9V Fault Protection with +3V Supply
- ♦ Fault-Protected Digital Inputs May Exceed V+ Supply Rail
- ♦ All Switches Off with Power Off
- ♦ Rail-to-Rail Signal Handling
- ♦ Output Clamped to Appropriate Supply Voltages During Fault Condition
- ♦ 25Ω (max) $R_{ON}$ at +25°C
- ♦ 1Ω (max) On-Resistance Match Between Channels
- ♦ Single- and Dual-Supply Operation
- ♦ Pin-Compatible with Industry-Standard MAX391/MAX392/MAX393
- ♦ TTL- and CMOS-Compatible Logic Inputs

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| **MAX4711**CUE | 0°C to +70°C | 16 TSSOP |
| MAX4711CSE | 0°C to +70°C | 16 Narrow SO |
| MAX4711CPE | 0°C to +70°C | 16 Plastic Dip |
| MAX4711EUE | -40°C to +85°C | 16 TSSOP |
| MAX4711ESE | -40°C to +85°C | 16 Narrow SO |
| MAX4711EPE | -40°C to +85°C | 16 Plastic Dip |

*Ordering Information continued at end of data sheet.*

## Pin Configurations/Functional Diagrams/Truth Tables




DIP/SO/TSSOP

| MAX4711 | |
|---|---|
| LOGIC | SWITCH |
| 0 | ON |
| 1 | OFF |

N.C. = NOT CONNECTED

# Fault-Protected, Low-Voltage, Quad SPST Analog Switches

## ABSOLUTE MAXIMUM RATINGS

V+ .....-0.3V to +13V
V- .....-13V to +0.3V
V+ to V-.....-0.3V to +13V
IN_.....(V- + 12V) to (V- - 0.3V)
COM_ (Note 1).....(V- - 0.3V) to (V+ + 0.3V)
NO_, NC_ (Note 2).....(V+ - 12V) to (V- + 12V)
Continuous Current into Any Terminal.....±40mA
Peak Current, into Any Terminal
(pulsed at 1ms,10% duty cycle).....±70mA

Continuous Power Dissipation ($T_A$ = +70°C)
16-Pin TSSOP (derate 5.70mW/°C above +70°C).....457mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C).....696mW
16-Pin Plastic Dip (derate 10.53mW/°C above +70°C)...842mW
Operating Temperature Ranges
MAX471_C_ E .....0°C to +70°C
MAX471_E_ E .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

**Note 1:** COM_ pin is not fault-protected. Signals on COM_ exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

**Note 2:** NO_ and NC_ pins are fault-protected. Signals on NO_ or NC_ exceeding -12V to +12V may damage device. These limits apply with V+ = V- = 0.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, $V_{IH}$ = +2.4V, $V_{IL}$ = +0.8V, GND = 0, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | $T_A$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| Fault-Free Analog Signal Range | $V_{COM\_}$, $V_{NO\_}$, $V_{NO\_}$ | Applies with power on | C, E | V- | | V+ | V |
| On-Resistance | $R_{ON}$ | V+ = +4.5V, V- = -4.5V, $V_{NO\_}$, $V_{NC\_}$ = ±3.5V, $I_{OUT}$ = 10mA | +25°C | | 16 | 25 | Ω |
| | | | C, E | | | 30 | |
| On-Resistance Match Between Channels (Note 4) | $\Delta R_{ON}$ | V+ = +4.5V, V- = -4.5V, $V_{NO\_}$, $V_{NC\_}$ = ±3.5V, $I_{OUT}$ = 10mA | +25°C | | 0.2 | 1 | Ω |
| | | | C, E | | | 2 | |
| On-Resistance Flatness | $R_{FLAT}$ | V+ = +4.5V, V- = -4.5V, $V_{NO\_}$, $V_{NC\_}$ = ±3.5V, $I_{OUT}$ = 10mA | +25°C | | 1.3 | 4 | Ω |
| | | | C, E | | | 5 | |
| NO_, NC_ Off-Leakage Current (Note 5) | $I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$ | V+ = +5.5V, V- = -5.5V, $V_{COM\_}$ = ±4.5V, $V_{NO\_}$, $V_{NC\_}$ = 4.5V | +25°C | -0.5 | | +0.5 | nA |
| | | | C, E | -10 | | +10 | |
| COM_ Off-Leakage Current (Note 5) | $I_{COM\_(OFF)}$ | V+ = +5.5V, V- = -5.5V, $V_{COM\_}$ = ±4.5V, $V_{NO\_}$, $V_{NC\_}$ = 4.5V | +25°C | -0.5 | | +0.5 | nA |
| | | | C, E | -10 | | +10 | |
| COM_ On-Leakage Current (Note 5) | $I_{COM\_(ON)}$ | V+ = +5.5V, V- = -5.5V, $V_{COM\_}$ = ±4.5V, $V_{NO\_}$, $V_{NC\_}$ = ±4.5V or floating | +25°C | -0.5 | | +0.5 | nA |
| | | | C, E | -20 | | +20 | |
| **FAULT** | | | | | | | |
| Fault-Protected Analog Signal Range | $V_{NO\_}$, $V_{NC\_}$ | Applies with power on | C, E | -12 + V+ | | +12 + V- | V |
| Fault-Protected Analog Signal Range | $V_{NO\_}$, $V_{NC\_}$ | Applies with power off | C, E | -12 | | +12 | V |
| COM_ Output-Leakage Current, Supplies ON (Note 5) | $I_{COM}$ | All channels off, V+ = +5V, V- = -5V, $V_{NO\_}$, $V_{NC\_}$ = ±7V | +25°C | -50 | | +50 | nA |
| | | | C, E | -500 | | +500 | |

## ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, $V_{IH}$ = +2.4V, $V_{IL}$ = +0.8V, GND = 0, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | $T_A$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| NO_ or NC_ Off-Leakage Current, Supplies ON (Note 5) | $I_{NO\_}$, $I_{NC\_}$ | V+ = +5V, V- = -5V, $V_{NO\_}$, $V_{NC\_}$ = ±7V | +25°C | -50 | | +50 | nA |
| | | | C, E | -500 | | +500 | |
| NO_ or NC_ Input-Leakage Current, Supplies OFF (Note 5) | $I_{NO\_}$, $I_{NC\_}$ | $V_{NO\_}$, $V_{NC\_}$ = ±12V, V± = 0 | +25°C | -0.5 | | +0.5 | µA |
| | | | C, E | -5 | | +5 | |
| Output Clamp Current | $I_{COM\_}$ | $V_{NO\_}$, $V_{NC\_}$ = +7V, V+ = +5V, V- = -5V | C, E | 9 | 20 | 33 | mA |
| | | $V_{NO\_}$, $V_{NC\_}$ = -7V V+ = +5V, V- = -5V | | -33 | -16 | -9 | |
| Output Clamp Resistance | $R_{CLAMP\_}$ | $V_{NO\_}$, $V_{NC\_}$ = ±7V | +25°C | | 200 | | Ω |
| Fault Trip Threshold | | | +25°C | V- - 0.4V | | V+ + 0.4V | V |
| ±Fault Output Turn-On Delay Time | | $V_{NO\_}$, $V_{NC\_}$ = ±7V, $R_{COM}$ = 1kΩ | +25°C | | 200 | | ns |
| ±Fault Recovery Time | | $V_{NO\_}$, $V_{NC\_}$ = ±7V, $R_{COM}$ = 1kΩ | +25°C | | 700 | | ns |
| **LOGIC INPUT** | | | | | | | |
| Input Logic High | $V_{IH}$ | | C, E | 2.4 | | | V |
| Input Logic Low | $V_{IL}$ | | C, E | | | 0.8 | V |
| Input-Leakage Current (Note 5) | $I_{IN}$ | $V_{IN\_}$ = 0 or V+ | +25°C | -1 | | +1 | µA |
| | | | C, E | -5 | | +5 | |
| **SWITCH DYNAMICS** | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{NO\_}$ or $V_{NC\_}$ = ±3V, $R_L$ = 300Ω, $C_L$ = 35pF, Figure 2 | +25°C | | 80 | 125 | ns |
| | | | C, E | | | 150 | |
| Turn-Off Time | $t_{OFF}$ | $V_{NO\_}$ or $V_{NC\_}$ = ±3V, $R_L$ = 300Ω, $C_L$ = 35pF, Figure 2 | +25°C | | 50 | 80 | ns |
| | | | C, E | | | 100 | |
| Break-Before-Make Time Delay (MAX4713 only) | $t_{BBM}$ | $V_{NO\_}$ or $V_{NC\_}$ = ±3V, $R_L$ = 300Ω, $C_L$ = 35pF, Figure 2 | +25°C | 15 | 30 | | ns |
| | | | C, E | 5 | | | |
| Charge Injection | Q | $V_{GEN}$ = 0, $R_{GEN}$ = 0, $C_L$ = 1nF, Figure 4 | +25°C | | 25 | | pC |
| NO_ or NC_ Off-Capacitance | $C_{N\_(OFF)}$ | f = 1MHz, Figure 5 | +25°C | | 8 | | pF |
| COM_ Off-Capacitance | $C_{COM\_(OFF)}$ | f = 1MHz, Figure 5 | +25°C | | 8 | | pF |
| COM_ On-Capacitance | $C_{COM\_(ON)}$ | f = 1MHz, Figure 5 | +25°C | | 30 | | pF |
| Off-Isolation (Note 6) | $V_{ISO}$ | $R_L$ = 50Ω, $C_L$ = 15pF, $P_{IN}$ = 0, f = 1MHz, Figure 6 | +25°C | | -59 | | dB |
| Channel-to-Channel Crosstalk (Note 7) | $V_{CT}$ | $R_L$ = 50Ω, $C_L$ = 15pF, $P_{IN}$ = 0, f = 1MHz, Figure 6 | +25°C | | -87 | | dB |

# Fault-Protected, Low-Voltage, Quad SPST Analog Switches

## ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, $V_{IH}$ = +2.4V, $V_{IL}$ = +0.8V, GND = 0, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | $T_A$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | |
| Power-Supply Range | V+, V- | | C, E | ±2.7 | | ±5.5 | V |
| V+ Supply Current | I+ | All $V_{IN\_}$ = 0 or V+ | +25°C | | 38 | 75 | µA |
| | | | C, E | | | 100 | |
| V- Supply Current | I- | All $V_{IN\_}$ = 0 or V+ | +25°C | | 38 | 75 | µA |
| | | | C, E | | | 100 | |
| GND Supply Current | $I_{GND}$ | All $V_{IN\_}$ = 0 or V+ | +25°C | | 0 | 1 | µA |
| | | | C, E | | | 10 | |

## ELECTRICAL CHARACTERISTICS—+5V Single Supply

(V+ = +4.5V to +5.5V, V- = 0, $V_{IH}$ = +2.4V, $V_{IL}$ = +0.8V, GND = 0, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | $T_A$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| Fault-Free Analog Signal Range | $V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$ | Power on | C, E | V- | | V+ | V |
| On-Resistance | $R_{ON}$ | V+ = +4.5V, $V_{NO\_}$, $V_{NC\_}$ = +3.5V, $I_{OUT}$ = 10mA | +25°C | | 30 | 40 | Ω |
| | | | C, E | | | 50 | |
| On-Resistance Match Between Channels (Note 4) | $\Delta R_{ON}$ | V+ = +4.5V, $V_{NO\_}$, $V_{NC\_}$ = +3.5V, $I_{OUT}$ = 10mA | +25°C | | 0.3 | 2 | Ω |
| | | | C, E | | | 3 | |
| On-Resistance Flatness | $R_{FLAT}$ | V+ = +4.5V, $V_{NO\_}$, $V_{NC\_}$ = +1.5V, +2.25V, +3.5V, $I_{OUT}$ = 10mA | +25°C | | 2 | 5 | Ω |
| | | | C, E | | | 6 | |
| NO_, NC_ Off-Leakage Current (Note 5) | $I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$ | V+ = +5.5V, $V_{COM\_}$ = +1V, +4.5V; $V_{NO\_}$, $V_{NC\_}$ = +4.5V, +1V | +25°C | -0.5 | | +0.5 | nA |
| | | | C, E | -10 | | +10 | |
| COM_ Off-Leakage Current (Note 5) | $I_{COM\_(OFF)}$ | V+ = +5.5V, $V_{COM\_}$ = +1V, +4.5V; $V_{NO\_}$, $V_{NC\_}$ = +4.5V, +1V | +25°C | -0.5 | | +0.5 | nA |
| | | | C, E | -10 | | +10 | |
| COM_ On-Leakage Current (Note 5) | $I_{COM\_(ON)}$ | V+ = +5.5V, $V_{COM\_}$ = +1V, +4.5V; $V_{NO\_}$, $V_{NC\_}$ = +1V, +4.5V, or floating | +25°C | -0.5 | | +0.5 | nA |
| | | | C, E | -20 | | +20 | |
| **FAULT** | | | | | | | |
| Fault-Protected Analog Signal Range | $V_{NO\_}$, $V_{NC\_}$ | Power on | C, E | -12 + V+ | | +12 | V |

## ELECTRICAL CHARACTERISTICS—+5V Single Supply (continued)

(V+ = +4.5V to +5.5V, V- = 0, $V_{IH}$ = +2.4V, $V_{IL}$ = +0.8V, GND = 0, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | $T_A$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Fault-Protected Analog Signal Range | $V_{NO\_}$, $V_{NC\_}$ | Power off | C, E | -12 | | +12 | V |
| COM_ Output-Leakage Current, Supplies ON (Note 5) | $I_{COM\_}$ | All channels off; $V_{NO\_}$, $V_{NC\_}$ = +12V or -7V, V+ = +5V | +25°C | -50 | | +50 | nA |
| | | | C, E | -500 | | +500 | |
| NO_ or NC_ Off-Leakage Current, Supplies ON (Note 5) | $I_{NO\_}$, $I_{NC\_}$ | $V_{NO\_}$, $V_{NC\_}$ = +12V or -7V, V+ = +5V | +25°C | -50 | | +50 | nA |
| | | | C, E | -500 | | +500 | |
| NO_ or NC_ Input-Leakage Current, Supplies OFF (Note 5) | $I_{NO\_}$, $I_{NC\_}$ | $V_{NO\_}$, $V_{NC\_}$ = ±12V, V± = 0 | +25°C | -0.5 | | +0.5 | µA |
| | | | C, E | -5 | | +5 | |
| Output Clamp Current | $I_{COM\_}$ | $V_{NO\_}$, $V_{NC\_}$ = +12V, V+ = 5V | C, E | 2 | 6 | 11 | mA |
| Output Clamp Resistance | $R_{CLAMP\_}$ | Clamp on | +25°C | | 500 | | Ω |
| +Fault Output Turn-On Delay Time | | $V_{NO\_}$, $V_{NC\_}$ = +12V, $R_L$ = 300Ω, V+ = +5V | +25°C | | 200 | | ns |
| +Fault Recovery Time | | $V_{NO\_}$, $V_{NC\_}$ = +12V, $R_L$ = 300Ω, V+ = +5V | +25°C | | 500 | | µs |
| **LOGIC INPUT** | | | | | | | |
| Input Logic High | $V_{IH}$ | | C, E | 2.4 | | | V |
| Input Logic Low | $V_{IL}$ | | C, E | | | 0.8 | V |
| Input-Leakage Current (Note 5) | $I_{IN}$ | $V_{IN\_}$ = 0 or V+ | C, E | -1 | | +1 | µA |
| **SWITCH DYNAMICS** | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{NO\_}$ or $V_{NC\_}$ = +3V, $R_L$ = 300Ω, $C_L$ = 35pF, Figure 2 | +25°C | | 170 | 230 | ns |
| | | | C, E | | | 275 | |
| Turn-Off Time | $t_{OFF}$ | $V_{NO\_}$ or $V_{NC\_}$ = +3V, $R_L$ = 300Ω, $C_L$ = 35pF, Figure 2 | +25°C | | 55 | 100 | ns |
| | | | C, E | | | 125 | |
| Break-Before-Make Time Delay (MAX4713 only) | $t_{BBM}$ | $V_{NO\_}$ or $V_{NC\_}$ = +3V, $R_L$ = 300Ω, $C_L$ = 35pF, Figure 2 | +25°C | 30 | 115 | | ns |
| | | | C, E | 20 | | | |
| Charge Injection | Q | $V_{GEN}$= 0, $R_{GEN}$ = 0, $C_L$ = 1nF, Figure 4 | +25°C | | -1 | | pC |
| **POWER SUPPLY** | | | | | | | |
| Power-Supply Range | V+ | | C, E | 2.7 | | 11 | V |
| V+ Supply Current | I+ | All $V_{IN\_}$ = 0 or V+ | +25°C | | 34 | 65 | µA |
| | | | C, E | | | 75 | |

# Fault-Protected, Low-Voltage, Quad SPST Analog Switches

## ELECTRICAL CHARACTERISTICS—+3V Single Supply

(V+ = +2.7V to +3.6V, V- = 0, $V_{IH}$ = +2.0V, $V_{IL}$ = +0.6V, GND = 0, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | $T_A$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| Fault-Free Analog Signal Range | $V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$ | Power-on | C, E | V- | | V+ | V |
| On-Resistance | $R_{ON}$ | V+ = +2.7V, $V_{NO\_}$, $V_{NC\_}$ = +1V, $I_{OUT}$ = 1mA | +25°C | | 54 | 75 | Ω |
| | | | C, E | | | 100 | |
| On-Resistance Match Between Channels (Note 4) | $\Delta R_{ON}$ | V+ = +2.7V, $V_{NO\_}$, $V_{NC\_}$ = +1V, $I_{OUT}$ = 1mA | +25°C | | 1 | 7 | Ω |
| | | | C, E | | | 9 | |
| NO_, NC_ Off-Leakage Current (Note 5) | $I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$ | V+ = +3.6V, $V_{COM\_}$ = +0.7V, +3V; $V_{NO\_}$, $V_{NC\_}$ = +3V, +0.7V | +25°C | -0.5 | | +0.5 | nA |
| | | | C, E | -10 | | +10 | |
| COM_ Off-Leakage Current (Note 5) | $I_{COM\_(OFF)}$ | V+ = +3.6V, $V_{COM\_}$ = +0.7V, +3V; $V_{NO\_}$, $V_{NC\_}$ = +3V, +0.7V | +25°C | -0.5 | | +0.5 | nA |
| | | | C, E | -10 | | +10 | |
| COM_ On-Leakage Current (Note 5) | $I_{COM\_(ON)}$ | V+ = +3.6V, $V_{COM\_}$ = +0.7, +3V; $V_{NO\_}$, $V_{NC\_}$ = +0.7V,+3V, or floating | +25°C | -0.5 | | +0.5 | nA |
| | | | C, E | -20 | | +20 | |
| **FAULT** | | | | | | | |
| Fault-Protected Analog Signal Range | $V_{NO\_}$, $V_{NC\_}$ | Power-on | C, E | -12 + V+ | | +12 | V |
| Fault-Protected Analog Signal Range | $V_{NO\_}$, $V_{NC\_}$ | Power-off | C, E | -12 | | +12 | V |
| COM_ Output-Leakage Current, Supplies ON (Note 5) | $I_{COM}$ | All channels off; $V_{NO\_}$, $V_{NC\_}$ = +12V or -9V, V+ = +3V | +25°C | -50 | | +50 | nA |
| | | | C, E | -500 | | +500 | |
| NO_ or NC_ Off-Leakage Current, Supplies ON (Note 5) | $I_{NO\_}$, $I_{NC\_}$ | $V_{NO\_}$, $V_{NC\_}$ = +12V or -9V, V+ = +3V | +25°C | -50 | | +50 | nA |
| | | | C, E | -500 | | +500 | |
| NO_ or NC_ Input-Leakage Current, Supplies OFF (Note 5) | $I_{NO\_}$, $I_{NC\_}$ | $V_{NO\_}$, $V_{NC\_}$ = ±12V, V± = 0 | +25°C | -0.5 | | +0.5 | µA |
| | | | C, E | -5 | | +5 | |
| Output Clamp Current | $I_{COM\_}$ | $V_{NO\_}$, $V_{NC\_}$ = +12V, V+ = +3V | C, E | 0.5 | | 3.0 | mA |
| Output Clamp Resistance | $R_{CLAMP\_}$ | V+ = +3V, $V_{NO\_}$, $V_{NC\_}$ = +12V; clamp on | +25°C | | 600 | | kΩ |
| +Fault Output Turn-On Delay Time | | $V_{NO\_}$, $V_{NC\_}$ = +12V, $R_L$ = 300Ω, V+ = +3V | +25°C | | 200 | | ns |
| +Fault Recovery Time | | $V_{NO\_}$, $V_{NC\_}$ = +12V, $R_L$ = 300Ω, V+ = +3V | +25°C | | 2.2 | | µs |

## ELECTRICAL CHARACTERISTICS—+3V Single Supply (continued)

(V+ = +2.7V to +3.6V, V- = 0, $V_{IH}$ = +2.0V, $V_{IL}$ = +0.6V, GND = 0, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | $T_A$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **LOGIC INPUT** | | | | | | | |
| Input Logic High | $V_{IH}$ | | C, E | 2 | | | V |
| Input Logic Low | $V_{IL}$ | | C, E | | | 0.6 | V |
| Input-Leakage Current (Note 5) | $I_{IN\_}$ | $V_{IN\_}$ = 0 or V+ | C, E | -5 | | +5 | µA |
| **SWITCH DYNAMICS** | | | | | | | |
| Turn-On Time | $t_{ON}$ | V+ = +2.7V, $V_{NO\_}$ or $V_{NC\_}$ = +1.5V, $R_L$ = 300Ω, $C_L$ = 35pF, Figure 2 | +25°C | | 340 | 500 | ns |
| | | | C, E | | | 600 | |
| Turn-Off Time | $t_{OFF}$ | V+ = +2.7V, $V_{NO\_}$ or $V_{NC\_}$ = +1.5V, $R_L$ = 300Ω, $C_L$ = 35pF, Figure 2 | +25°C | | 100 | 175 | ns |
| | | | C, E | | | 225 | |
| Break-Before-Make Time Delay (MAX4713 only) | $t_{BBM}$ | V+ = +2.7V, $V_{NO\_}$ or $V_{NC\_}$ = +1.5V, $R_L$ = 300Ω, $C_L$ = 35pF, Figure 2 | +25°C | 60 | 240 | | ns |
| | | | C, E | 50 | | | |
| **POWER SUPPLY** | | | | | | | |
| Power-Supply Range | V+ | | C, E | 2.7 | | 11 | V |
| V+ Supply Current | I+ | All $V_{IN\_}$ = 0 or V+ | +25°C | | 8 | 15 | µA |
| | | | C, E | | | 20 | |

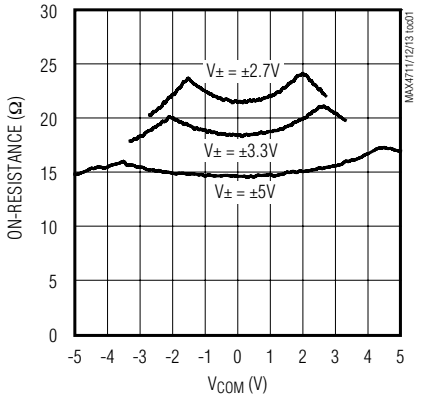
**Note 3:** Algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
**Note 4:** $\Delta R_{ON} = \Delta R_{ON}(MAX) - \Delta R_{ON}(MIN)$
**Note 5:** Leakage parameters are 100% tested at maximum-rated temperature and with dual supplies. Leakage parameters are guaranteed by correlation at +25°C.
**Note 6:** Off-isolation = 20 $\log_{10}$ [$V_{COM\_}$/($V_{NO\_}$ or $V_{NC\_}$)], $V_{COM\_}$ = output, $V_{NO\_}$ or $V_{NC\_}$ = input to off switch.
**Note 7:** Between any two switches.

# Fault-Protected, Low-Voltage, Quad SPST Analog Switches

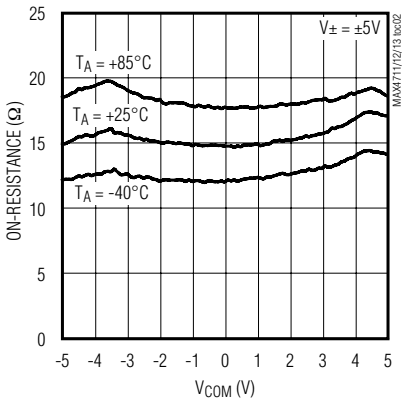
## Typical Operating Characteristics

(V+ = +5V, V- = -5V, $T_A$ = +25°C, unless otherwise noted.)

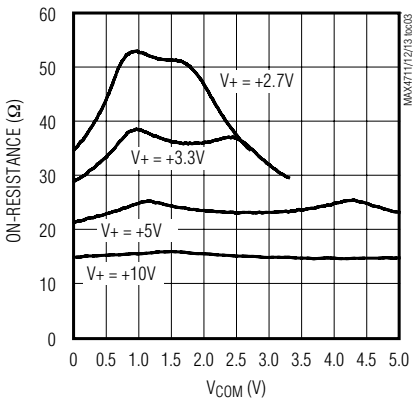
**ON-RESISTANCE vs. $V_{COM}$ (DUAL SUPPLIES)**



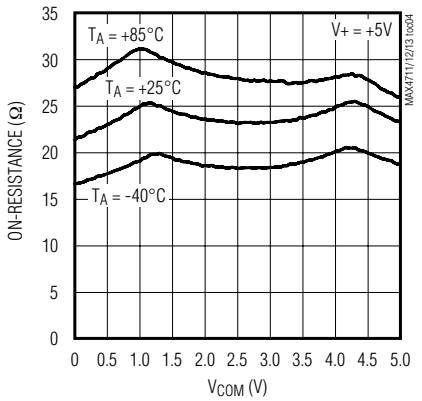

**ON-RESISTANCE vs. $V_{COM}$ AND TEMPERATURE (DUAL SUPPLIES)**



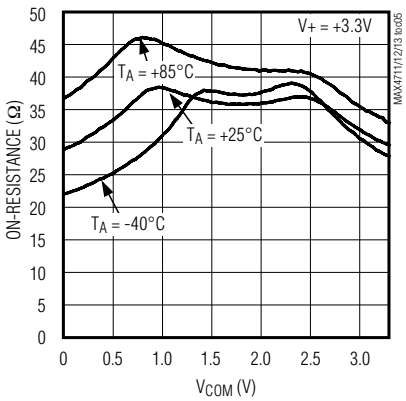

**ON-RESISTANCE vs. $V_{COM}$ (SINGLE SUPPLY)**



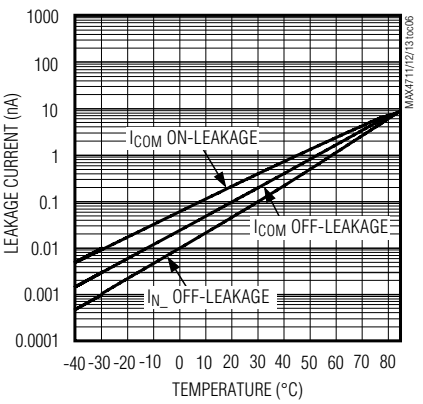

**ON-RESISTANCE vs. $V_{COM}$ AND TEMPERATURE (SINGLE SUPPLY)**



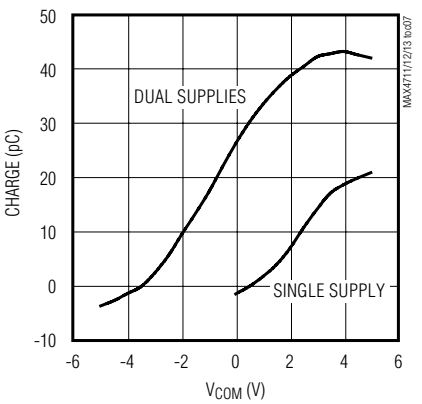

**ON-RESISTANCE vs. $V_{COM}$ AND TEMPERATURE (SINGLE SUPPLY)**



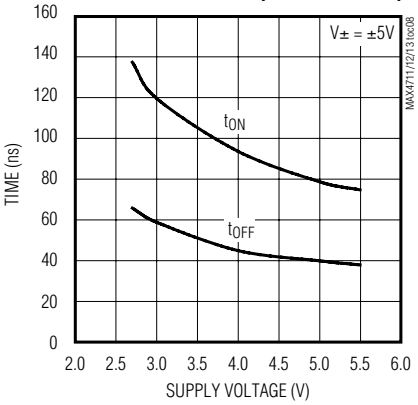

**ON/OFF-LEAKAGE CURRENT vs. TEMPERATURE**



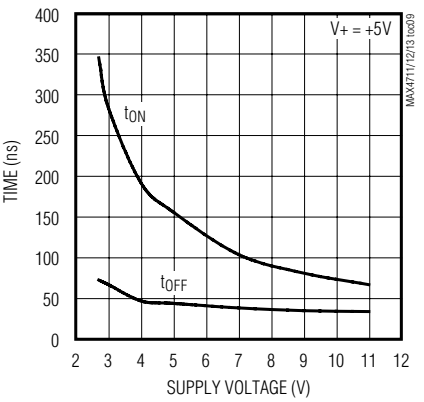

**CHARGE INJECTION vs. $V_{COM}$**




**TURN-ON/TURN-OFF TIME vs. SUPPLY VOLTAGE (DUAL SUPPLIES)**




**TURN-ON/TURN-OFF TIME vs. SUPPLY VOLTAGE (SINGLE SUPPLY)**

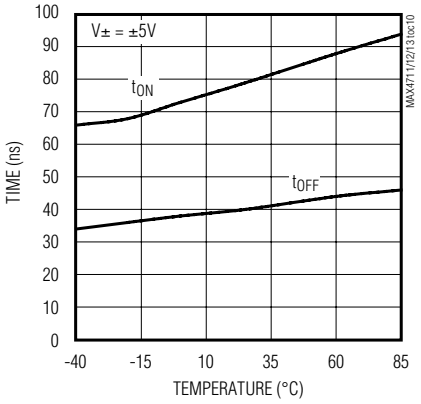


# Fault-Protected, Low-Voltage, Quad SPST Analog Switches

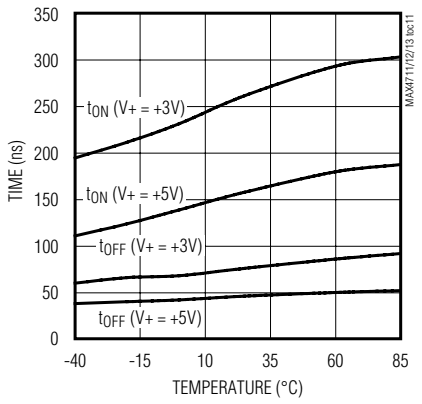
## Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, $T_A$ = +25°C, unless otherwise noted.)

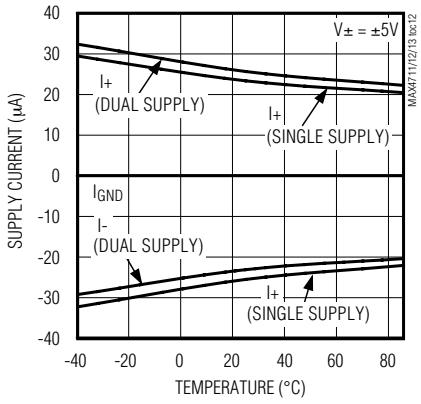
**TURN-ON/TURN-OFF TIME vs. TEMPERATURE (DUAL SUPPLIES)**



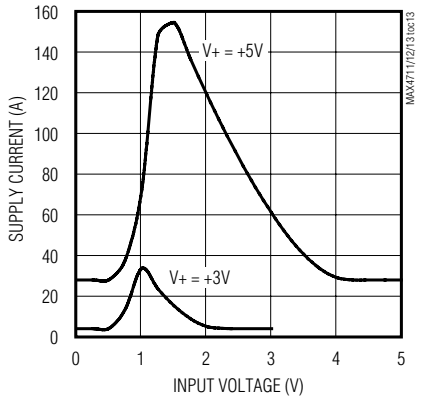

**TURN-ON/TURN-OFF TIME vs. TEMPERATURE (SINGLE SUPPLY)**



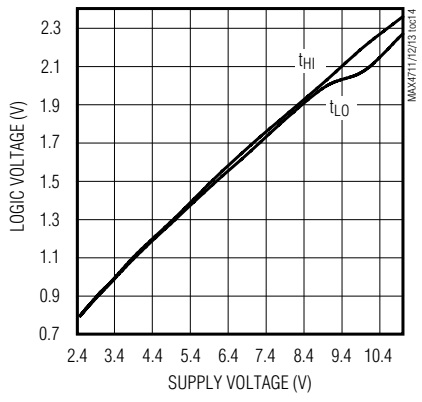

**SUPPLY CURRENT vs. TEMPERATURE $V_{IN}$ = 0 OR 5V**



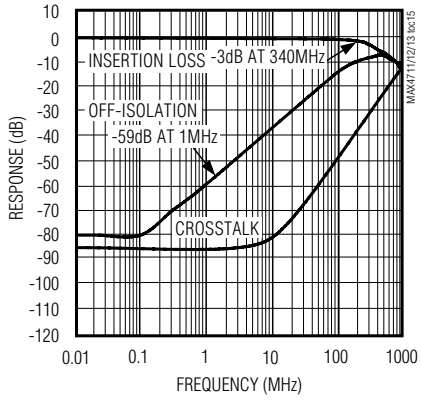

**SUPPLY CURRENT vs. INPUT VOLTAGE**



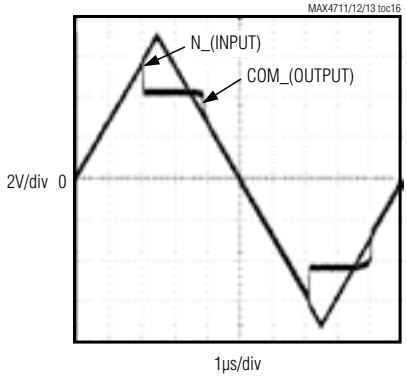

**LOGIC LEVEL THRESHOLD vs. SUPPLY VOLTAGE**



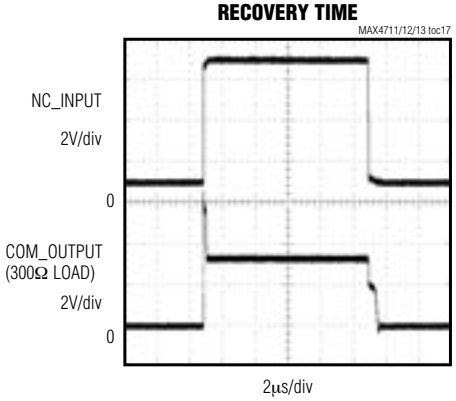

**FREQUENCY RESPONSE**




**FAULT TURN-ON DELAY AND RECOVERY TIME**




**FAULT TURN-ON DELAY AND RECOVERY TIME**



# Fault-Protected, Low-Voltage, Quad SPST Analog Switches

## Pin Description

| PIN | | | NAME | FUNCTION |
|---|---|---|---|---|
| MAX4711 | MAX4712 | MAX4713 | | |
| 1, 16, 9, 8 | 1, 16, 9, 8 | 1, 16, 9, 8 | IN1, IN2, IN3, IN4 | Logic Inputs. Fault-protected to (V- + 12V). |
| 2, 15, 10, 7 | 2, 15, 10, 7 | 2, 15, 10, 7 | COM1, COM2, COM3, COM4 | Analog Switch Common Terminals |
| 3, 14, 11, 6 | — | — | NC1, NC2, NC3, NC4 | Fault-Protected Analog Switch Normally Closed Terminals |
| — | 3, 14, 11, 6 | — | NO1, NO2, NO3, NO4 | Fault-Protected Analog Switch Normally Open Terminals |
| — | — | 3, 6 | NO1, NO4 | Fault-Protected Analog Switch Normally Open Terminals |
| — | — | 14, 11 | NC2, NC3 | Fault-Protected Analog Switch Normally Closed Terminals |
| 4 | 4 | 4 | V- | Negative Supply Voltage Input. Connect to GND for single-supply operation. |
| 5 | 5 | 5 | GND | Ground |
| 12 | 12 | 12 | N.C. | No Connection. Not internally connected. |
| 13 | 13 | 13 | V+ | Positive Supply Input |

## Detailed Description

The MAX4711/MAX4712/MAX4713 differ considerably from traditional fault-protection switches, with several advantages. First, they are constructed with two parallel FET's allowing very low on-resistance. Second, they allow signals on the NC_ or NO_ pins that are within or slightly beyond the supply rails to be passed through the switch to the COM terminal, allowing rail-to-rail signal operation. Third, when a signal on NC_ or NO_ exceeds the supply rails by about 150mV (a fault condition) the voltage on COM_ is limited to the same polarity supply voltage. Operation is identical for both fault polarities.

During a fault condition, the NO_ or NC_ input becomes high impedance regardless of the switch state or load resistance. If the switch is on, the COM_ output current is supplied from V+ or V- by the clamp FET's that are connected from COM to each supply. These FET's can typically source or sink up to 15mA. When power is removed, the fault protection is still in effect. In this case, the NO_ or NC_ terminals are a virtual open circuit. The fault can be up to ±12V.

The COM_ pins are not fault-protected, they act as normal CMOS switch terminals. If a voltage source is connected to any COM_ pin, it should be limited to the supply voltages. Exceeding the supply voltage will cause high currents to flow through the ESD-protected diodes, possibly damaging the device (see *Absolute Maximum Ratings*).

### Pin Compatibility

These switches have identical pinouts to common non-fault-protected CMOS switches. Care should be exercised while considering them for direct replacements in existing printed circuit boards since only the NO_ and NC_ pins of each switch are fault-protected.

### Internal Construction

Internal construction is shown in Figure 1, with the analog signal paths shown in bold. A single NO switch is shown; the NC configuration is identical except the logic-level translator is inverting. The analog switch is formed by the parallel combination of N-channel FET (N1) and P-channel FET (P1), which are driven on and off simultaneously according to the input fault condition and the logic-level state.

### Normal Operation

Two comparators continuously compare the voltage on the NO_ (or NC_) pin with V+ and V-. When the signal on NO_ or NC_ is between V+ and V- the switch acts normally, with FETs N1 and P1 turning on and off in response to IN_ signals. The parallel combination of N1 and P1 forms a low-value resistor between NO_ (or

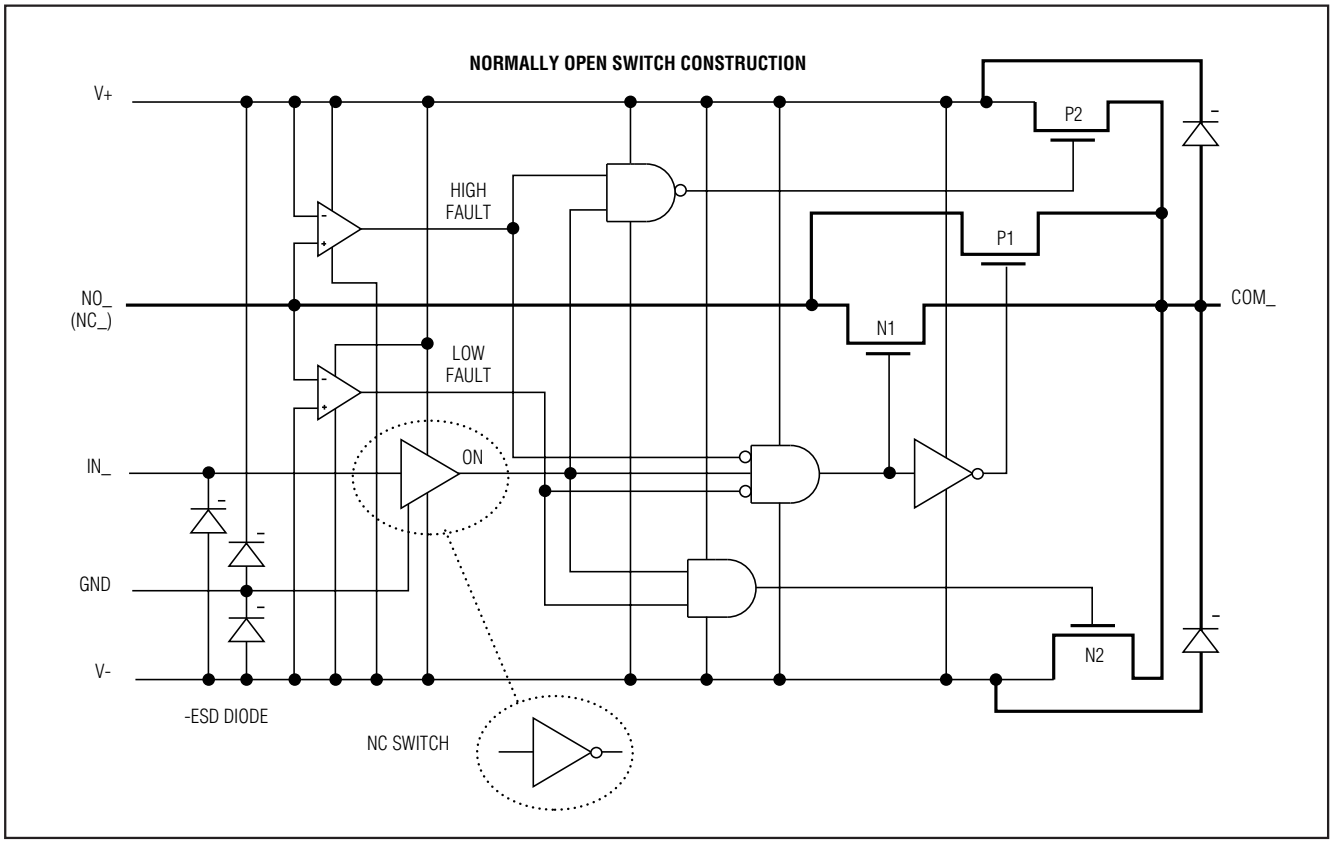



*Figure 1. Block Diagram*

NC_) and COM_ so that signals pass equally well in either direction.

### Positive Fault Condition

When the signal on NO_ (or NC_) exceeds V+ by about 150mV, the high-fault comparator output is high, turning off FETs N1 and P1. This makes the NO_ (or NC_) input high impedance regardless of the switch state. If the switch state is "off", all FETs are turned off and both NO_ (or NC_) and COM_ are high impedance. If the switch state is "on", clamp FET P2 is turned on, sourcing current from V+ to COM_.

### Negative Fault Condition

When the signal on NO_ (or NC_) exceeds V- by about 150mV, the low-fault comparator output is high, turning off FETs N1 and P1. This makes the NO_ (or NC_) input high impedance regardless of the switch state. If the switch state is "off", all FETs are turned off and both NO_ (or NC_) and COM_ are high impedance. If the switch state is "on", clamp FET N2 is turned on, sinking current from COM_ to V-.

### Transient Fault Response and Recovery

When a fast rise-time or fall-time transient on NC_ or NO_ exceeds V+ or V-, the output (COM_) follows the input to the supply rail with only a few nanoseconds delay. This delay is due to the switch on-resistance and circuit capacitance to ground. When the input transient returns to within the supply rails, however, there is a 700ns output recovery delay time. These values depend on the COM_ output resistance and capacitance, and are not production tested or guaranteed. The delays are not dependent on the fault amplitude. Higher COM_ output resistance and capacitance increase recovery times.

### COM_ and IN_ Pins

FETs N2 and P2 can source about ±15mA from V+ or V- to COM_ in the fault condition. Ensure that if the COM_ pin is connected to a low-resistance load, the absolute maximum current rating of 40mA is never exceeded both in normal and fault conditions.

# Fault-Protected, Low-Voltage, Quad SPST Analog Switches

The COM_ pins do not have fault protection. Reverse ESD-protection diodes are internally connected between COM_, and V+ and V-. If a signal on COM_ exceeds V+ or V- by more than a diode drop, one of these diodes will conduct. The IN_ pin can exceed the positive supply voltage, but they can go below the negative supply by only a diode drop. The maximum voltage on these pins is 12V if operating from a single supply, regardless of the supply voltage (including 0 volts), and if operating from dual supplies, the maximum voltage is (V- + 12V).

### Fault-Protection Voltage and Power Off

The maximum fault voltage on the NC_ or NO_ pins is ±12V with power off.

### IN_ Logic-Level Thresholds

The logic-level thresholds are CMOS and TTL compatible when using ±4.5V to ±5.5V or single +4.5V to +11V supplies. When using a +2.7V supply, the logic thresholds are $V_{IH}$ = 2.0V and $V_{IL}$ = 0.6V.

### Dual Supplies

The MAX4711/MAX4712/MAX4713 operate with bipolar supplies between ±2.7V and ±5.5V. The V+ and V- supplies need not be symmetrical, but their difference should not exceed 11V.

### Single Supply

The MAX4711/MAX4712/MAX4713 operate from a single supply between +2.7V and +11V when V- is connected to GND.

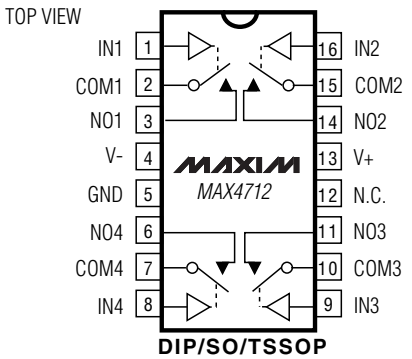
## Chip Information

TRANSISTOR COUNT: 463

## Ordering Information (continued)

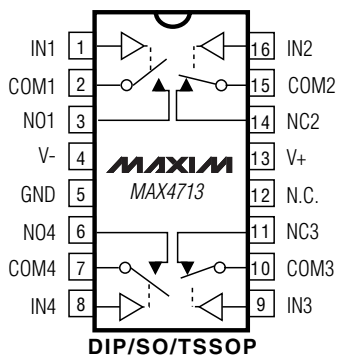
| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| **MAX4712**CUE | 0°C to +70°C | 16 TSSOP |
| MAX4712CSE | 0°C to +70°C | 16 Narrow SO |
| MAX4712CPE | 0°C to +70°C | 16 Plastic Dip |
| MAX4712EUE | -40°C to +85°C | 16 TSSOP |
| MAX4712ESE | -40°C to +85°C | 16 Narrow SO |
| MAX4712EPE | -40°C to +85°C | 16 Plastic Dip |
| **MAX4713**CUE | 0°C to +70°C | 16 TSSOP |
| MAX4713CSE | 0°C to +70°C | 16 Narrow SO |
| MAX4713CPE | 0°C to +70°C | 16 Plastic Dip |
| MAX4713EUE | -40°C to +85°C | 16 TSSOP |
| MAX4713ESE | -40°C to +85°C | 16 Narrow SO |
| MAX4713EPE | -40°C to +85°C | 16 Plastic Dip |

## Pin Configurations/Functional Diagrams/Truth Tables (continued)




DIP/SO/TSSOP

| MAX4712 | |
|---|---|
| LOGIC | SWITCH |
| 0 | OFF |
| 1 | ON |

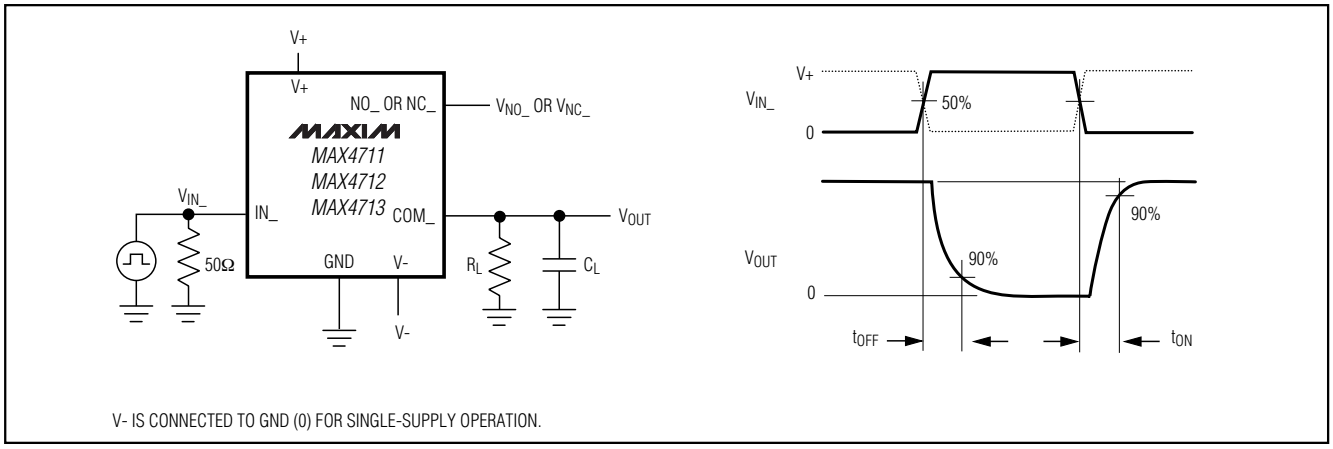



DIP/SO/TSSOP

| MAX4713 | | |
|---|---|---|
| LOGIC | SWITCHES 1, 4 | SWITCHES 2, 3 |
| 0 | OFF | ON |
| 1 | ON | OFF |

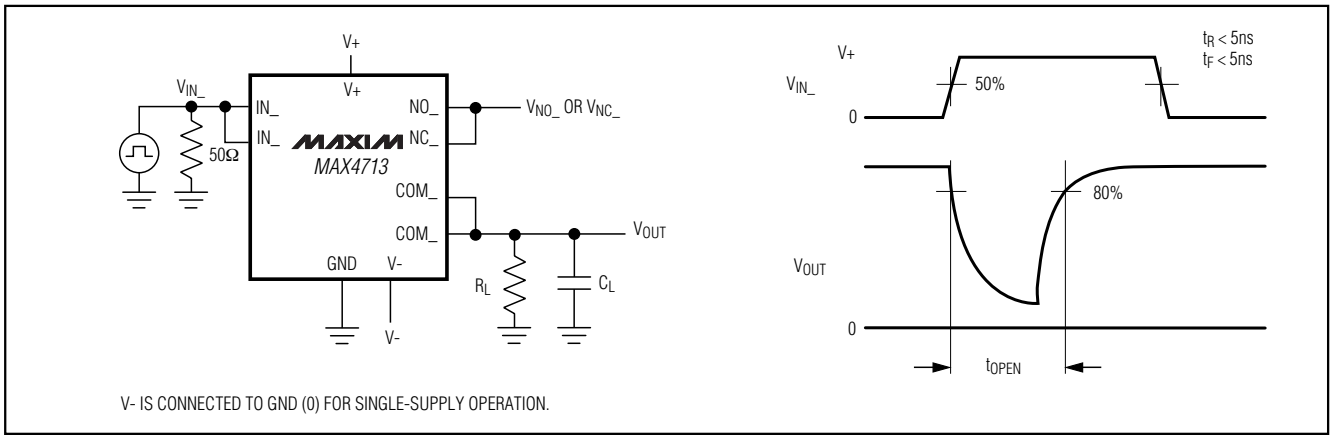
SWITCHES SHOWN FOR LOGIC "0" INPUT

## Test Circuits/Timing Diagrams



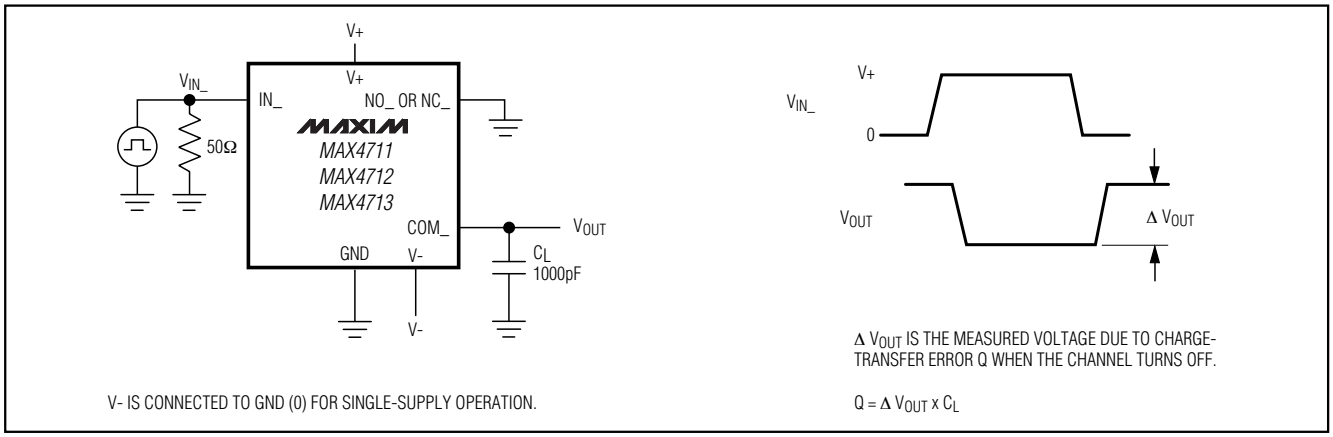

V- IS CONNECTED TO GND (0) FOR SINGLE-SUPPLY OPERATION.

*Figure 2. Switch Turn-On/Turn-Off Times*




V- IS CONNECTED TO GND (0) FOR SINGLE-SUPPLY OPERATION.

*Figure 3. MAX4713 Break-Before-Make Interval*




Δ $V_{OUT}$ IS THE MEASURED VOLTAGE DUE TO CHARGE-TRANSFER ERROR Q WHEN THE CHANNEL TURNS OFF.

V- IS CONNECTED TO GND (0) FOR SINGLE-SUPPLY OPERATION.

$Q = \Delta V_{OUT} \times C_L$

*Figure 4. Charge Injection*

# Fault-Protected, Low-Voltage, Quad SPST Analog Switches

## Test Circuits/Timing Diagrams (continued)

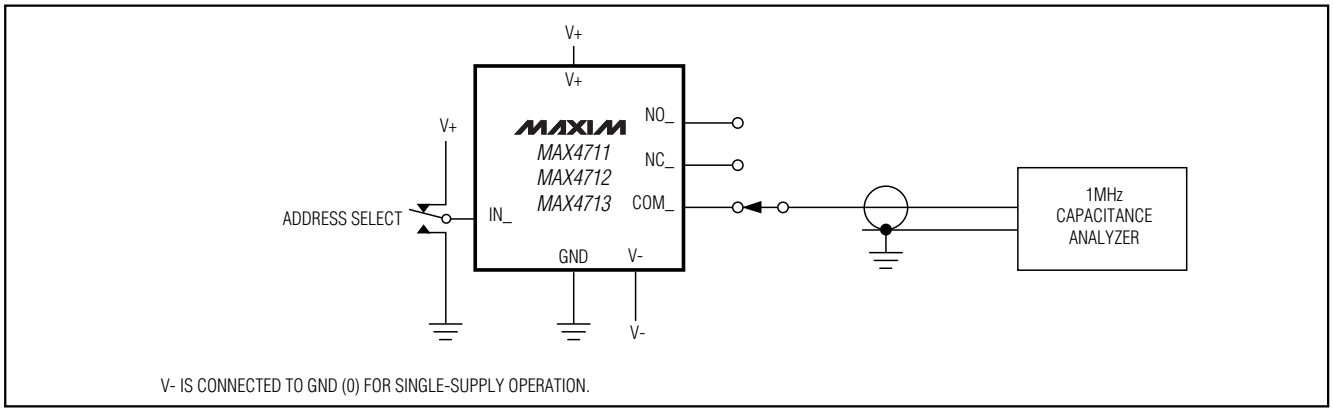



*Figure 5. COM_, NO_, NC_ Capacitance*

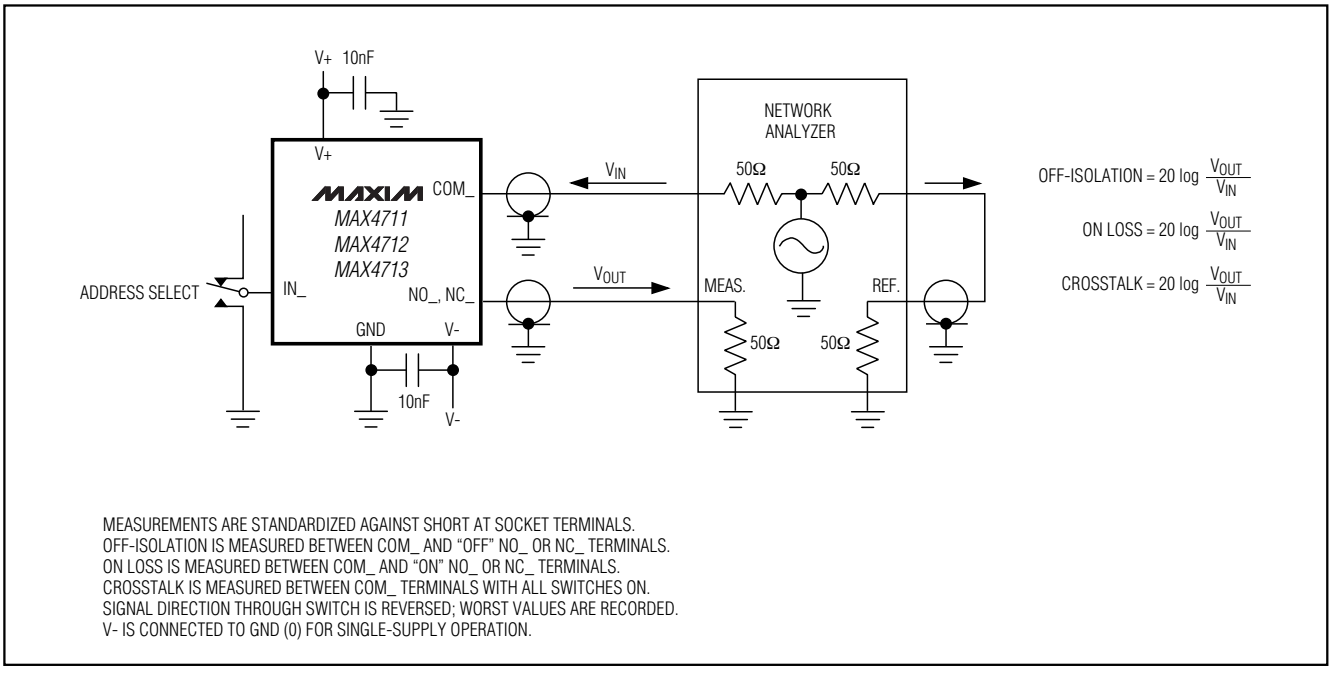


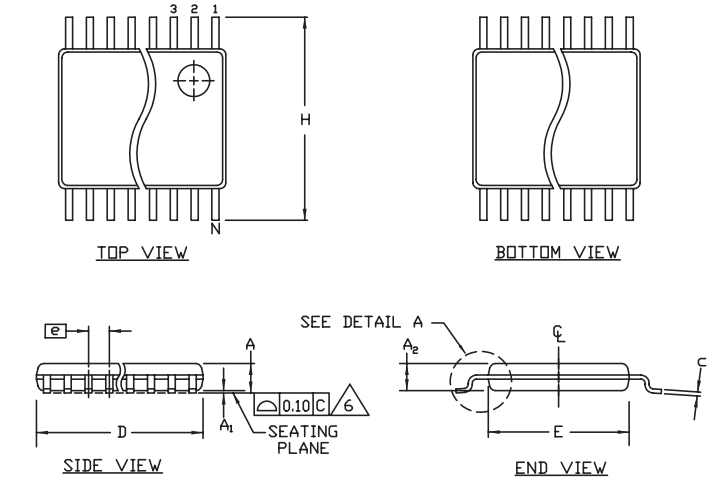

*Figure 6. Frequency Response, Off-Isolation, and Crosstalk*

# Fault-Protected, Low-Voltage, Quad SPST Analog Switches

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS




| SYMBOL | COMMON DIMENSIONS | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | —— | 1.10 | | .043 |
| $A_1$ | 0.05 | 0.15 | .002 | .006 |
| $A_2$ | 0.85 | 0.95 | .033 | .037 |
| b | 0.19 | 0.30 | .007 | .012 |
| $b_1$ | 0.19 | 0.25 | .007 | .010 |
| c | 0.09 | 0.20 | .004 | .008 |
| $c_1$ | 0.09 | 0.14 | .004 | .006 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 4.30 | 4.50 | .169 | .177 |
| e | 0.65 BSC | | .026 BSC | |
| H | 6.25 | 6.55 | .246 | .258 |
| L | 0.50 | 0.70 | .020 | .028 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |

| JEDEC | | | VARIATIONS | | | |
|---|---|---|---|---|---|---|
| MO-153 | N | | MILLIMETERS | | INCHES | |
| | | | MIN. | MAX. | MIN. | MAX. |
| AB-1 | 14 | D | 4.90 | 5.10 | .193 | .201 |
| AB | 16 | D | 4.90 | 5.10 | .193 | .201 |
| AC | 20 | D | 6.40 | 6.60 | .252 | .260 |
| AD | 24 | D | 7.70 | 7.90 | .303 | .311 |
| AE | 28 | D | 9.60 | 9.80 | .378 | .386 |

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0066 | F | 1/1 |

# Fault-Protected, Low-Voltage, Quad SPST Analog Switches

## Package Information (continued)

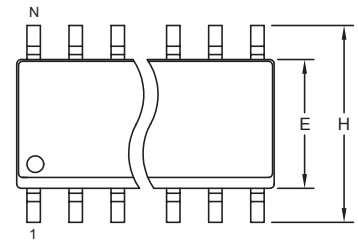
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOICN .EPS

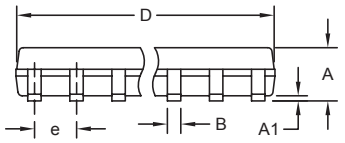
| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| e | 0.050 BSC | | 1.27 BSC | |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

VARIATIONS:

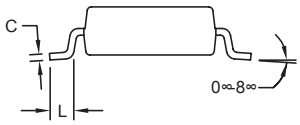
| | INCHES | | MILLIMETERS | | | |
|---|---|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX | N | MS012 |
| D | 0.189 | 0.197 | 4.80 | 5.00 | 8 | AA |
| D | 0.337 | 0.344 | 8.55 | 8.75 | 14 | AB |
| D | 0.386 | 0.394 | 9.80 | 10.00 | 16 | AC |




TOP VIEW




FRONT VIEW




SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

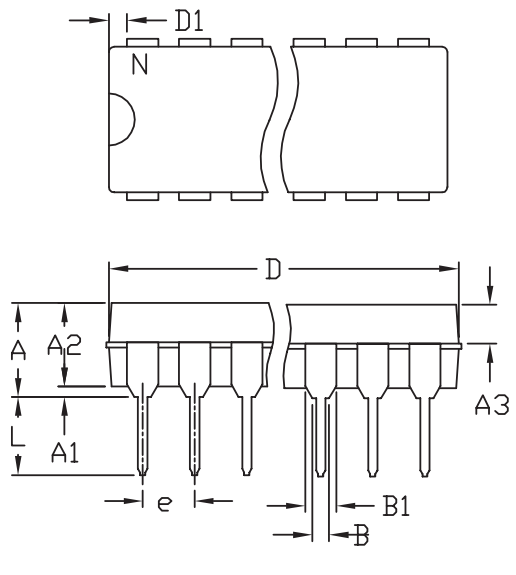
TITLE: PACKAGE OUTLINE, .150" SOIC

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0041 | B | 1/1 |

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

PDIPN.EPS




| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | --- | 0.180 | --- | 4.572 |
| A1 | 0.015 | --- | 0.38 | --- |
| A2 | 0.125 | 0.175 | 3.18 | 4.45 |
| A3 | 0.055 | 0.080 | 1.40 | 2.03 |
| B | 0.015 | 0.022 | 0.381 | 0.56 |
| B1 | 0.045 | 0.065 | 1.14 | 1.65 |
| C | 0.008 | 0.014 | 0.2 | 0.355 |
| D1 | 0.005 | 0.080 | 0.13 | 2.03 |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E1 | 0.240 | 0.310 | 6.10 | 7.87 |
| e | 0.100 BSC. | | 2.54 BSC. | |
| eA | 0.300 BSC. | | 7.62 BSC. | |
| eB | 0.400 BSC. | | 10.16 BSC. | |
| L | 0.115 | 0.150 | 2.921 | 3.81 |

| | INCHES | | MILLIMETERS | | | |
|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | N | MS001 |
| D | 0.348 | 0.390 | 8.84 | 9.91 | 8 | AB |
| D | 0.735 | 0.765 | 18.67 | 19.43 | 14 | AC |
| D | 0.745 | 0.765 | 18.92 | 19.43 | 16 | AA |
| D | 0.885 | 0.915 | 22.48 | 23.24 | 18 | AD |
| D | 1.015 | 1.045 | 25.78 | 26.54 | 20 | AE |
| D | 1.14 | 1.265 | 28.96 | 32.13 | 24 | AF |
| D | 1.360 | 1.380 | 34.54 | 35.05 | 28 | *5 |

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

TITLE: PACKAGE FAMILY OUTLINE: PDIP .300"

1/1

DOCUMENT CONTROL NUMBER: 21-0043 D REV