19-0157; Rev 1; 1/94

MAXIM

Single/Dual, Ultra-Fast, Low-Power, Precision TTL Comparators

MAX912/MAX913

General Description

The MAX913 single and MAX912 dual high-speed, low-power comparators have differential inputs and complementary TTL outputs. Fast propagation delay (10ns typ), extremely low supply current, and a wide common-mode input range that includes the negative rail make the MAX912/MAX913 ideal for low-power, high-speed, single +5V (or ±5V) applications such as V/F converters or switching regulators.

The MAX912/MAX913 outputs remain stable through the linear region. This feature eliminates output instability common to high-speed comparators when driven with a slow-moving input signal.

The MAX912/MAX913 can be powered from a single +5V supply or a ±5V split supply. The MAX913 is an improved plug-in replacement for the LT1016. It provides significantly wider input voltage range **and** equivalent speed at a fraction of the power. The MAX912 dual comparator has equal performance to the MAX913 and includes independent latch controls.

Applications

Zero-Crossing Detectors
Ethernet Line Receivers
Switching Regulators
High-Speed Sampling Circuits
High-Speed Triggers
Extended Range V/F Converters
Fast Pulse Width/Height Discriminators

Features

- ♦ **Ultra Fast (10ns)**
- ♦ **Single +5V or Dual ±5V Supply Operation**
- ♦ **Input Range Extends Below Negative Supply**
- ♦ **Low Power: 6mA (+5V) Per Comparator**
- ♦ **No Minimum Input Signal Slew-Rate Requirement**
- ♦ **No Power-Supply Current Spiking**
- ♦ **Stable in the Linear Region**
- ♦ **Inputs Can Exceed Either Supply**
- ♦ **Low Offset Voltage: 0.8mV**

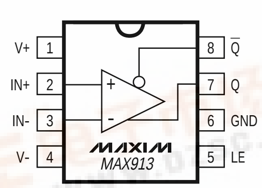
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX912CPE	0°C to +70°C	16 Plastic DIP
MAX912CSE	0°C to +70°C	16 Narrow SO
MAX912C/D	0°C to +70°C	Dice*
MAX912EPE	-40°C to +85°C	16 Plastic DIP
MAX912ESE	-40°C to +85°C	16 Narrow SO
MAX912MJE	-55°C to +125°C	16 CERDIP
MAX913CPA	0°C to +70°C	8 Plastic DIP
MAX913CSA	0°C to +70°C	8 SO
MAX913C/D	0°C to +70°C	Dice*
MAX913EPA	-40°C to +85°C	8 Plastic DIP
MAX913ESA	-40°C to +85°C	8 SO
MAX913MJA	-55°C to +125°C	8 CERDIP

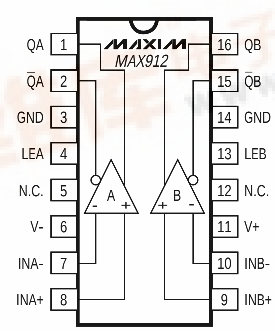
** Dice are specified at T_A = +25°C, DC parameters only.*

Pin Configurations

TOP VIEW



DIP/SO



DIP/Narrow SO

Call toll free 1-800-998-8800 for free samples or literature.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage....................7V
Negative Supply Voltage....................-7V
Differential Input Voltage....................±15V
Input Voltage (Referred to V-)....................- 0.3V to 15V
Latch Pin Voltage....................Equal to Supplies
Continuous Output Current....................±20mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C)...727mW
8-Pin SO (derate 5.88mW/°C above +70°C)....................471mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C)........640mW
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C)...842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C)...696mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C)....800mW
Operating Temperature Ranges:
MAX91_ C_ _....................0°C to +70°C
MAX91_ E_ _....................-40°C to +85°C
MAX91_ MJ_....................-55°C to +125°C
Storage Temperature Range....................-65°C to +150°C
Lead Temperature (soldering, 10sec)....................+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +5V, V- = -5V, V_Q = 1.4V, V_{LE} = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 1)	V_{OS}	$R_S \leq 100\Omega$	T_A = +25°C		0.8	2	mV
			$T_A = T_{MIN}$ to T_{MAX}			3	
Offset Drift	TCV_{OS}				2		µV/°C
Input Offset Current (Note 1)	I_{OS}		T_A = +25°C		0.3	0.5	µA
			$T_A = T_{MIN}$ to T_{MAX}			0.8	
Input Bias Current	I_B		T_A = +25°C		3	5	µA
		C, E temp. ranges				8	
		M temp. range				10	
Input Voltage Range	V_{CM}	C, E temp. ranges		-5.2		+3.5	V
		M temp. range		-5.0		+3.5	
		Single +5V	C, E temp. ranges	-0.2		+3.5	
			M temp. range	0		+3.5	
Common-Mode Rejection Ratio	CMRR	$-5.0V \leq V_{CM} \leq +3.5V$		80	110		dB
Power-Supply Rejection Ratio	PSRR	Positive supply: $4.5V \leq V+ \leq 5.5V$		60	85		dB
		Negative supply: $-2V \geq V- \geq -7V$		80	100		
Small-Signal Voltage Gain	A_V	$1V \leq V_Q \leq 2V$, T_A = +25°C		1500	3500		V/V
Output Voltage	V_{OH}	$V+ \geq 4.5V$	I_{OUT} = 1mA	2.7	3.4		V
			I_{OUT} = 10mA	2.4	3.0		
	V_{OL}	I_{SINK} = 4mA			0.3	0.5	
		T_A = +25°C, I_{SINK} = 10mA			0.4		
Positive Supply Current Per Comparator	I+	C, E temp. ranges			6	10	mA
		M temp. range				12	
Negative Supply Current Per Comparator	I-				0.4	2	mA
Latch-Pin High Input Voltage	V_{IH}			2.0			V
Latch-Pin Low Input Voltage	V_{IL}					0.8	V
Latch-Pin Current	I_{IL}	V_{LE} = 0V				-20	µA

ELECTRICAL CHARACTERISTICS (continued)

($V+ = +5V$, $V- = -5V$, $V_Q = 1.4V$, $V_{LE} = 0V$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted).

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Propagation Delay (Note 2)	t_{PD+}, t_{PD-}	$\Delta V_{IN} = 100mV$, $V_{OD} = 5mV$	$T_A = +25°C$			10	14	ns
			$T_A = T_{MIN}$ to T_{MAX}				16	
		$\Delta V_{IN} = 100mV$, $V_{OD} = 20mV$	$T_A = +25°C$			9	12	
			$T_A = T_{MIN}$ to T_{MAX}				15	
Differential Propagation Delay (Note 2)	Δt_{PD}	$\Delta V_{IN} = 100mV$, $V_{OD} = 5mV$	$T_A = +25°C$	MAX913		2	3	ns
				MAX912		3	5	
Channel-to-Channel Propagation Delay (Note 2)		$\Delta V_{IN} = 100mV$, $V_{OD} = 5mV$ (MAX912 only)	$T_A = +25°C$			500		ps
Latch Setup Time (Note 3)	t_{SU}				2	0		ns
Latch Hold Time (Note 3)	t_H				3	2		ns
Latch Propagation Delay (Note 4)	t_{LPD}					7		ns

Note 1: Input Offset Voltage (V_{OS}) is defined as the average of the two input offset voltages, measured by forcing first one output, then the other to 1.4V. Input Offset Current (I_{OS}) is defined the same way.

Note 2: Propagation Delay (t_{PD}) and Differential Propagation Delay (Δt_{PD}) cannot be measured in automatic handling equipment with low input overdrive values. The MAX912/MAX913 are sample tested to 0.1% AQL with a 1V step and 500mV overdrive at +25°C only. Correlation tests show that t_{PD} and Δt_{PD} can be guaranteed with this test, if additional DC tests are performed to guarantee that all internal bias conditions are correct. For low overdrive conditions, V_{OS} is added to the overdrive. Differential Propagation Delay is defined as: $\Delta t_{PD} = t_{PD+} - t_{PD-}$.

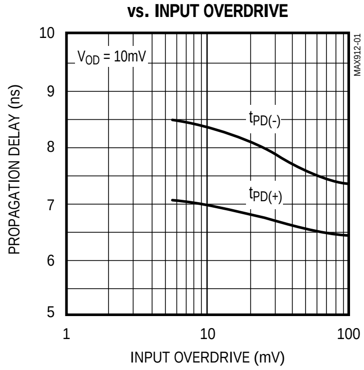
Note 3: Input latch setup time (t_{SU}) is the interval in which the input signal must be stable prior to asserting the latch signal. The hold time (t_H) is the interval after the latch is asserted in which the input signal must be stable. These parameters are guaranteed by design.

Note 4: Latch Propagation Delay (t_{LPD}) is the delay time for the output to respond when the latch-enable pin is deasserted. See Timing Diagram.

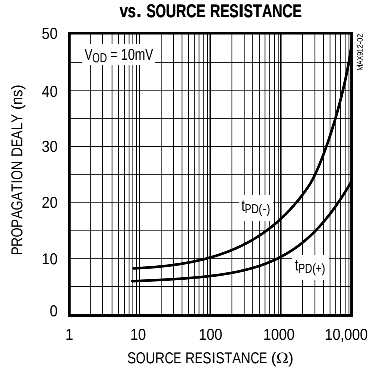
Typical Operating Characteristics

($V+ = 5V$, $V- = -5V$, $V_{LE} = 0V$, $C_L = 15pF$, $T_A = +25°C$, unless otherwise noted.)

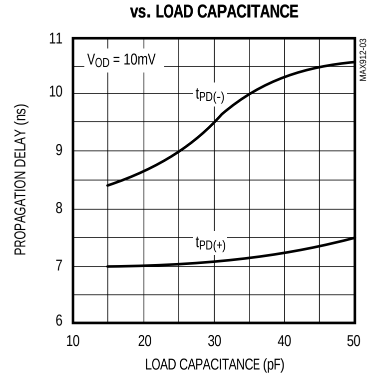
PROPAGATION DELAY vs. INPUT OVERDRIVE



PROPAGATION DELAY vs. SOURCE RESISTANCE



PROPAGATION DELAY vs. LOAD CAPACITANCE

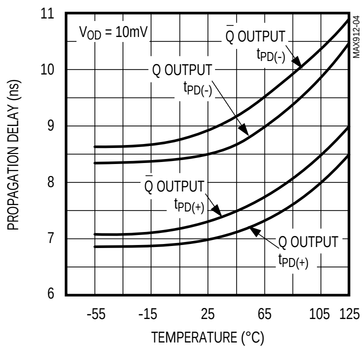


Single/Dual, Ultra-Fast, Low-Power, Precision TTL Comparators

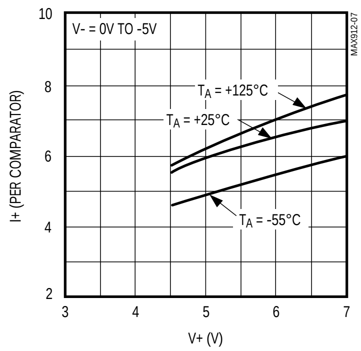
Typical Operating Characteristics (continued)

($V+ = 5V$, $V- = -5V$, $V_{LE} = 0V$, $C_L = 15pF$, $T_A = +25°C$, unless otherwise noted.)

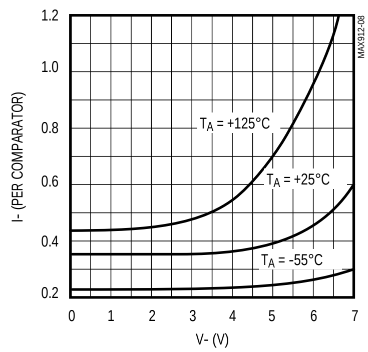
PROPAGATION DELAY vs. TEMPERATURE



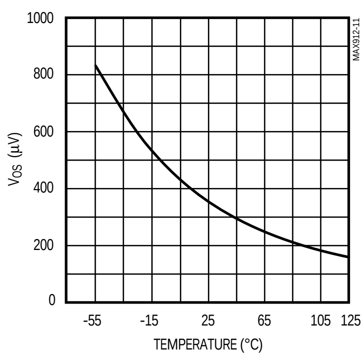
POSITIVE SUPPLY CURRENT (PER COMPARATOR) vs. POSTIVE SUPPLY VOLTAGE



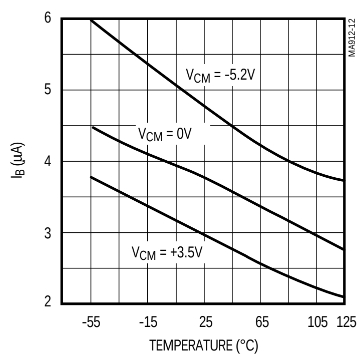
NEGATIVE SUPPLY CURRENT (PER COMPARATOR) vs. NEGATIVE SUPPLY VOLTAGE



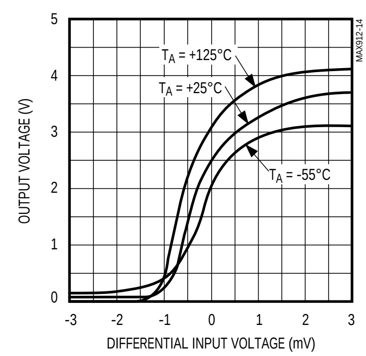
OFFSET VOLTAGE vs. TEMPERATURE



INPUT BIAS CURRENT vs. TEMPERATURE



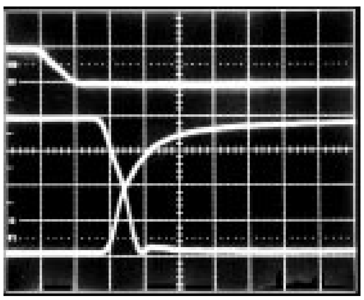
OUTPUT VOLTAGE vs. DIFFERENTIAL INPUT VOLTAGE



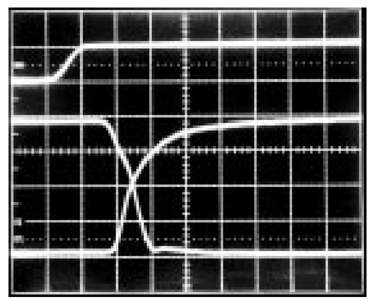
Typical Operating Characteristics (continued)

(V+ = 5V, V- = -5V, V_{LE} = 0V, C_L = 15pF, T_A = +25°C, unless otherwise noted.)

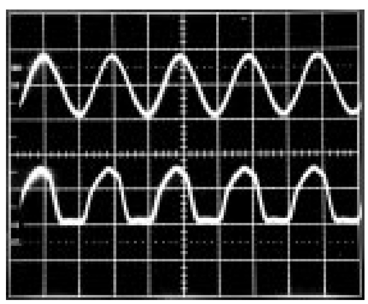
POSITIVE-TO-NEGATIVE PROPAGATION DELAY



NEGATIVE-TO-POSITIVE PROPAGATION DELAY

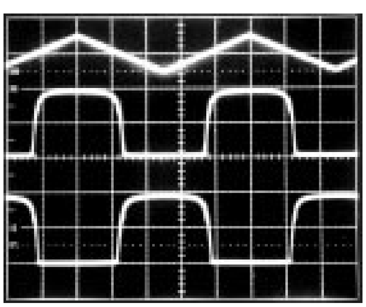


MAX912/MAX913 RESPONSE TO 50MHz (±10mVP-P) SINE WAVE

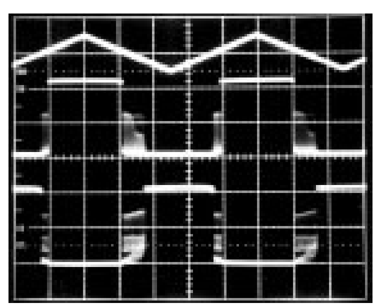


MAX912/MAX913 RESPONSE TO SLOW-MOVING TRIANGLE WAVE

MAX912/MAX913 RESPONSE



INDUSTRY STANDARD 686 RESPONSE



Pin Descriptions

PIN MAX912	NAME	FUNCTION
1	QA	Comparator A TTL output
2	$\overline{Q}$A	Comparator A complementary TTL output
3, 14	GND	Logic ground. Connect **both** GND pins to ground.
4	LEA	Comparator A latch enable. QA and $\overline{Q}$A are latched when LEA is high or floating. Comparator A latch is transparent when LEA is low.
5, 12	N.C.	Not internally connected
6	V-	Negative power supply: -5V for dual supplies (bypass to GND with a 0.1µF capacitor), or GND for a single supply
7	INA-	Comparator A inverting input
8	INA+	Comparator A noninverting input
9	INB+	Comparator B noninverting input
10	INB-	Comparator B inverting input
11	V+	Positive power supply, +5V. Bypass to GND with a 0.1µF capacitor.
13	LEB	Comparator B latch enable. QB and $\overline{Q}$B are latched when LEB is high or floating. Comparator B latch is transparent when LEB is low.
15	$\overline{Q}$B	Comparator B complementary TTL output
16	QB	Comparator B TTL output

PIN MAX913	NAME	FUNCTION
1	V+	Positive power supply. Bypass to GND with a 0.1µF capacitor.
2	IN+	Noninverting input
3	IN-	Inverting input
4	V-	Negative power supply: -5V for dual supplies (bypass to GND with a 0.1µF capacitor), or GND for a single supply
5	LE	Latch enable. Q and $\overline{Q}$ are latched when LE is TTL high or floating. The comparator latch is transparent when LE is low.
6	GND	Logic ground
7	Q	TTL output
8	$\overline{Q}$	Complementary TTL output

Detailed Description

The MAX913 (single) and MAX912 (dual) high-speed comparators have a unique design that prevents oscillation when the comparator is in its linear region. No minimum input slew rate is required.

Many high-speed comparators oscillate in the linear region, as shown in the *Typical Operating Characteristics'* industry-standard 686 response graph. One way to overcome this oscillation is to sample the output after it has passed through the unstable region. Another practical solution is to add hysteresis. Either solution results in a loss of resolution and bandwidth.

Because the MAX912/MAX913 do not need hysteresis, they offer high resolution to all signals—including low-frequency signals.

The MAX912/MAX913 provide a TTL-compatible latch function that holds the comparator output state (Figure 1). As long as Latch Enable (LE) is high or floating, the input signal has no effect on the output state. With LE low, the outputs are controlled by the input differential voltage and the latch is transparent.

Input Amplifier

A comparator can be thought of as having two sections: an input amplifier and a logic interface. The MAX912/MAX913's input amplifier is fully differential, with input offset voltage trimmed to below 2.0mV at +25°C. Input common-mode range extends from 200mV **below** the negative supply rail to 1.5V below the positive power supply. The total common-mode range is 8.7V when operating from ±5VDC supplies.

The MAX912/MAX913's amplifier has no built-in hysteresis. For highest accuracy, do not add hysteresis. Figure 2 shows how hysteresis degrades resolution.

Resolution

A comparator's ability to resolve small signal differences—its resolution—is affected by various factors. As with most amplifiers, the most significant factors are the input offset voltage (V_{OS}) and the common-mode and power-supply rejection ratios (CMRR, PSRR). If source impedance is high, input offset current can be significant. If source impedance is unbalanced, the input bias current can introduce another error.

For high-speed comparators, an additional factor in resolution is the comparator's stability in its linear region. Many high-speed comparators are useless in their linear region because they oscillate. This makes the differential input voltage region around 0V unusable, as does a high V_{OS}. Hysteresis does not cure the problem, but acts to keep the input away from its linear range (Figure 2).

The MAX912/MAX913 do not oscillate in the linear region, which greatly enhances the comparator's resolution.

Applications Information

Power Supplies and Bypassing

The MAX912/MAX913 are tested with ±5V power supplies that provide an input common-mode range (V_{CM}) of 8.7V (-5.2V to +3.5V). Operation from a single +5V supply provides a common-mode input range of 3.7V (-0.2V to +3.5V). Connect V- to GND for single-supply operation. The MAX912/MAX913 will operate from a minimum single-supply voltage of +4.5V.

The V+ supply provides power to both the analog input stage and digital output circuits, whereas the V- supply only powers the analog section. Bypass V+ and V- to ground with 0.1µF to 1.0µF ceramic capacitors in parallel with 10µF or greater tantalum capacitors. Connect the ceramic capacitors very close to the MAX912/MAX913's

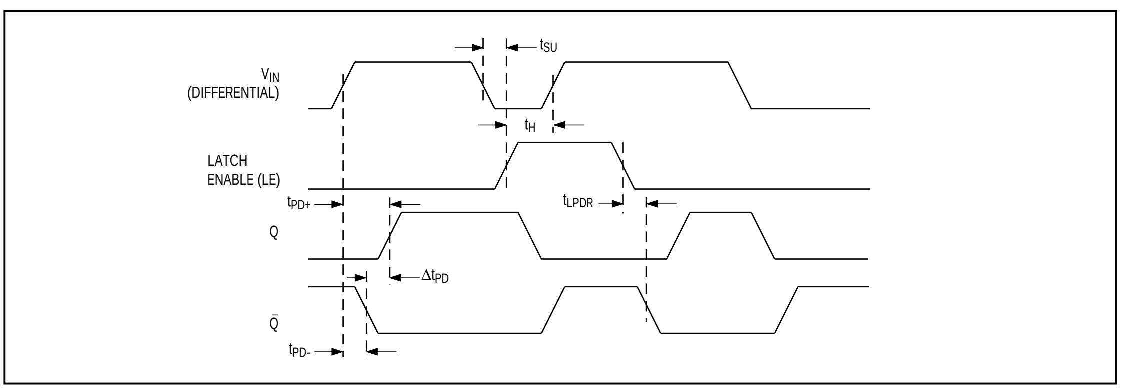


Figure 1. Timing Diagram

supply pins, keeping leads short to minimize lead inductance. For particularly noisy applications, use ferrite beads on the power-supply lines.

Board Layout

As with all high-speed components, careful attention to layout is essential for best performance.

1) Use a printed circuit board with an unbroken ground plane.
2) Pay close attention to the bandwidth of bypass components and keep leads short.
3) Avoid sockets; solder the comparator and other components directly to the board to minimize unwanted parasitic inductance and capacitance.

Input Slew Rate

The MAX912/MAX913 design eliminates the input slew-rate requirement imposed on many standard comparators. As long as LE is high after the maximum propagation delay and the input is greater than the comparator's total DC error, the output will be valid without oscillations.

Maximum Clock (LE) and Signal Rate

The maximum clock and signal rate is 70MHz, based on the comparator's rise and fall time with a 5mV overdrive at +25°C (Figure 1). With a 20mV overdrive, the maximum propagation delay is 12ns and the clock and signal rate is 85MHz.

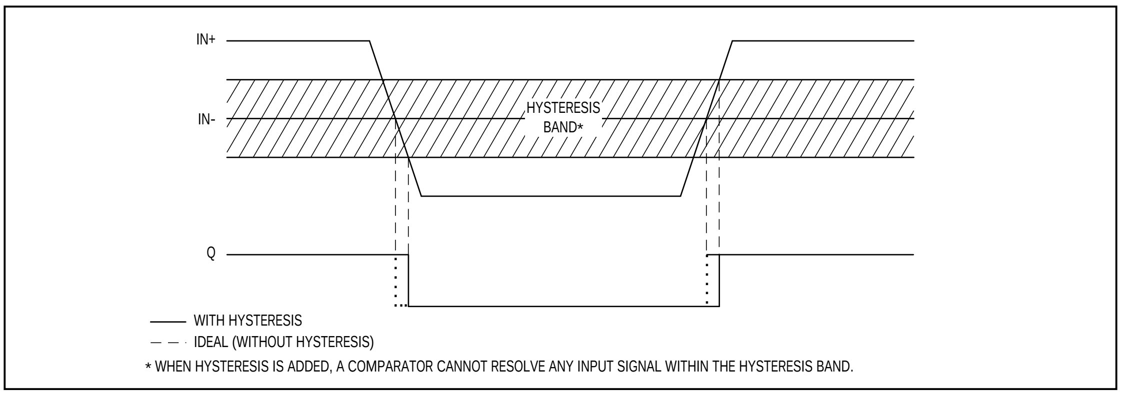
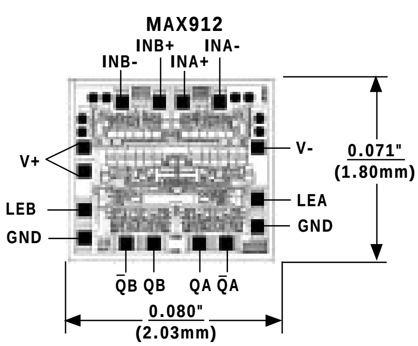
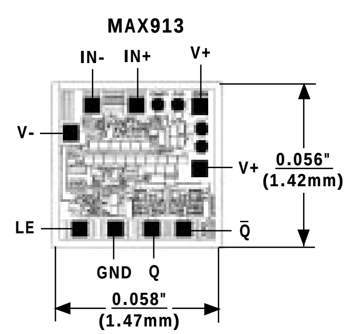


Figure 2. Effect of Hysteresis on Input Resolution

Chip Topographies



TRANSISTOR COUNT: 197;
SUBSTRATE CONNECTED TO V-.



TRANSISTOR COUNT: 100;
SUBSTRATE CONNECTED TO V-.

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