

MAXIM

800Mbps LVDS/LVPECL-to-LVDS 2 x 2 Crosspoint Switch

MAX9152

General Description

The MAX9152 2 x 2 crosspoint switch is designed for applications requiring high speed, low power, and low-noise signal distribution. This device includes two LVDS/LVPECL inputs, two LVDS outputs, and two logic inputs that set the internal connections between differential inputs and outputs.

The MAX9152 can be programmed to connect any input to either or both outputs, allowing it to be used in the following configurations: 2 x 2 crosspoint switch, 2:1 mux, 1:2 demux, 1:2 splitter, or dual repeater. This flexibility makes the MAX9152 ideal for protection switching in fault-tolerant systems, loopback switching for diagnostics, fanout buffering for clock/data distribution, and signal regeneration for communication over extended distances.

Ultra-low 120ps_{PK-PK} (max) PRBS jitter ensures reliable communications in high-speed links that are highly sensitive to timing error, especially those incorporating clock-and-data recovery, or serializers and deserializers. The high-speed switching performance guarantees an 800Mbps data rate and less than 50ps (max) skew between channels.

LVDS inputs and outputs are compatible with the TIA/EIA-644 LVDS standard. The LVDS inputs are designed to also accept LVPECL signals directly, and PECL signals with an attenuation network. The LVDS outputs are designed to drive 75Ω or 100Ω loads, and feature a selectable differential output resistance to minimize reflections.

The MAX9152 is available in 16-pin TSSOP and SO packages, and consumes only 109mW while operating from a single +3.3V supply over the -40°C to +85°C temperature range.

Applications

- Cell Phone Base Stations
- Add/Drop Muxes
- Digital Crossconnects
- DSLAMS
- Network Switches/Routers
- Protection Switching
- Loopback Diagnostics
- Clock/Data Distribution
- Cable Repeaters

Features

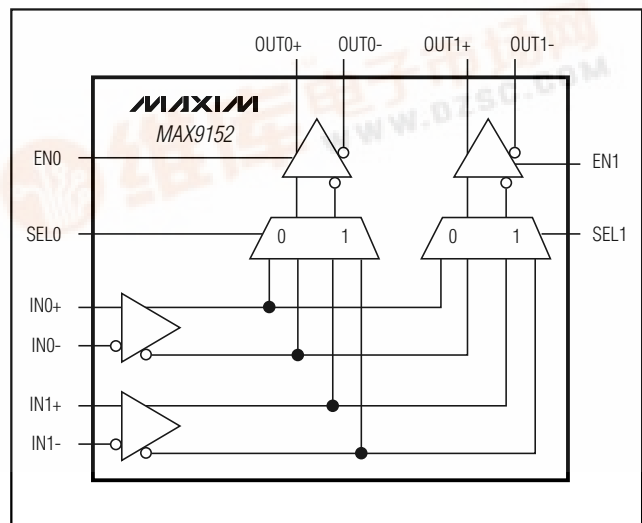
- ◆ Pin-Programmable Configuration
 - 2 x 2 Crosspoint Switch
 - 2:1 Mux
 - 1:2 Demux
 - 1:2 Splitter
 - Dual Repeater
- ◆ Ultra-Low 120ps_{PK-PK} (max) Jitter with 800Mbps, PRBS = 2²³ -1 Data Pattern
- ◆ Low 50ps (max) Channel-to-Channel Skew
- ◆ 109mW Power Dissipation
- ◆ Compatible with ANSI TIA/EIA-644 LVDS Standard
- ◆ Inputs Accept LVDS/LVPECL Signals
- ◆ LVDS Output Rated for 75Ω and 100Ω Loads
- ◆ Pin-Programmable Differential Output Resistance
- ◆ Pin-Compatible Upgrade to DS90CP22 (SO Package)
- ◆ Available in 16-Pin TSSOP Package (Half the Size of SO)

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX9152ESE	-40°C to +85°C	16 SO
MAX9152EUE	-40°C to +85°C	16 TSSOP

Pin Configuration appears at end of data sheet.

Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND-0.3V to +4.0V
 IN₊, IN₋, OUT₊, OUT₋ to GND-0.3V to +4.0V
 EN₋, SEL₋, NC/RSEL to GND-0.3V to (V_{CC} + 0.3V)
 Short-Circuit Duration (OUT₊, OUT₋)Continuous
 Continuous Power Dissipation (T_A = +70°C)
 16-Pin SO (derate 8.7mW/°C above +70°C)696mW
 16-Pin TSSOP (derate 9.4mW/°C above +70°C)755mW

Storage Temperature Range-65°C to +150°C
 Junction Temperature+150°C
 Operating Temperature Range-40°C to +85°C
 Lead Temperature (soldering, 10s)+300°C
 ESD Protection
 Human Body Model, IN₊, IN₋, OUT₊, OUT₋ ±7kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, NC/RSEL = open for R_L = 75Ω ±1%, NC/RSEL = high for R_L = 100Ω ±1%, differential input voltage |V_{ID}| = 0.1V to V_{CC}, input voltage (V_{IN+}, V_{IN-}) = 0 to V_{CC}, EN₋ = high, SEL0 = low, SEL1 = high, and T_A = -40°C to +85°C. Typical values at V_{CC} = +3.3V, |V_{ID}| = 0.2V, input common-mode voltage V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
LVCMOS/LVTTL INPUTS (EN₋, SEL₋)							
Input High Voltage	V _{IH}		2.0		V _{CC}	V	
Input Low Voltage	V _{IL}		GND		0.8	V	
Input High Current	I _{IH}	V _{IN} = V _{CC} or 2.0V	0		20	μA	
Input Low Current	I _{IL}	V _{IN} = 0 or 0.8V	-10		10	μA	
NC/RSEL INPUT							
Input High Voltage	V _{IH}		2.0		V _{CC}	V	
Input Low Voltage	V _{IL}		GND		0.8	V	
Input High Current	I _{IH}	V _{IN} = V _{CC} or 2.0V	0		20	μA	
Input Low Current	I _{IL}	V _{IN} = 0 or 0.8V	-10		10	μA	
DIFFERENTIAL INPUTS (IN₊, IN₋)							
Differential Input High Threshold	V _{TH}				100	mV	
Differential Input Low Threshold	V _{TL}		-100			mV	
Input Current	I _{IN+} , I _{IN-}	V _{IN+} = V _{CC} or 0, V _{IN-} = V _{CC} or 0	-1		1	μA	
		V _{IN+} = 3.6V or 0, V _{IN-} = 3.6V or 0, V _{CC} = 0	-1		1		
LVDS OUTPUTS (OUT₊, OUT₋)							
Differential Output Impedance (Note 2)	R _{DIFF}	NC/RSEL = low or open	60	90	118	Ω	
		NC/RSEL = high	85	122	155		
Differential Output Voltage	V _{OD}	R _L = 75Ω, NC/RSEL = open, Figure 1	280	382	470	mV	
		R _L = 100Ω, NC/RSEL = high, Figure 1					
Change in Magnitude of V _{OD} Between Complementary Output States	ΔV _{OD}	R _L = 75Ω, NC/RSEL = open, Figure 1				25	mV
		R _L = 100Ω, NC/RSEL = high, Figure 1					
Offset Common-Mode Voltage	V _{OS}	R _L = 75Ω, NC/RSEL = open, Figure 1	1.150			1.430	V
		R _L = 100Ω, NC/RSEL = high, Figure 1					
Change in Magnitude of V _{OS} Between Complementary Output States	ΔV _{OS}	R _L = 75Ω, NC/RSEL = open, Figure 1				25	mV
		R _L = 100Ω, NC/RSEL = high, Figure 1					

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +3.0V$ to $+3.6V$, NC/RSEL = open for $R_L = 75\Omega \pm 1\%$, NC/RSEL = high for $R_L = 100\Omega \pm 1\%$, differential input voltage $|V_{ID}| = 0.1V$ to V_{CC} , input voltage (V_{IN+} , V_{IN-}) = 0 to V_{CC} , EN_- = high, SEL0 = low, SEL1 = high, and $T_A = -40^\circ C$ to $+85^\circ C$. Typical values at $V_{CC} = +3.3V$, $|V_{ID}| = 0.2V$, input common-mode voltage $V_{CM} = 1.2V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Short-Circuit Current	I_{OS}	$V_{ID} = +100mV$, $V_{OUT+} = 0$, other output open		-12	-20	mA
		$V_{ID} = -100mV$, $V_{OUT-} = 0$, other output open				
Both Output Short-Circuit Current	I_{OSB}	$V_{ID} = +100mV$, $V_{OUT+} = 0$, $V_{OUT-} = 0$		-12	-20	mA
		$V_{ID} = -100mV$, $V_{OUT+} = 0$, $V_{OUT-} = 0$				
Output High-Z Current	I_{OZ+} , I_{OZ-}	Disabled, $V_{OUT+} = V_{CC}$ or 0, $V_{OUT-} = V_{CC}$ or 0	-1		1	μA
Power-Off Output Current	I_{OFF+} , I_{OFF-}	$V_{CC} = 0$, $V_{OUT+} = 3.6V$ or 0, $V_{OUT-} = 3.6V$ or 0	-1		1	μA
SUPPLY CURRENT						
Supply Current	I_{CC}	$R_L = 75\Omega$, $C_L = 5pF$, enabled, quiescent, Figure 5		38	55	mA
		$R_L = 100\Omega$, $C_L = 5pF$, enabled, quiescent, Figure 5		33	50	
		$R_L = 75\Omega$, $C_L = 5pF$, enabled, switching at 400MHz (800Mbps), Figure 5 (Note 2)		58	70	
		$R_L = 100\Omega$, $C_L = 5pF$, enabled, switching at 400MHz (800Mbps), Figure 5 (Note 2)		52	65	
High-Z Supply Current	I_{CCZ}	Disabled		15	25	mA

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = +3.0V$ to $+3.6V$, NC/RSEL = open for $R_L = 75\Omega \pm 1\%$, NC/RSEL = high for $R_L = 100\Omega \pm 1\%$, $C_L = 5pF$, differential input voltage $|V_{ID}| = 0.15V$ to V_{CC} , EN_- = high, SEL0 = low, SEL1 = high, differential input transition time = 0.6ns (20% to 80%), input voltage (V_{IN+} , V_{IN-}) = 0 to V_{CC} , LVCMOS/LVTTL inputs = 0 to 3V with 2ns (10% to 90%) transition times, $T_A = -40^\circ C$ to $+85^\circ C$. Typical values at $V_{CC} = +3.3V$, $|V_{ID}| = 0.2V$, $V_{CM} = 1.2V$, $T_A = +25^\circ C$, unless otherwise noted.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input to SEL Setup Time (Note 5)	t_{SET}	Figures 2, 3	0.4			ns
Input to SEL Hold Time (Note 5)	t_{HOLD}	Figures 2, 3	0.6			ns
SEL to Switched Output	t_{SWITCH}	Figures 2, 3	1.8	2.5	3.5	ns
Disable Time High to Z	t_{PHZ}	Figure 4			3.8	ns
Disable Time Low to Z	t_{PLZ}	Figure 4			3.8	ns
Enable Time Z to High	t_{PZH}	Figure 4			3.2	ns
Enable Time Z to Low	t_{PZL}	Figure 4			3.2	ns
Propagation Low-to-High Delay	t_{PLHD}	Figures 5, 6	1.7	2.3	3.4	ns
		$V_{CC} = +3.3V$, $T_A = +25^\circ C$; Figures 5, 6	2.0	2.3	2.9	
Propagation High-to-Low Delay	t_{PHLD}	Figures 5, 6	1.7	2.3	3.4	ns
		$V_{CC} = +3.3V$, $T_A = +25^\circ C$; Figures 5, 6	2.0	2.3	2.9	

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AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +3.0V$ to $+3.6V$, NC/RSEL = open for $R_L = 75\Omega \pm 1\%$, NC/RSEL = high for $R_L = 100\Omega \pm 1\%$, $C_L = 5pF$, differential input voltage $|V_{ID}| = 0.15V$ to V_{CC} , EN_- = high, SEL0 = low, SEL1 = high, differential input transition time = $0.6ns$ (20% to 80%), input voltage (V_{IN+} , V_{IN-}) = 0 to V_{CC} , LVCMOS/LVTTL inputs = 0 to 3V with 2ns (10% to 90%) transition times, $T_A = -40^\circ C$ to $+85^\circ C$. Typical values at $V_{CC} = +3.3V$, $|V_{ID}| = 0.2V$, $V_{CM} = 1.2V$, $T_A = +25^\circ C$, unless otherwise noted.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pulse Skew $ t_{PLHD} - t_{PHLD} $ (Note 6)	t_{SKEW}	Figures 5, 6		25	90	ps
Output Channel-to-Channel Skew	t_{CCS}	Figures 5, 7		20	50	ps
Output Low-to-High Transition Time (20% to 80%)	t_{LHT}	Figures 5, 6	160	270	480	ps
Output High-to-Low Transition Time (20% to 80%)	t_{HLT}	Figures 5, 6	160	270	480	ps
LVDS Data Path Peak-to-Peak Jitter (Note 7)	t_{JIT}	$V_{ID} = 200mV$, $V_{CM} = 1.2V$, 50% duty cycle, 800Mbps, input transition time = 600ps (20% to 80%)		10	30	ps
		$V_{ID} = 200mV$, $V_{CM} = 1.2V$, PRBS = $2^{23} - 1$ data pattern, 800Mbps, input transition time = 600ps (20% to 80%)		65	120	

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{TH} , V_{TL} , V_{ID} , V_{OD} , and ΔV_{OD} .

Note 2: Guaranteed by design and characterization, not production tested.

Note 3: AC parameters are guaranteed by design and characterization.

Note 4: C_L includes scope probe and test jig capacitance.

Note 5: t_{SET} and t_{HOLD} time specify that data must be in a stable state before and after the SEL transition.

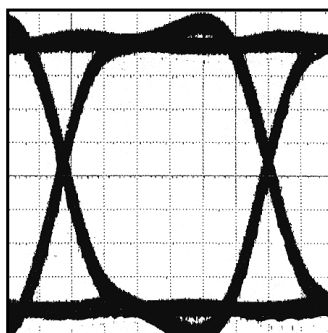
Note 6: t_{SKEW} is the magnitude difference of differential propagation delay over rated conditions; $t_{SKEW} = |t_{PHLD} - t_{PLHD}|$.

Note 7: Specification includes test equipment jitter.

Typical Operating Characteristics

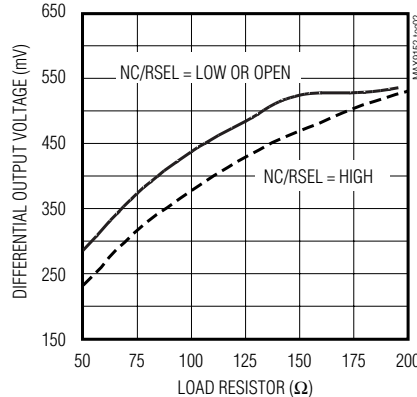
($V_{CC} = +3.3V$, $R_L = 100\Omega$, NC/RSEL = high, $C_L = 5pF$, input transition time = 600ps (20% to 80%), $V_{ID} = 200mV$, PRBS = $2^{23} - 1$ data pattern, $V_{CM} = +1.2V$, $T_A = +25^\circ C$, unless otherwise noted.)

DIFFERENTIAL OUTPUT EYE PATTERN IN 1:2 SPLITTER MODE AT 800Mbps

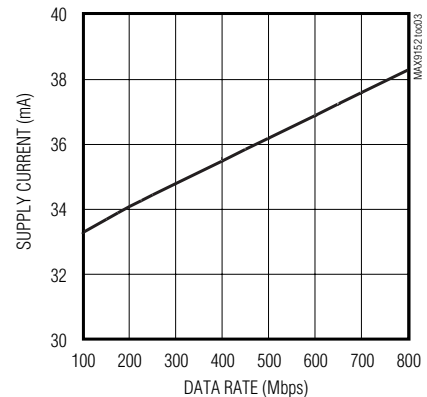


CONDITIONS: 3.3V, PRBS = $2^{23} - 1$ DATA PATTERN, $|V_{ID}| = 200mV$, $V_{CM} = +1.2V$
 HORIZONTAL SCALE = 200ps/div
 VERTICAL SCALE = 100mV/div

DIFFERENTIAL OUTPUT VOLTAGE vs. LOAD



SUPPLY CURRENT vs. DATA RATE

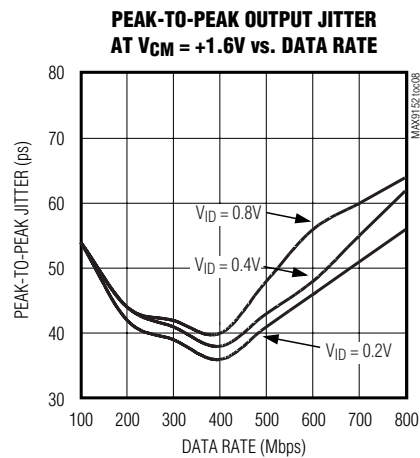
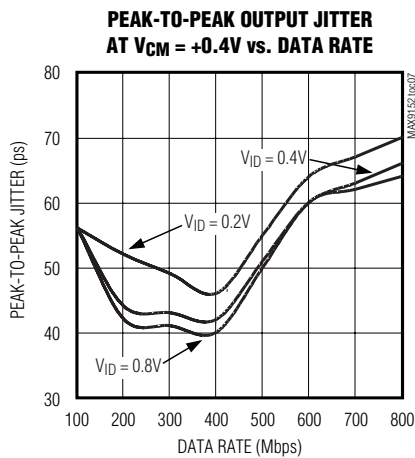
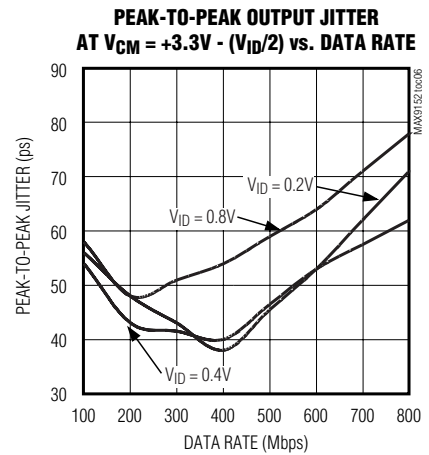
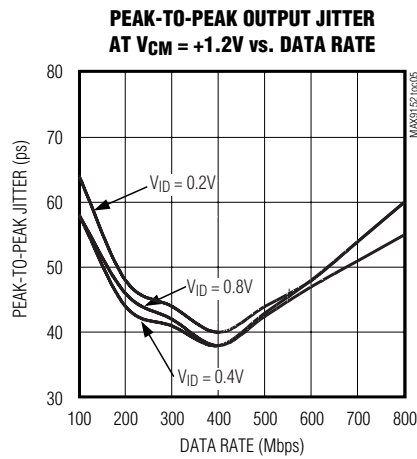
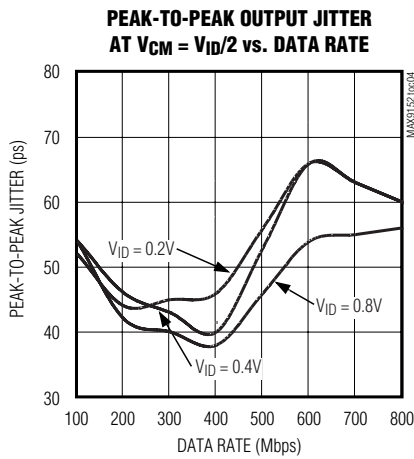


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Typical Operating Characteristics (continued)

($V_{CC} = +3.3V$, $R_L = 100\Omega$, NC/RSEL = high, $C_L = 5pF$, input transition time = 600ps (20% to 80%), $V_{ID} = 200mV$, PRBS = $2^{23} - 1$ data pattern, $V_{CM} = +1.2V$, $T_A = +25^\circ C$, unless otherwise noted.)

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Pin Description

PIN	NAME	FUNCTION
1, 2	SEL1, SEL0	LVCMOS/LVTTL Logic Inputs. Allow the switch to be configured as a mux, repeater, or splitter.
3, 4	IN0+, IN0-	LVDS/LVPECL Differential Input 0
5	V _{CC}	Power-Supply Input. Bypass V _{CC} to GND with 0.1μF and 0.001μF ceramic capacitors.
6, 7	IN1+, IN1-	LVDS/LVPECL Differential Input 1
8	NC/RSEL	Logic Input. Selects differential output resistance. Set NC/RSEL to open or low when R _L = 75Ω, set to high when R _L = 100Ω.
9	NC	No Connect
10, 11	OUT1-, OUT1+	LVDS Differential Output 1
12	GND	Ground
13, 14	OUT0-, OUT0+	LVDS Differential Output 0
15, 16	EN1, EN0	LVCMOS/LVTTL Logic Inputs. Enables or disables the outputs. Setting EN0 or EN1 high enables the corresponding output, OUT0 or OUT1. Setting EN0 or EN1 low puts the corresponding output into high impedance (differential output resistance is also high impedance).

Detailed Description

The LVDS interface standard is a signaling method intended for point-to-point communication over a controlled impedance medium as defined by the ANSI TIA/EIA-644 and IEEE 1596.3 standards. LVDS uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI emissions and system susceptibility to noise.

The MAX9152 is an 800Mbps 2 x 2 crosspoint switch designed for high-speed, low-power point-to-point and multidrop interfaces. The device accepts LVDS or differential LVPECL signals and routes them to outputs depending on the selected mode of operation.

A differential input with a magnitude of 0.1V to V_{CC} with single-ended voltage levels at or within the MAX9152's V_{CC} and ground switches the output. A differential input with a magnitude of at least 0.15V with single-ended voltage levels at or within the MAX9152's V_{CC} and ground is required to meet the AC specifications.

In the 1:2 splitter mode, the outputs repeat the selected input. This is useful for distributing a signal or creating a copy for use in protection switching. In the repeater

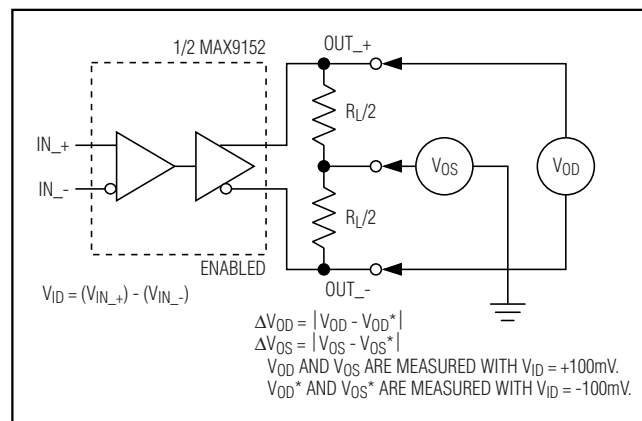


Figure 1. Test Circuit for V_{OD} and V_{OS}

mode, the device operates as a two-channel buffer. Repeating restores signal amplitude, allowing isolation of media segments or longer media drive. The device is a crosspoint switch where any input can be connected to any output or outputs. In 2:1 mux mode, primary and backup signals can be selected to provide a protection-switched, fault-tolerant application.

800Mbps LVDS/LVPECL-to-LVDS 2 x 2 Crosspoint Switch

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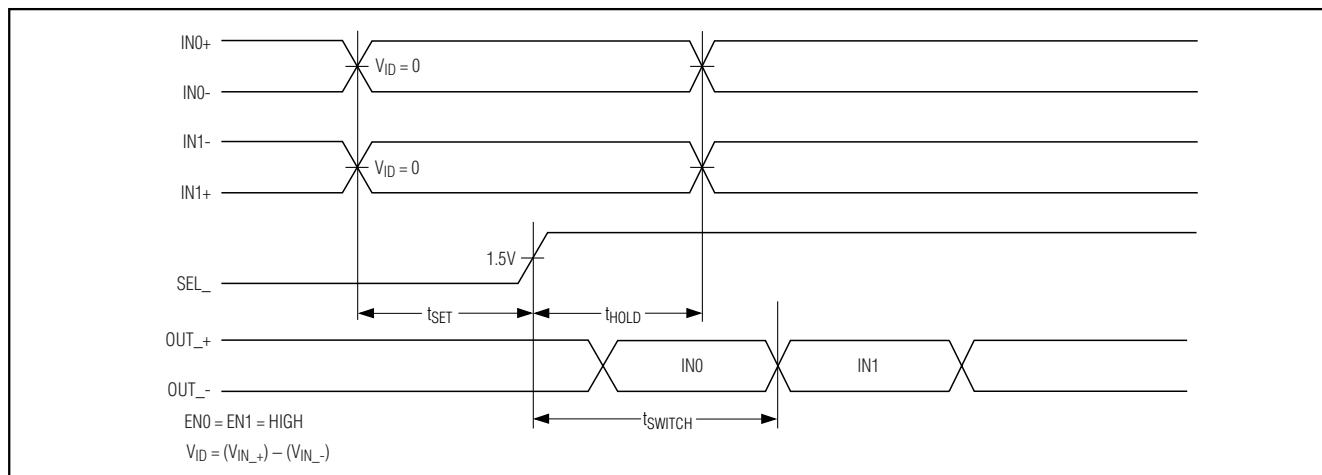


Figure 2. Input to Rising Edge Select Setup, Hold, and Mux Switch Timing Diagram

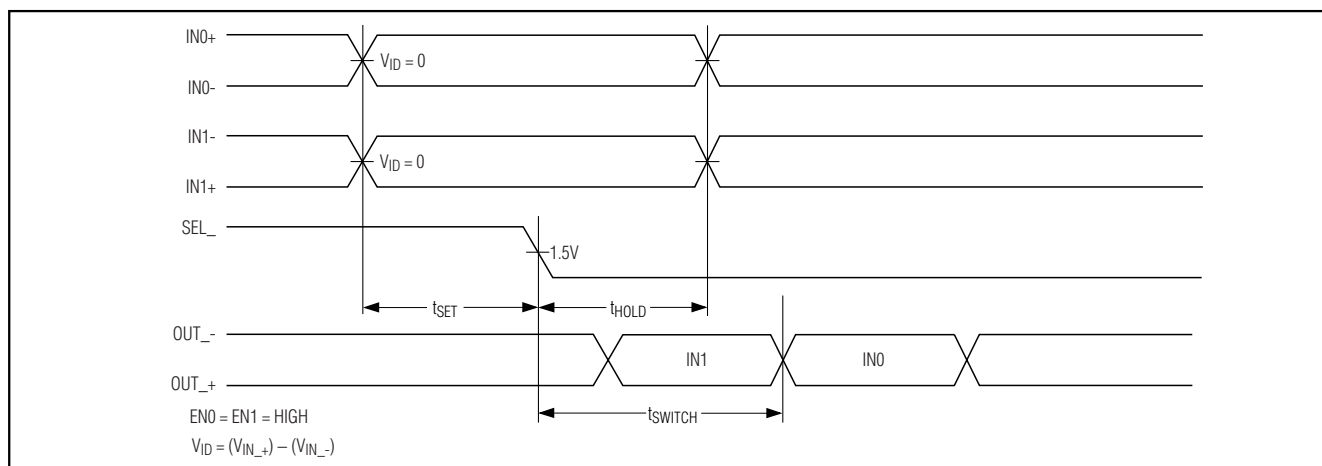


Figure 3. Input to Falling Edge Select Setup, Hold, and Mux Switch Timing Diagram

Input Fail-Safe

The differential inputs of the MAX9152 do not have internal fail-safe biasing. If fail-safe biasing is required, it can be implemented with external large-value resistors. IN₊ should be pulled up to V_{CC} with 10kΩ and IN₋ should be pulled down to GND with 10kΩ. The voltage-divider formed by the 10kΩ resistors and the 100Ω termination resistor (across IN₊ and IN₋) provides a slight positive differential bias and sets a high state at the device output when inputs are undriven.

Output Resistance

The MAX9152 has a selectable differential output resistance to reduce reflections from impedance discontinuities in the interconnect. Reflections are reduced,

compared to a high-impedance output. A termination resistor at the receiver is still required and is the primary termination for the interconnect. Select the output resistance that best matches the differential characteristic impedance of the interconnect used.

Select Function

The SEL0 and SEL1 logic inputs allow the device to be configured as a high-speed differential crosspoint, 2:1 mux, 1:2 demux, dual repeater, or 1:2 splitter (Figure 8). See Table 1 for mode selection settings.

Enable Function

The EN0 and EN1 logic inputs enable and disable driver outputs OUT0 and OUT1. Setting EN0 or EN1 high enables the corresponding driver output. Setting EN0

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or EN1 low puts the corresponding driver output into a high-impedance state (the differential output resistance also becomes high impedance).

Table 1. Input/Output Function Table

SEL0	SEL1	OUT0	OUT1	MODE
L	L	IN0	IN0	1:2 splitter
L	H	IN0	IN1	Repeater
H	L	IN1	IN0	Switch
H	H	IN1	IN1	1:2 splitter

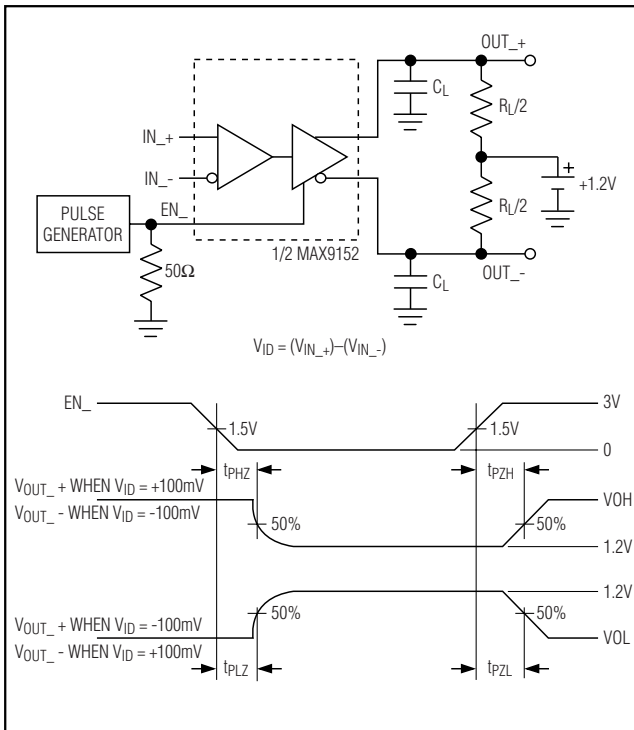


Figure 4. Output Active to High-Z and High-Z to Active Test Circuit and Timing Diagram

Applications Information

Unused Differential Inputs

Unused differential inputs should be tied to ground and VCC to prevent the high-speed input stage from switching due to noise. IN₊ should be pulled to VCC with 10kΩ and IN₋ should be pulled to GND with 10kΩ.

Expanding the Number of LVDS Output Ports

Devices can be cascaded to make larger switches. Total propagation delay and total jitter should be considered to determine the maximum allowable switch size. Three MAX9152s are needed to make a 2 input x 4 output crosspoint switch with two device propagation delays. Seven MAX9152s make a 2 input x 8 output crosspoint with three device delays.

Accepting PECL Inputs

The inputs accept PECL signals with the use of an attenuation circuit, as shown in Figure 9.

Power-Supply Bypassing

Bypass VCC to ground with high-frequency surface-mount ceramic 0.1μF and 0.001μF capacitors in paral-

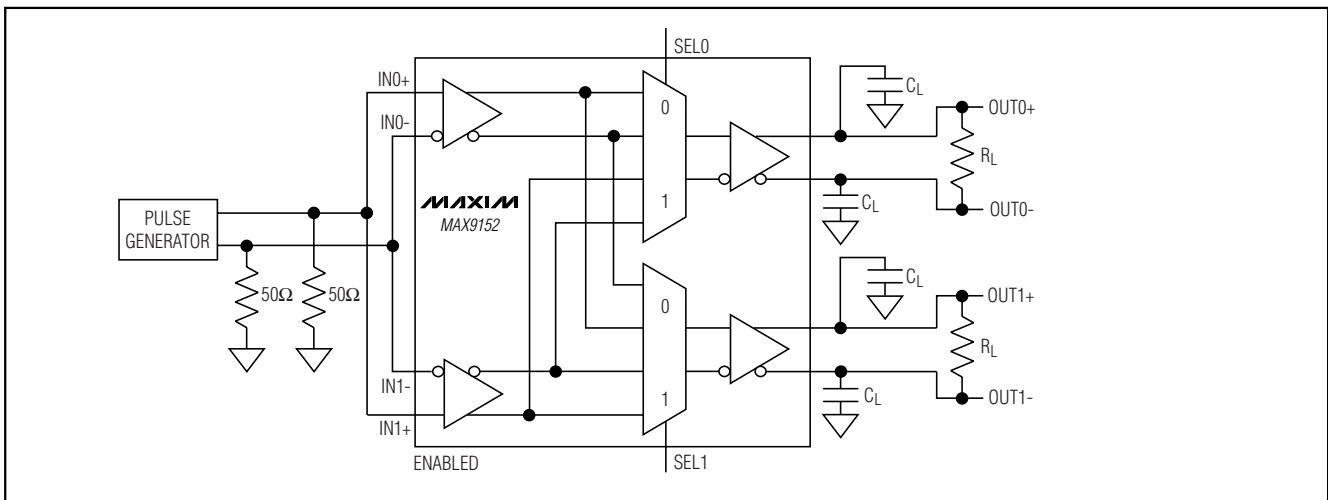


Figure 5. Output Transition Time, Propagation Delay, and Output Channel-to-Channel Skew Test Circuit

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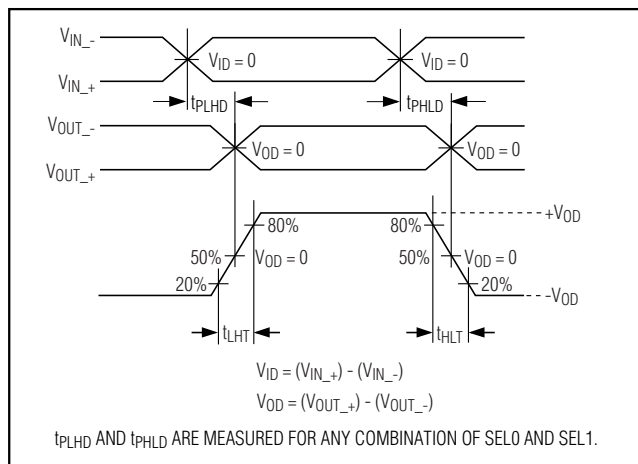


Figure 6. Output Transition Time and Propagation Delay Timing Diagram

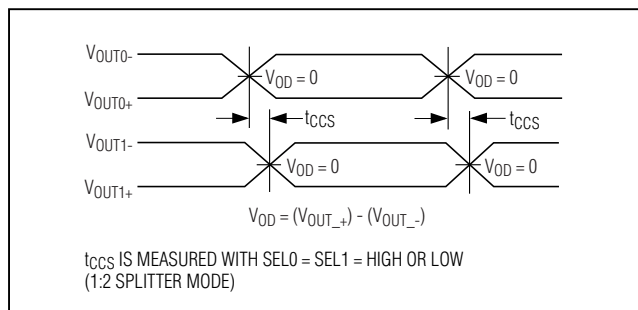


Figure 7. Output Channel-to-Channel Skew

lel as close to the device as possible, with the smaller value capacitor closest to V_{CC} .

Differential Traces

Trace characteristics affect the performance of the MAX9152. Use controlled-impedance traces. Eliminate reflections and ensure that noise couples as common mode by running the differential trace pairs close together. Reduce skew by matching the electrical length of the traces. Excessive skew can result in a degradation of magnetic field cancellation.

Maintain the distance between the differential traces to avoid discontinuities in differential impedance. Avoid 90° turns and minimize the number of vias to further prevent impedance discontinuities.

Cables and Connectors

Transmission media should have nominal differential impedance of 75Ω or 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

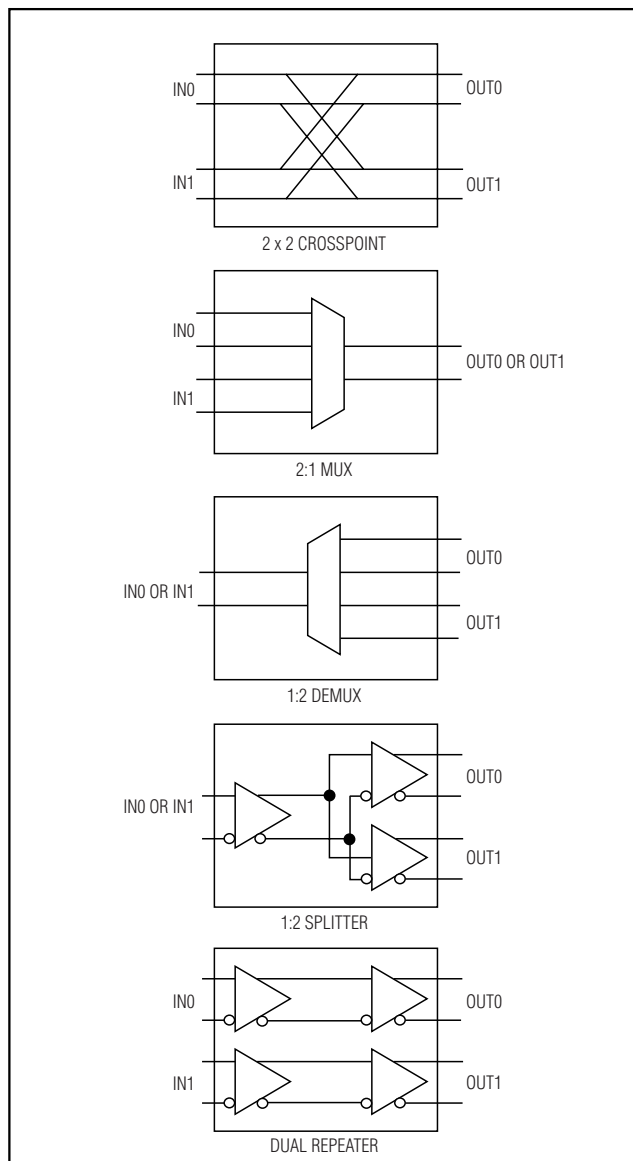


Figure 8. Programmable Configurations

Avoid the use of unbalanced cables such as ribbon or simple coaxial cable. Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to canceling effects. Balanced cables tend to pick up noise as common mode, which is rejected by the differential receiver.

Board Layout

For LVDS applications, a four-layer printed-circuit (PC) board that provides separate power, ground, and signal planes is recommended.

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Chip Information

TRANSISTOR COUNT: 880
PROCESS: CMOS

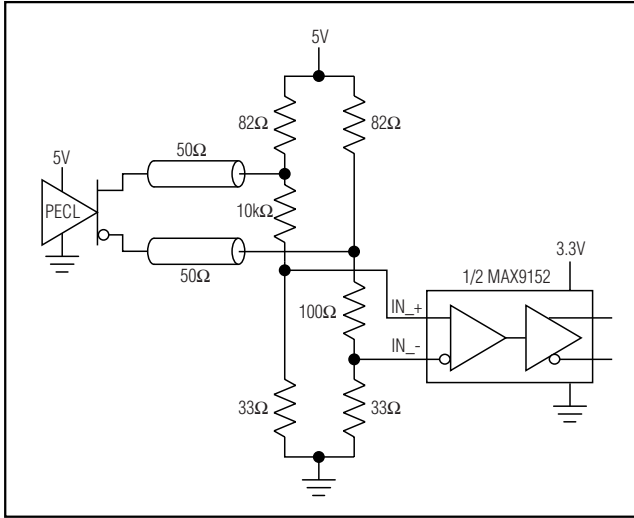
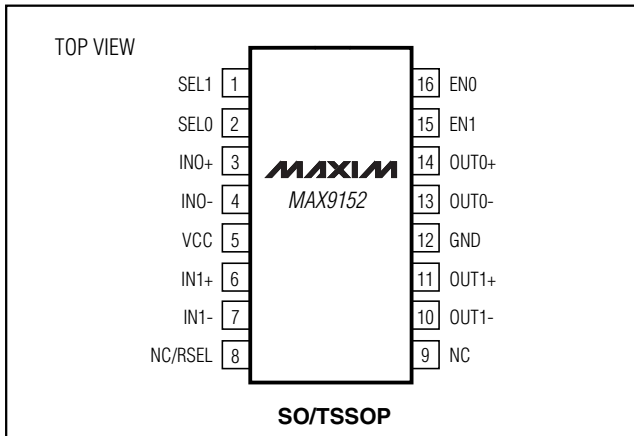


Figure 9. PECL to LVDS Level Conversion Network

Pin Configuration

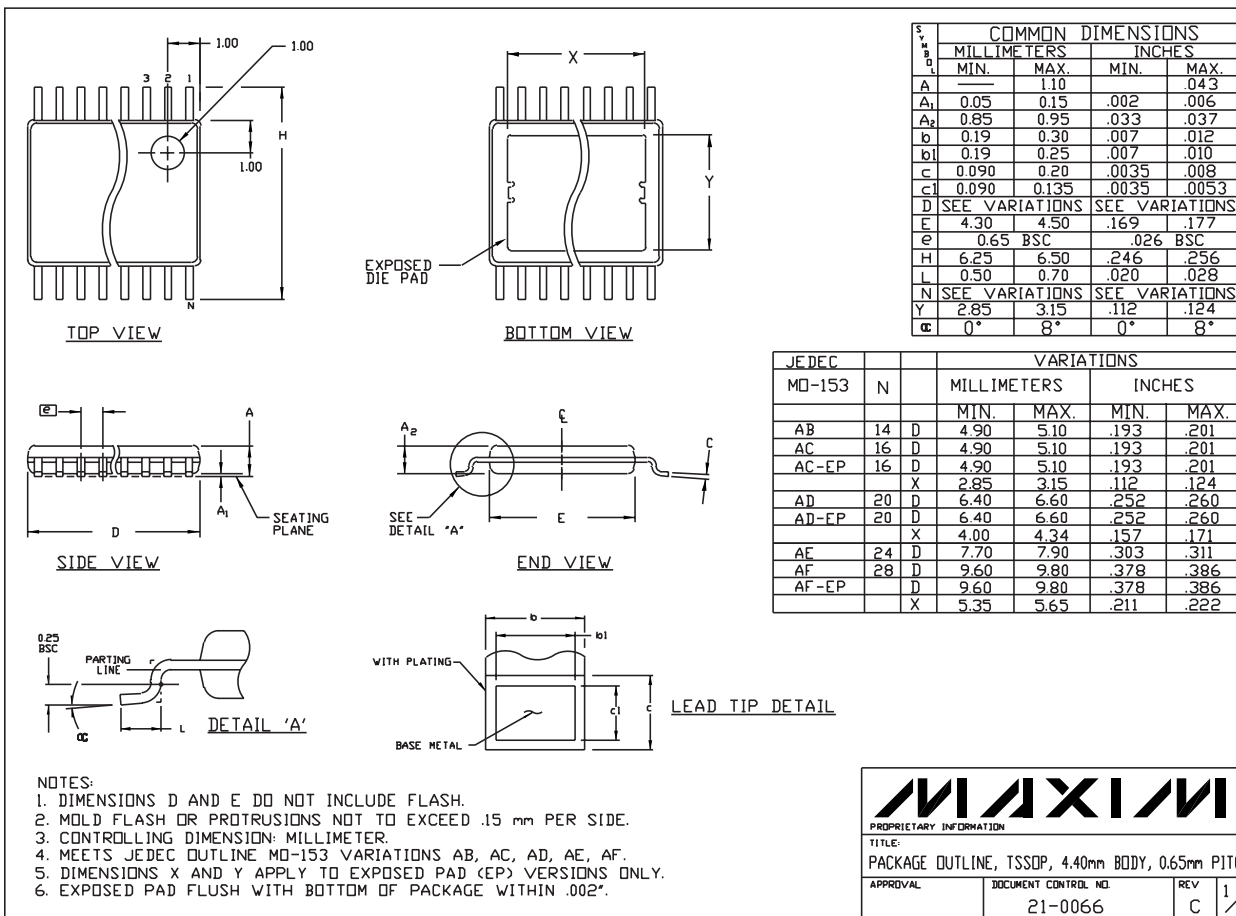


800Mbps LVDS/LVPECL-to-LVDS 2 x 2 Crosspoint Switch

Package Information

MAX9152

TSSOP:EP



800Mbps LVDS/LVPECL-to-LVDS 2 x 2 Crosspoint Switch

Package Information (continued)

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS		N	MS012
	MIN	MAX	MIN	MAX		
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
 1. D&E DO NOT INCLUDE MOLD FLASH
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
 3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
 4. CONTROLLING DIMENSION: MILLIMETER
 5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
 6. N = NUMBER OF PINS

MAXIM PACKAGE FAMILY OUTLINE: SOIC .150" 1/1 21-0041 A
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