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ET2716(0) • ET2716(1)

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16,384-BIT (2048 x 8) UV ERASABLE PROM

MEMORY COMPONENTS

The ET2716 is a high speed 16K UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

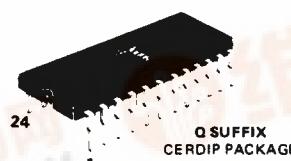
The ET2716 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, N-channel silicon gate technology X-MOS.

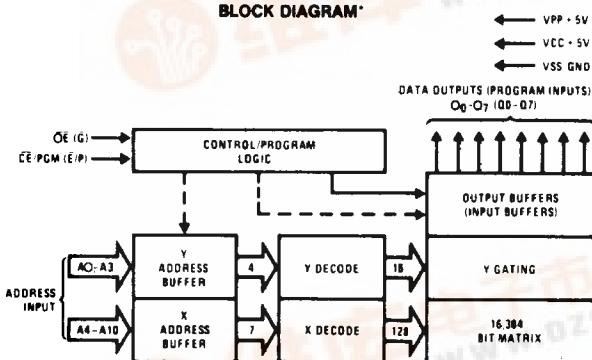
- 2048 x 8 organization
- 525 mW max active power, 132 mW max standby power
- Low power during programming
- Access time ET2716-1, 350ns ; ET2716, 450ns
- Single 5V power supply
- Static-no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- Three-state output with OR-tie capability

NMOS

16,384-BIT
(2048 x 8)
UV ERASABLE PROM



BLOCK DIAGRAM*



Pin Connection During Read or Program

MODE	PIN NAME/NUMBER				
	CE/PGM (E/P) 18	OE (G) 20	VPP 21	VCC 24	OUTPUTS 9-11, 13-17
Read	VIL	VIL	5	5	DOUT
Program	Pulsed VIL to VIH	VIH	25	5	DIN

*Symbols in parentheses are proposed JEDEC standard.

PIN ASSIGNMENT

A7	1	24	VCC
A6	2	23	AB
A5	3	22	A9
A4	4	21	VPP
A3	5	20	OE (G)
A2	6	19	A10
A1	7	18	CE/PGM (E/P)
A0	8	17	A7 (Q7)
Q0 (Q0)	9	16	Q8 (Q8)
Q1 (Q1)	10	15	Q5 (Q5)
Q2 (Q2)	11	14	Q4 (Q4)
VSS	12	13	Q3 (Q3)

PIN NAMES*

A0-A10	Address Inputs
Q0-Q7 (Q0-Q7)	Data Outputs
CE/PGM (E/P)	Chip Enable/Program
OE (G)	Output Enable
VPP	Read 5V, Program 25V
VCC	Power (5V)
VSS	Ground

ABSOLUTE MAXIMUM RATINGS (Note 1)

Temperature Under Bias	-10°C to 80°C	All Input or Output Voltages with Respect to VSS (except VPP)	6V to -0.3V
Storage Temperature	-65°C to +125°C	Power Dissipation	1.5 W
VPP Supply Voltage with Respect to VSS	26.5V to -0.3V	Lead Temperature (Soldering, 10 seconds)	300°C

READ OPERATION (Note 2)

DC OPERATING CHARACTERISTICS (Note 3)

$T_A = 0^\circ C$ to $+70^\circ C$, $VCC = 5V \pm 5\%$ for ET2716, $VCC = 5V \pm 10\%$ for ET2716-1

$VPP = VCC$ (Note 4), $VSS = 0V$, (Unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	TYP		UNITS
			MIN	MAX	
I _{LI}	Input Current	$VIN = 5.25V$ or $VIN = VIL$	-	-	10 μA
I _{LO}	Output Leakage Current	$VOUT = 5.25V$, $\bar{CE}/PGM = 5V$	-	-	10 μA
I _{PP1}	VPP Supply Current	$VPP = 5.25V$	-	-	5 mA
I _{CC1}	VCC Supply Current (Standby)	$\bar{CE}/PGM = VIH$, $\bar{OE} = VIL$	-	10	25 mA
I _{CC2}	VCC Supply Current (Active)	$\bar{CE}/PGM = \bar{OE} = VIL$	-	57	100 mA
V _{IL}	Input Low Voltage		-0.1	-	0.8 V
V _{IH}	Input High Voltage		2.0	-	$VCC + 1$ V
V _{OH}	Output High Voltage	$IOH = 400 \mu A$	2.4	-	1 V
V _{OL}	Output Low Voltage	$IOL = 2.1 mA$	-	-	0.45 V

AC CHARACTERISTICS

$T_A = 0^\circ C$ to $+70^\circ C$, $VCC = 5V \pm 5\%$ for ET2716, $VCC = 5V \pm 10\%$ for ET2716-1

$VPP = VCC$ (Note 4), $VSS = 0V$, (Unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	ET2716-1		ET2716	UNITS	
			MIN	MAX			
I _{ACC}	T _{AVQV}	Address to Output Delay	$\bar{CE}/PGM = \bar{OE} = VIL$	-	350	-	450 ns
I _{CE}	T _{ELQV}	\bar{CE} to Output Delay	$\bar{OE} = VIL$	-	350	-	450 ns
I _{OE}	T _{GLQV}	Output Enable to Output Delay	$\bar{CE}/PGM = VIL$	-	120	-	120 ns
I _{DF}	T _{GHQZ}	Output Enable High to Output Hi-Z	$\bar{CE}/PGM = VIL$	0	100	0	100 ns
I _{OH}	T _{AQXQ}	Address to Output Hold	$\bar{CE}/PGM = \bar{OE} = VIL$	0	-	0	-
I _{OD}	T _{EHQZ}	\bar{CE} to Output Hi-Z	$\bar{OE} = VIL$	0	100	0	100 ns

AC Test Conditions

CAPACITANCE (Note 5)

$T_A = 25^\circ C$, $f = 1 MHz$

SYMBOL	PARAMETER	CONDITIONS	TYP	MAX	UNITS
C _I	Input Capacitance	$VIN = 0V$	4	6	pF
C _O	Output Capacitance	$VOUT = 0V$	8	12	pF

Output Load: 1 TTL gate and $CL = 100 pF$
 Input Rise and Fall Times: 20 ns
 Input pulse levels: 0.45V to 2.4V
 Timing measurement reference level =
 Inputs and outputs 0.8V and 2V

Note 1 : "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2 : VCC must be applied at the same time or before VPP and removed after or at the same time as VPP

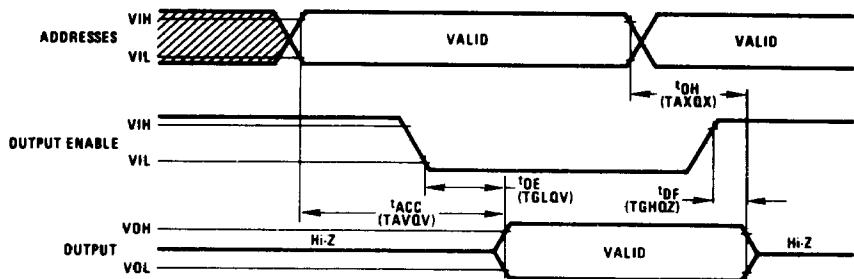
Note 3 : Typical conditions are for operation at: $T_A = 25^\circ C$, $VCC = 5V$, $VPP = VCC$, and $VSS = 0V$

Note 4 : VPP may be connected to VCC except during program.

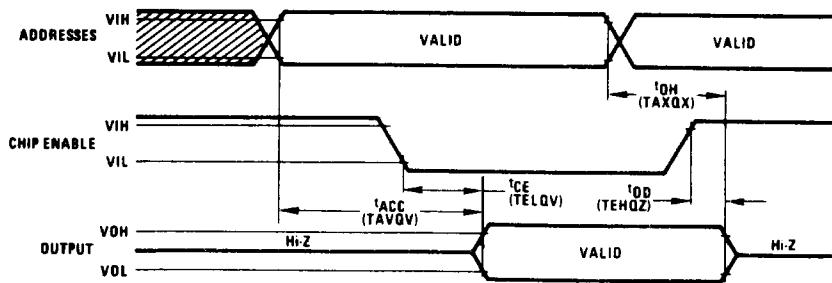
Note 5 : Capacitance is guaranteed by periodic testing. $T_A = 25^\circ C$, $f = 1 MHz$.

SWITCHING TIME WAVEFORMS*

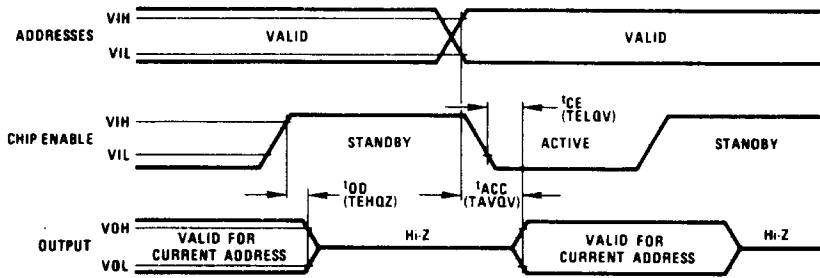
Read Cycle ($\overline{CE}/\overline{PGM} = VIL$)



Read Cycle ($\overline{OE} = VIL$)



Standby Power Down Mode ($\overline{OE} = ViL$)



* Symbols in parentheses are proposed JEDEC standard.

PROGRAM OPERATION

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS (Notes 1 and 2)

(TA = 25°C ± 5°C) (VCC = 5V ± 5%, VPP = 25V ± 1V)

SYMBOL	PARAMETER	MIN	MAX	UNITS
IL1	Input Leakage Current (Note 3)	—	10	µA
VIL	Input Low Level	-0.1	0.8	V
VIH	Input High Level	2.0	VCC + 1	V
ICC	VCC Power Supply Current	—	100	mA
IPP1	VPP Supply Current (Note 4)	—	5	mA
IPP2	VPP Supply Current During Programming Pulse (Note 5)	—	30	mA

AC CHARACTERISTICS AND OPERATING CONDITIONS (Notes 1, 2, and 6)

(TA = 25°C ± 5°C) (VCC = 5V ± 5%, VPP = 25V ± 1V)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	
taS	TAVPH	Address Setup Time	2	—	—	µs
tOS	TGHPH	OE Setup Time	2	—	—	µs
tDS	TDVPH	Data Setup Time	2	—	—	µs
taH	TPLAX	Address Hold Time	2	—	—	µs
tOH	TPLGX	OE Hold Time	2	—	—	µs
tDH	TPLDX	Data Hold Time	2	—	—	µs
tDF	TGHQZ	Chip Disable to Output Float Delay (Note 4)	0	—	100	ns
tCE	TGLQV	Chip Enable to Output Delay (Note 4)	—	—	120	ns
tPW	TPHPL	Program Pulse Width	45	50	55	ms
tPR	TPH1PH2	Program Pulse Rise Time	5	—	—	ns
tPF	TPL2PL1	Program Pulse Fall Time	5	—	—	ns

Note 1 : VCC must be applied at the same time or before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be inserted into a board with power applied.

Note 2 : Care must be taken to prevent overshoot of the VPP supply when switching to + 25V

Note 3 : 0.45V ≤ VIN ≤ 5.25V

Note 4 : CE/PGM = VIL, VPP = VCC

Note 5 : VPP = 26 V

Note 6 : Transition times ≤ 20 ns unless otherwise noted

Program Mode

The ET2716 is programmed by introducing "0" s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the chip enable pin. All input voltage levels including the program pulse on chip enable are TTL compatible. The programming sequence is :

With $V_{PP} = 25V$, $V_{CC} = 5V$, $\overline{OE} = VIH$ and $\overline{CE}/\overline{PGM} = VIL$, an address is selected and the desired data word is applied to the output pins. ($VIL = "0"$ and $VIL = "1"$ for both address and data). After the address and data signals are stable the program pin is pulsed from VIL to VIH with a pulse width between 45 ms and 55 ms.

Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (VIH or higher) must not be maintained longer than $t_{PW(MAX)}$ on the program pin during programming. ET2716's may be programmed in parallel with the same data in this mode.

Program Verify Mode

The programming of the ET2716 may be verified either 1 word at a time during the programming (as shown in the timing diagram) or by reading all of the words out at the end of the programming sequence. This can be done with $V_{PP} = 25V$ (or $5V$) in either case. V_{PP} must be at $5V$ for all operating modes and can be maintained at $25V$ for all programming modes.

Program Inhibit Mode

The program inhibit mode allows programming several ET2716's simultaneously with different data for each

one by controlling which ones receive the program pulse. All similar inputs of the ET2716 may be paralleled. Pulsing the program pin (from VIL to VIH) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{OE} = VIH$ will put its outputs in the Hi-Z state.

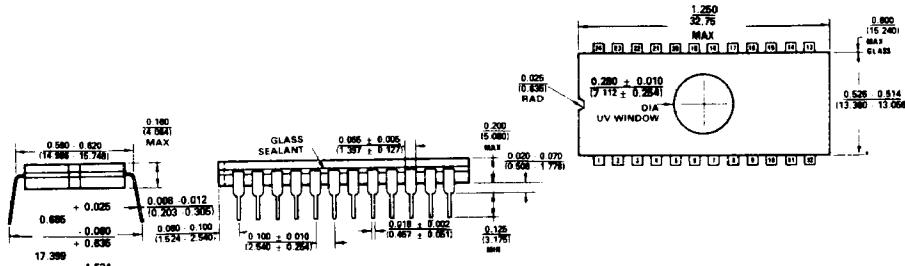
ERASING

The ET2716 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the ET2716 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time.

An ultraviolet source of 2537 \AA yielding a total integrated dosage of 15 watt-seconds/cm² is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a $12,000 \mu\text{W}/\text{cm}^2$ power rating is used. The ET2716 to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

PHYSICAL DIMENSIONS inches (millimeters)

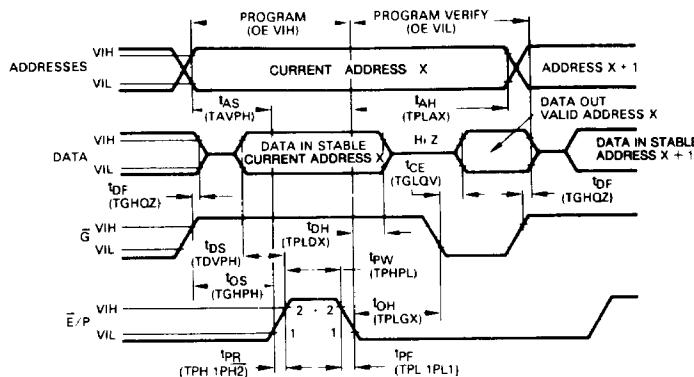


UV window Cavity Dual-In-Line Package (JQ)
Order Number ET2716Q (-, 1)
Package Number J24 CQ

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

TIMING DIAGRAM *

Program Mode



DEVICE OPERATION

The ET2716 has 3 modes of operation in the normal system environment. These are shown in Table I.

Read Mode

The ET 2716 read operation requires that $\overline{OE} = VIL$, $\overline{CE}/PCM = VIL$ and that addresses A0—A10 have been stabilized. Valid data will appear on the output pins after t_{ACC} , t_{OE} or t_{CE} times (see Switching Time Waveforms) depending on which is limiting.

Deselect Mode

The ET 2716 is deselected by making \overline{OE} = VIH. This mode is independent of CE/PGM and the condition of the addresses. The outputs are Hi-Z when \overline{OE} = VIH. This allows OR-tying 2 or more ET2716's for memory expansion.

Standby Mode (Power Down)

The ET2716 may be powered down to the standby mode by making CE/PGM = VIH. This is independent of OE and automatically puts the outputs in their Hi-Z state. The power is reduced to 25 % (132 mW max) of the normal operating power. VCC and VPP must be maintained at 5V. Access time at power up remains either t_{ACC} or t_{CF} (see **Switching Time Waveforms**).

PROGRAMMING

The ET 2716 is shipped from THOMSON SEMICONDUCTEURS completely erased. All bits will be at "1" level (output high) in this initial state and after any full erasure. Table II shows the 3 programming modes.

TABLE I. OPERATING MODES (V_{CC} = V_{PP} = 5V)

MODE	PIN NAME/NUMBER		
	CE/PGM (E/P) 18	OE (G) 20	OUTPUTS
Read	VIL	VIL	DOUT
Deselect	Don't Care	VIH	Hi Z
Standby	VIH	Don't Care	Hi Z

TABLE II. PROGRAMMING MODES (VCC = 5V)

MODE	PIN NAME/NUMBER			
	CE/PGM (E/P) 18	OE (G) 20	VPP 21	OUTPUTS Q 9-11, 13-17
Program	Pulsed VIL to VIH	VIH	25	DIN
Program Verify	VIL	VIL	25(5)	DOUT
Program Inhibit	VIL	VIH	25	H _z

* Symbols in parentheses are proposed JEDEC standard.