查询ETL9344供应商 捷多邦，专业PCB打样工厂，24小时加急出货

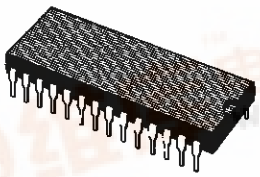
SGS-THOMSON MICROELECTRONICS

ETL9444/ETL9445 ETL9344/ETL9345

4-BIT NMOS MICROCONTROLLERS

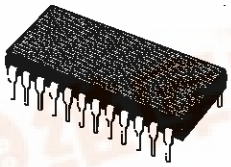
- LOW COST
- POWERFUL INSTRUCTION SET
- 2k x 8 ROM, 128 x 4 RAM
- 23 I/O LINES (ETL9444)
- TRUE VECTORED INTERRUPT, PLUS RESTART
- THREE-LEVEL SUBROUTINE STACK
- 16µs INSTRUCTION TIME
- SINGLE SUPPLY OPERATION (4.5-6.3V)
- LOW CURRENT DRAIN (13mA max.)
- INTERNAL TIME-BASE COUNTER FOR REAL-TIME PROCESSING
- INTERNAL BINARY COUNTER REGISTER WITH MICROWIRE® SERIAL I/O CAPABILITY
- GENERAL PURPOSE AND TRI-STATE® OUTPUTS
- LSTTL/CMOS COMPATIBLE IN AND OUT
- DIRECT DRIVE OF LED DIGIT AND SEGMENT LINES
- SOFTWARE/HARDWARE COMPATIBLE WITH OTHER MEMBERS OF ET9400 FAMILY
- EXTENDED TEMPERATURE RANGE DEVICES
  ETL9344/L9345 (– 40°C to + 85°C)
- WIDER SUPPLY RANGE (4.5 – 9.5V) OPTIONALLY AVAILABLE
- SOIC 24/28 AND PLCC 28 PACKAGES AVAILABLE

ETL9444/ETL9344



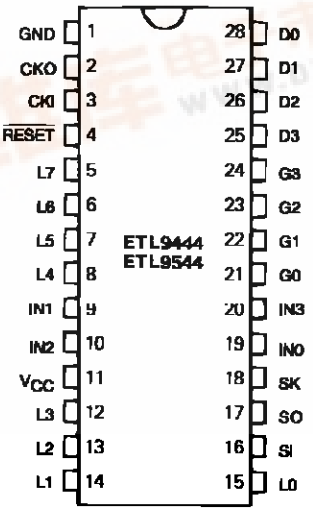
N
(Plastic Package)

ETL9345/ETL9345



N
(Plastic Package)

PIN CONNECTION



DESCRIPTION

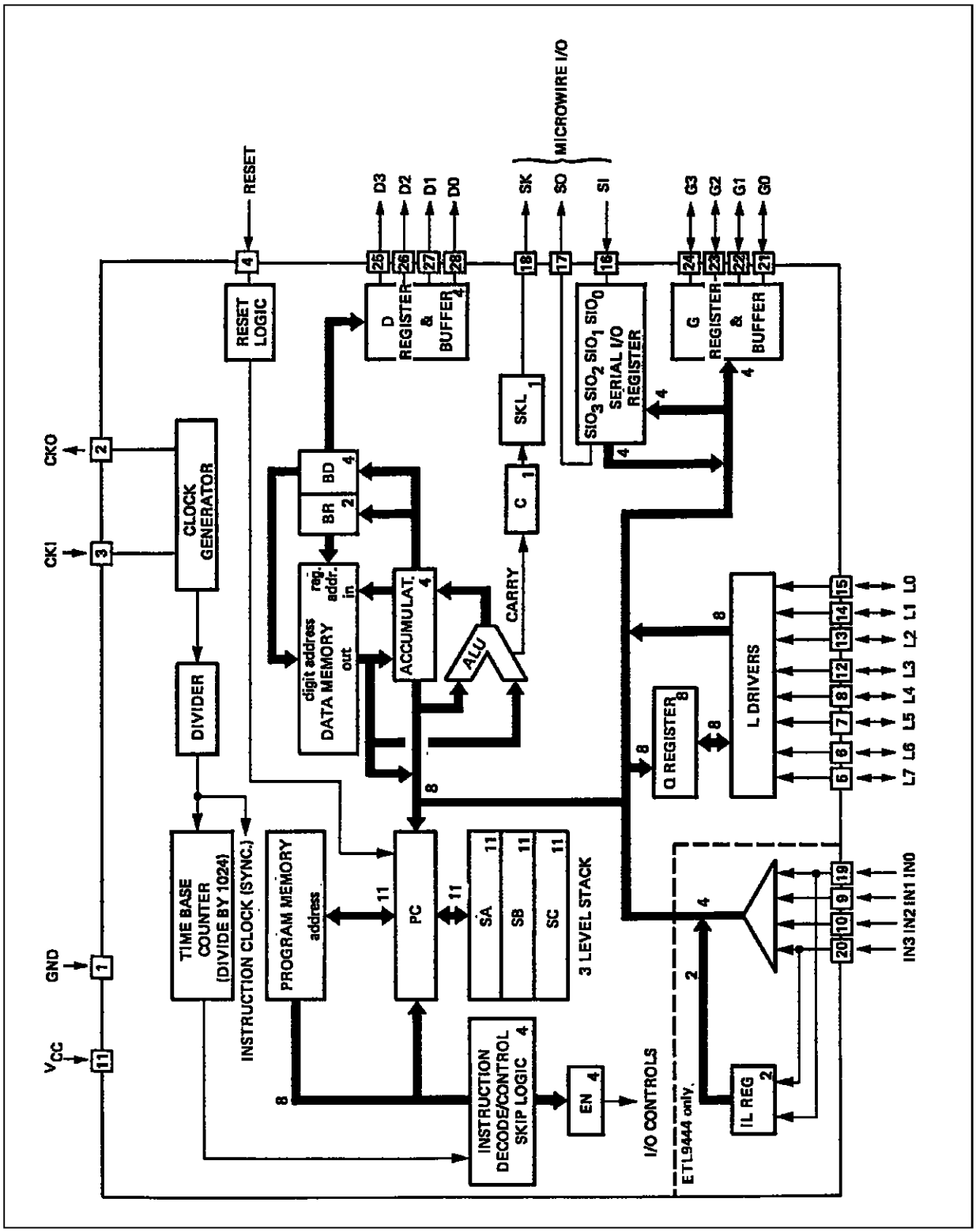
The ETL9444/L9445 and ETL9344/L9345 Single-Chip N-Channel Microcontrollers are fully compatible with the COPS® family, fabricated using N-channel, silicon gate XMOS technology. They are complete microcomputers containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The ETL9445 is identical to the ETL9444, except with 19 I/O lines instead of 23 : They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customi-

找PDF 维库一下 pdf.dzsc.com

zed controller oriented processor at a low end-product cost.

The ETL9344/L9345 are exact functional equivalents, but extended temperature range versions of the ETL9444/L9445 respectively.

Figure 1 : Block Diagram (28-pin version).



ETL9444/L9445

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	Voltage at any Pin Relative to GND	– 0.5 to + 10	V
	Ambient Operating Temperature	0 to + 70	°C
	Ambient Storage Temperature	– 65 to + 150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C
	Power Dissipation	0.75W at 25°C 0.4W at 70°C	
	Total Source Current	120	mA
	Total Sink Current	120	mA

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +70°C$, $4.5V \le V_{CC} \le 9.5V$ (unless otherwise specified)

Parameter	Test Conditions	Min.	Max.	Unit
Standard Operating Voltage (V_{CC})	Note 1	4.5	6.3	V
Optional Operating Voltage (V_{CC})		4.5	9.5	V
Power Supply Ripple	Peak to Peak		0.5	V
Operating Supply Current	All Inputs and Outputs Open		13	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input (÷ 32, ÷ 16, ÷ 8)				
Logic High (V_{IH})		2.0		V
Logic Low (V_{IL})		– 0.3	0.4	V
Schmitt Trigger Input (÷ 4)				
Logic High (V_{IH})		0.7 V_{CC}		V
Logic Low (V_{IL})		– 0.3	0.6	V
$\overline{\text{RESET}}$ Input Levels	Schmitt Trigger Input			
Logic High		0.7 V_{CC}		V
Logic Low		– 0.3	0.6	V
SO Input Level (test mode)		2.0	2.5	V
All Other Inputs				
Logic High	V_{CC} = Max.	3.0		V
Logic High	With TTL trip level options	2.0		V
Logic Low	selected, V_{CC} = 5V ± 5%.	– 0.3	0.8	V
Logic High	With high trip level options	3.6		V
Logic Low	selected.	– 0.3	1.2	V
Input Capacitance			7	pF
Hi-Z Input Leakage		– 1	+ 1	µA
Output Voltage Levels				
LSTTL Operation	V_{CC} = 5V ± 5%			
Logic High (V_{OH})	I_{OH} = – 25µA	2.7		V
Logic Low (V_{OL})	I_{OL} = 0.36mA		0.4	V
CMOS Operation				
Logic High	I_{OH} = – 10µA	V_{CC} – 1		V
Logic Low	I_{OL} = + 10µA		0.2	V

Note : 1. V_{CC} voltage change must be less than 0.5V in a 1ms period to maintain proper operation.

ETL9444/L9445

DC ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Min.	Max.	Unit
Output Current Levels				
Output Sink Current				
SO and SK Outputs (I_{OL})	V_{CC} = 9.5V, V_{OL} = 0.4V	1.8		mA
	V_{CC} = 6.3V, V_{OL} = 0.4V	1.2		mA
	V_{CC} = 4.5V, V_{OL} = 0.4V	0.9		mA
L_0-L_7 Outputs and Standard	V_{CC} = 9.5V, V_{OL} = 0.4V	0.8		mA
G_0-G_3, D_0-D_3 Outputs (I_{OL})	V_{CC} = 6.3V, V_{OL} = 0.4V	0.5		mA
	V_{CC} = 4.5V, V_{OL} = 0.4V	0.4		mA
G_0-G_3 and D_0-D_3 Outputs with	V_{CC} = 9.5V, V_{OL} = 1.0V	15		mA
High Current Options (I_{OL})	V_{CC} = 6.3V, V_{OL} = 1.0V	11		mA
	V_{CC} = 4.5V, V_{OL} = 1.0V	7.5		mA
G_0-G_3 and D_0-D_3 Outputs with	V_{CC} = 9.5V, V_{OL} = 1.0V	30		mA
Very High Current Options (I_{OL})	V_{CC} = 6.3V, V_{OL} = 1.0V	22		mA
	V_{CC} = 4.5V, V_{OL} = 1.0V	15		mA
CKI (single-pin RC oscillator)	V_{CC} = 4.5V, V_{IH} = 3.5V	2		mA
CKO	V_{CC} = 4.5V, V_{OL} = 0.4V	0.2		mA
Output Source Current				
Standard Configuration,	V_{CC} = 9.5V, V_{OH} = 2.0V	– 140	– 800	µA
All Outputs (I_{OH})	V_{CC} = 6.3V, V_{OH} = 2.0V	– 75	– 480	µA
	V_{CC} = 4.5V, V_{OH} = 2.0V	– 30	– 250	µA
Push-pull Configuration	V_{CC} = 9.5V, V_{OH} = 4.75V	– 1.4		mA
SO and SK Outputs (I_{OH})	V_{CC} = 6.3V, V_{OH} = 2.4V	– 1.4		mA
	V_{CC} = 4.5V, V_{OH} = 1.0V	– 1.2		mA
LED Configuration, L_0-L_7				
Outputs, Low Current	V_{CC} = 9.5V, V_{OH} = 2.0V	– 1.5	– 18	mA
Driver Option (I_{OH})	V_{CC} = 6.0V, V_{OH} = 2.0V	– 1.5	– 13	mA
LED Configuration, L_0-L_7				
Outputs, High Current	V_{CC} = 9.5V, V_{OH} = 2.0V	– 3.0	– 35	mA
Driver Option (I_{OH})	V_{CC} = 6.0V, V_{OH} = 2.0V	– 3.0	– 25	mA
TRI-STATE® Configuration,	V_{CC} = 9.5V, V_{OH} = 5.5V	– 0.75		mA
L_0-L_7 Outputs, Low	V_{CC} = 6.3V, V_{OH} = 3.2V	– 0.8		mA
Current Driver Option (I_{OH})	V_{CC} = 4.5V, V_{OH} = 1.5V	– 0.9		mA
TRI-STATE® Configuration,	V_{CC} = 9.5V, V_{OH} = 5.5V	– 1.5		mA
L_0-L_7 Outputs, High	V_{CC} = 6.3V, V_{OH} = 3.2V	– 1.6		mA
Current Driver Option (I_{OH})	V_{CC} = 4.5V, V_{OH} = 1.5V	– 1.8		mA
Input Load Source Current	V_{CC} = 5.0V, V_{IL} = 0V	– 10	– 140	µA
CKO Output				mA
RAM Power Supply Option				
Power Requirement	V_R = 3.3V		6.0	
TRI-STATE® Output Leakage Current		– 2.5	+ 2.5	µA
Total Sink Current Allowed				
All Outputs Combined			120	mA
D, G Ports			120	mA
L_7-L_4			4	mA
L_3-L_0			4	mA
All Other Pins			1.5	mA
Total Source Current Allowed				
All I/O Combined			120	mA
L_7-L_4			60	mA
L_3-L_0			60	mA
Each L Pin			30	mA
All Other Pins			1.5	mA

ETL9344/L9345

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	Voltage at any Pin Relative to GND	– 0.5 to + 10	V
	Ambient Operating Temperature	– 40 to + 85	°C
	Ambient Storage Temperature	– 65 to + 150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C
	Power Dissipation	0.75W at 25°C 0.25W at 85°C	
	Total Source Current	120	mA
	Total Sink Current	120	mA

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS $-40°C \le T_A \le +85°C$, $4.5V \le V_{CC} \le 7.5V$ (unless otherwise specified)

Parameter	Test Conditions	Min.	Max.	Unit
Standard Operating Voltage (V_{CC})	Note 1	4.5	5.5	V
Optional Operating Voltage (V_{CC})		4.5	7.5	V
Power Supply Ripple	Peak to Peak		0.5	V
Operating Supply Current	All Inputs and Outputs Open		15	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input				
Logic High (V_{IH})		2.2		V
Logic Low (V_{IL})		– 0.3	0.3	V
Schmitt Trigger Input				
Logic High (V_{IH})		0.7 V_{CC}		V
Logic Low (V_{IL})		– 0.3	0.4	V
$\overline{\text{RESET}}$ Input Levels	Schmitt Trigger Input			
Logic High		0.7 V_{CC}		V
Logic Low		– 0.3	0.4	V
SO Input Level (test mode)		2.2	2.5	V
All Other Inputs				
Logic High	V_{CC} = Max.	3.0		V
Logic High	With TTL trip level options	2.2		V
Logic Low	selected, $V_{CC} = 5V \pm 5\%$	– 0.3	0.6	V
Logic High	With high trip level options	3.6		V
Logic Low	selected	– 0.3	1.2	V
Input Capacitance			7	pF
Hi-Z Input Leakage		– 2	+ 2	µA
Output Voltage Levels				
LSTTL Operation	$V_{CC} = 5V \pm 5\%$			
Logic High (V_{OH})	I_{OH} = – 20µA	2.7		V
Logic Low (V_{OL})	I_{OL} = 0.36mA		0.4	V
CMOS Operation				
Logic High	I_{OH} = – 10µA	V_{CC} – 1		V
Logic Low	I_{OL} = + 10µA		0.2	V

Note : 1. V_{CC} voltage change must be less than 0.5V in a 1ms period to maintain proper operation.

ETL9344/L9345

DC ELECTRICAL CHARACTERISTICS (continued)

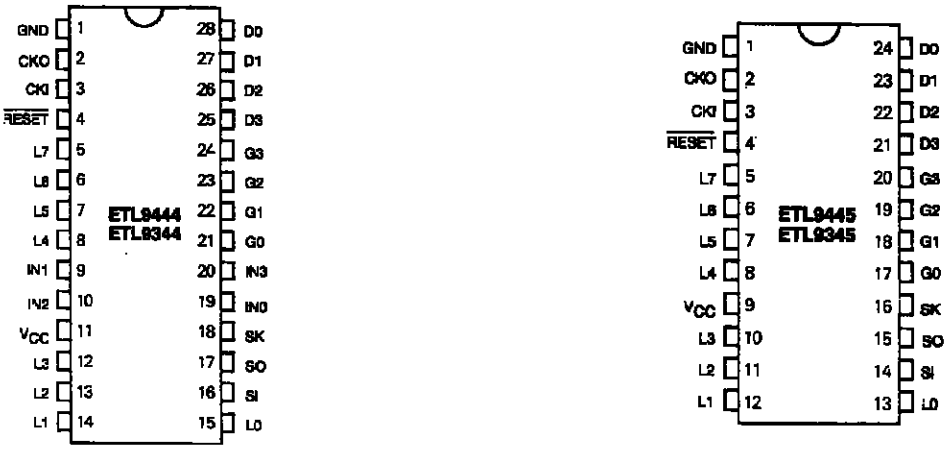
Parameter	Test Conditions	Min.	Max.	Unit
Output Current Levels				
Output Sink Current				
SO and SK Outputs (I_{OL})	V_{CC} = 7.5V, V_{OL} = 0.4V	1.4		mA
	V_{CC} = 5.5V, V_{OL} = 0.4V	1.0		mA
	V_{CC} = 4.5V, V_{OL} = 0.4V	0.8		mA
L_0-L_7 Outputs and Standard	V_{CC} = 7.5V, V_{OL} = 0.4V	0.6		mA
G_0-G_3, D_0-D_3 Outputs (I_{OL})	V_{CC} = 5.5V, V_{OL} = 0.4V	0.5		mA
	V_{CC} = 4.5V, V_{OL} = 0.4V	0.4		mA
G_0-G_3 and D_0-D_3 Outputs with	V_{CC} = 7.5V, V_{OL} = 1.0V	12		mA
High Current Options (I_{OL})	V_{CC} = 5.5V, V_{OL} = 1.0V	9		mA
	V_{CC} = 4.5V, V_{OL} = 1.0V	7		mA
G_0-G_3 and D_0-D_3 Outputs with	V_{CC} = 7.5V, V_{OL} = 1.0V	24		mA
Very High Current Options (I_{OL})	V_{CC} = 5.5V, V_{OL} = 1.0V	18		mA
	V_{CC} = 4.5V, V_{OL} = 1.0V	14		mA
CKI (single-pin RC oscillator)	V_{CC} = 4.5V, V_{IH} = 3.5V	2		mA
CKO	V_{CC} = 4.5V, V_{OL} = 0.4V	0.2		mA
Output Source Current				
Standard Configuration,	V_{CC} = 7.5V, V_{OH} = 2.0V	– 100	– 900	µA
All Outputs (I_{OH})	V_{CC} = 5.5V, V_{OH} = 2.0V	– 55	– 600	µA
	V_{CC} = 4.5V, V_{OH} = 2.0V	– 28	– 350	µA
Push-pull Configuration	V_{CC} = 7.5V, V_{OH} = 3.75V	– 0.85		mA
SO and SK Outputs (I_{OH})	V_{CC} = 5.5V, V_{OH} = 2.0V	– 1.1		mA
	V_{CC} = 4.5V, V_{OH} = 1.0V	– 1.2		mA
LED Configuration, L_0-L_7	V_{CC} = 7.5V, V_{OH} = 2.0V	– 1.4	– 27	mA
Outputs, Low Current	V_{CC} = 6.0V, V_{OH} = 2.0V	– 1.4	– 17	mA
Driver Option (I_{OH})	V_{CC} = 5.5V, V_{OH} = 2.0V	– 0.7	– 15	mA
LED Configuration, L_0-L_7	V_{CC} = 7.5V, V_{OH} = 2.0V	– 2.7	– 54	mA
Outputs, High Current	V_{CC} = 6.0V, V_{OH} = 2.0V	– 2.7	– 34	mA
Driver Option (I_{OH})	V_{CC} = 5.5V, V_{OH} = 2.0V	– 1.4	– 30	mA
TRI-STATE® Configuration,	V_{CC} = 7.5V, V_{OH} = 4.0V	– 0.7		mA
L_0-L_7 Outputs, Low	V_{CC} = 5.5V, V_{OH} = 2.7V	– 0.6		mA
Current Driver Option (I_{OH})	V_{CC} = 4.5V, V_{OH} = 1.5V	– 0.9		mA
TRI-STATE® Configuration,	V_{CC} = 7.5V, V_{OH} = 4.0V	– 1.4		mA
L_0-L_7 Outputs, High	V_{CC} = 5.5V, V_{OH} = 2.7V	– 1.2		mA
Current Driver Option (I_{OH})	V_{CC} = 4.5V, V_{OH} = 1.5V	– 1.8		mA
Input Load Source Current	V_{CC} = 5.0V, V_{IL} = 0V	– 10	– 200	µA
CKO Output				mA
RAM Power Supply Option				
Power Requirement	V_R = 3.3V		8.0	
TRI-STATE® Output Leakage Current		– 5	+ 5	µA
Total Sink Current Allowed				
All Outputs Combined			120	mA
D. G Ports			120	mA
L_7-L_4			4	mA
L_3-L_0			4	mA
All Other Pins			1.5	mA
Total Source Current Allowed				
All I/O Combined			120	mA
L_7-L_4			60	mA
L_3-L_0			60	mA
Each L Pin			30	mA
All Other Pins			1.5	mA

AC ELECTRICAL CHARACTERISTICS

ETL9444/L9445 : $0°C \le T_A \le +70°C$, $4.5V \le V_{CC} \le 9.5V$ (unless otherwise specified)
ETL9344/L9345 : $-40°C \le T_A \le +85°C$, $4.5V \le V_{CC} \le 7.5V$ (unless otherwise specified)

Parameter	Test Conditions	Min.	Max.	Unit
Instruction Cycle Time – t_c		16	40	µs
CKI				
Input Frequency – f_I	÷ 32 Mode	0.8	2.0	MHz
	÷ 16 Mode	0.4	1.0	MHz
	÷ 8 Mode	0.2	0.5	MHz
	÷ 4 Mode	0.1	0.25	MHz
Duty Cycle		30	60	%
Rise Time	f_I = 2MHz		120	ns
Fall Time			80	ns
CKI Using RC (÷ 4)	R = 56kΩ ± 5%			
	C = 100pF ± 10%			
Instruction Cycle Time		16	28	µs
CKO as SYNC Input				
t_{SYNC}		400		ns
INPUTS :				
IN_3-IN_0, G_3-G_0, L_7-L_0				
t_{SETUP}			8.0	µs
t_{HOLD}			1.3	µs
SI				
t_{SETUP}			2.0	µs
t_{HOLD}			1.0	µs
OUTPUT PROPAGATION DELAY	Test Condition :			
	C_L = 50pF, R_L = 20kΩ, V_{OUT} = 1.5V			
SO, SK Outputs				
t_{pd1}, t_{pd0}			4.0	µs
All Other Outputs				
t_{pd1}, t_{pd0}			5.6	µs

Figure 2 : Connection Diagrams.



Pin	Description
L_7-L_0	8 Bidirectional I/O Ports with TRI-STATE®
G_3-G_0	4 Bidirectional I/O Ports
D_3-D_0	4 General Purpose Outputs
IN_3-IN_0	4 General Purpose Inputs (COP444L only)
SI	Serial Input (or counter input)
SO	Serial Output (or general purpose output)
SK	Logic-controlled Clock (or general purpose output)
CKI	System Oscillator Input
CKO	System Oscillator Output (or general purpose input, RAM power supply, or SYNC input)
$\overline{\text{RESET}}$	System Reset Input
V_{CC}	Power Supply
GND	Ground

Figure 3 : Input/output Timing Diagrams (crystal divide-by-16 mode).

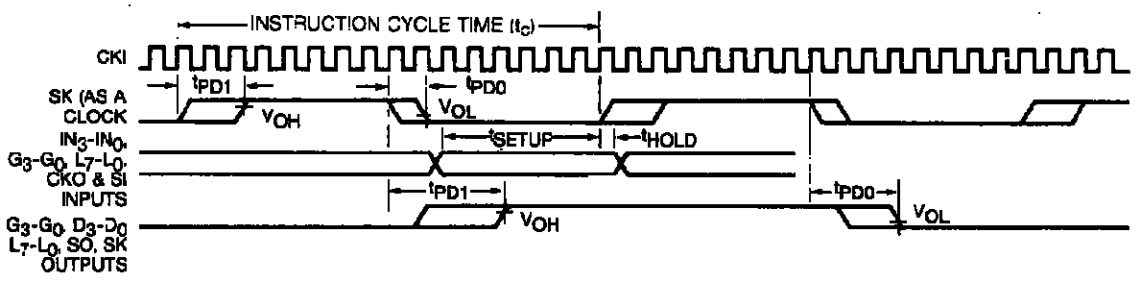
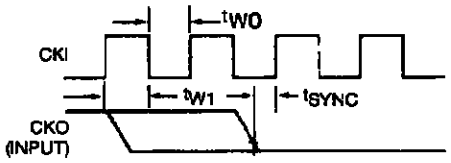


Figure 3a : Synchronization Timing.



FUNCTIONAL DESCRIPTION

A block diagram of the ETL9444 is given in figure 1. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1" (greater than 2 volts). When a bit is reset, it is a logic "0" (less than 0.8 volts).

All functional references to the ETL9444/L9445 also apply to the ETL9344/L9345.

PROGRAM MEMORY

Program Memory consists of a 2048 byte ROM. As can be seen by an examination of the ETL9444/L9445 instruction set, these words may be program instructions, program data or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID, and LQID instructions, ROM must often be thought of as being organized into 32 pages of 64 words each.

ROM addressing is accomplished by a 11-bit PC register. Its binary value selects one of the 2048 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 11-bit binary count value. Three levels of subroutine nesting are implemented by the 11-bit subroutine save registers, SA, SB, and SC ; providing a last-in, first-out (LIFO) hardware subroutine stack.

ROM instruction words are fetched, decoded and executed by the Instruction Decode, Control and Skip Logic circuitry.

DATA MEMORY

Data memory consists of a 512-bit RAM, organized as 8 data registers of 16 4-bit digits. RAM addressing is implemented by a 7-bit B register whose upper 3 bits (Br) select 1 of 8 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) is usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into or from the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the 7-bit contents of the operand field of these instructions. The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

INTERNAL LOGIC

The 4-bit A register (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Br and Bd portions of the B register, to load and input 4 bits of the 8-bit Q latch data, to input 4 bits of the 8-bit L I/O port data and to perform data exchanges with the SIO register.

A 4-bit adder performs the arithmetic and logic functions, storing its results in A. It also outputs a carry bit to the 1-bit C register, most often employed to indicate arithmetic overflow. The C register, in conjunction with the XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time. (See XAS instruction and EN register description, below).

Four general-purpose inputs, IN_3-IN_0, are provided.

The D register provides 4 general-purpose outputs and is used as the destination register for the 4-bit contents of Bd. The D outputs can be directly connected to the digits of a multiplexed LED display.

The G register contents are outputs to 4 general-purpose bidirectional I/O ports. G I/O ports can be directly connected to the digits of a multiplexed LED display.

The Q register is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are output to the L I/O ports when the L drivers are enabled under program control (See LEI instruction).

The 8 L drivers, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M. L I/O ports can be directly connected to the segments of a multiplexed LED display (using the LED Direct Drive output configuration option) with Q data being outputted to the Sa - Sg and decimal point segments of the display.

The SIO register functions as a 4-bit serial-in/serial-out shift register or as a binary counter depending on the contents of the EN register. (See EN register description, below). Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream, SIO may also be used to provide additional parallel I/O by connecting SO to external serial-in/parallel-out shift registers.

The XAS instruction copies C into the SKL latch. In the counter mode, SK is the output of SKL ; in the shift register mode, SK outputs SKL ANDed with the clock.

The EN register is an internal 4-bit register loaded under program control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN_3-EN_0).

1. The least significant bit of the enable register, EN_0, selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN_0 set, SIO is an asynchronous binary counter, decrementing its value by one upon each low-going pulse (”1” to ”0”) ocurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN_3. With EN_0 reset, SIO is a serial shift register shifting left each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time. (See 4 below). The SK output becomes a logic-controlled clock.
2. With EN_1 set the IN_1 input is enabled as an interrupt input. Immediately following an interrupt, EN_1 is reset to disable further interrupts.
3. With EN_2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN_2 disables the L drivers, placing the L I/O ports in a high-impedance input state.
4. EN_3, in conjunction with EN_0, affects the SO output. With EN_0 set (binary counter option selected) SO will output the value loaded into EN_3. With EN_0 reset (serial shift register option selected), setting EN_3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN_3 with the serial shift register option selected disables SO as the shift register output ; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to ”0”. The table below provides a summary of the modes associated with EN_3 and EN_0.

Enable Register Modes - Bits EN_3 and EN_0

EN_3	EN_0	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = Clock If SKL = 0, SK = 0
1	0	Shift Register	Input to Shift Register	Serial Out	If SKL = 1, SK = Clock If SKL = 0, SK = 0
0	1	Binary Counter	Input to Binary Counter	0	If SKL = 1, SK = 1 If SKL = 0, SK = 0
1	1	Binary Counter	Input to Binary Counter	1	If SKL = 1, SK = 1 If SKL = 0, SK = 0

INTERRUPT

The following features are associated with the IN1 interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

a. The interrupt, once acknowledged as explained below, pushes the next sequential program counter address (PC + 1) onto the stack, pushing in turn the contents of the other subroutine-save registers to the next lower level
(PC + 1 → SA → SB → SC). Any previous contents of SC are lost. The program counter is set to hex address 0FF (the last word of page 3) and EN_1 is reset.

b. An interrupt will be acknowledged only after the following conditions are met :
   1. EN_1 has been set.
   2. A low-going pulse (”1” to ”0”) at least two instruction cycles wide occurs on the IN_1 input.
   3. A currently executing instruction has been completed.

4. All successive transfer of control instructions and successive LBIs have been completed (e.g., if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed.

c. Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon popping of the stack. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address 0FF. At the end of the interrupt routine, a RET instruction is executed to "pop" the stack and return program control to the instruction following the original ASC. At this time, the skip logic is enabled and skips this instruction because of the previous ASC carry. Subroutines and LQID instructions should not be nested within the interrupt service routine, since their popping the stack will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.

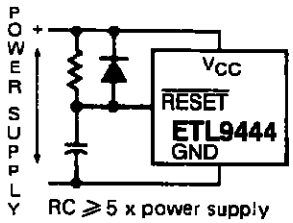
d. The first instruction of the interrupt routine at hex address 0FF must be a NOP.

e. A LEI instruction can be put immediately before the RET to re-enable interrupts.

INITIALIZATION

The Reset Logic will initialize (clear) the device upon power-up if the power supply rise time is less than 1ms and greater than 1µs. If the power supply rise time is greater than 1ms, the user use provide an external RC network and diode to the RESET pin as shown below. If the RC network is not used, the RESET pin must be pulled up to V_{CC} either by the internal load or by an external resistor (≥40kΩ) to V_{CC}. The RESET pin is configured as a Schmitt trigger input. Initialization will occur whenever a logic "0" is applied to the RESET input, provided it stays low for at least three instruction cycle times.

Power-up Clear Circuit.



RC ≥ 5 x power supply Rise time (R ≥ 40 k)

Power up clear circuit

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, and G registers are cleared. The SK output is enabled as a SYNC output, providing a pulse each instruction cycle time. Data Memory (RAM) is not cleared upon initialization. The first instruction at address 0 must be a CLRA.

OSCILLATOR

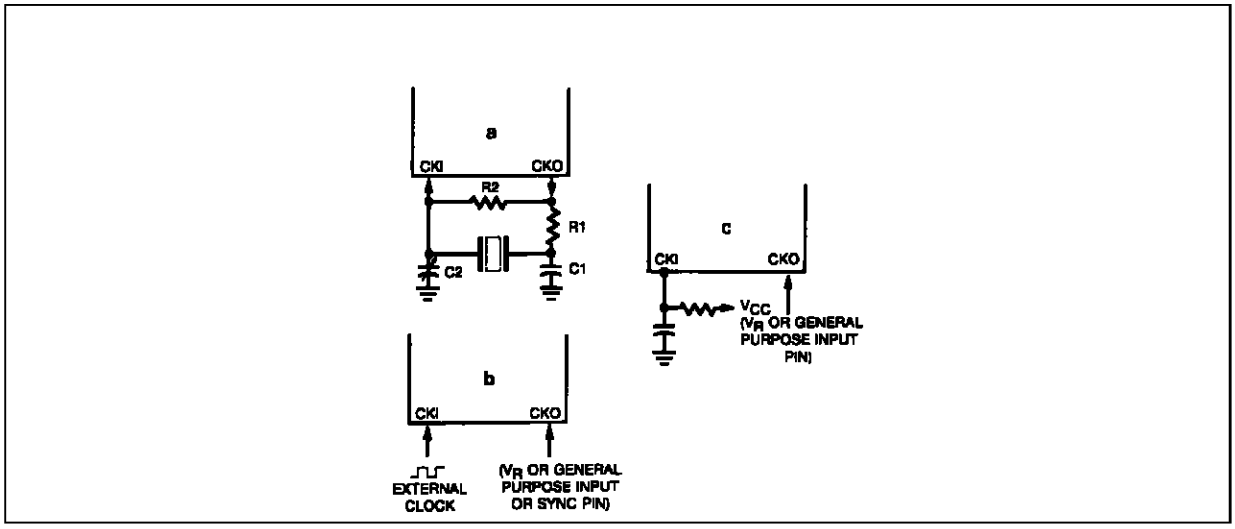
There are three basic clock oscillator configurations available as shown by figure 4.

a. Crystal Controlled Oscillator. CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency divided by 32 (optional by 16 or 8).

b. External Oscillator. CKI is an external clock input signal. The external frequency is divided by 32 (optional by 16 or 8) to give the instruction cycle time. CKO is now available to be used as the RAM power supply (V_R), as a general purpose input, or as a SYNC input.

c. RC Controlled Oscillator. CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is available as the RAM power supply (V_R) or as a general purpose input.

Figure 4 : ETL9444/L9445 Oscillator.



CRYSTAL OSCILLATOR

Crystal Value	Component Values			
	R1 (Ω)	**R2** (Ω)	**C1** (pF)	**C2** (pF)
455kHz	4.7k	1M	220	220
2.097MHz	1k	1M	30	6-36

RC CONTROLLED OSCILLATOR

R (kΩ)	**C** (pF)	Instruction Cycle Time (μs)
51	100	19 ± 15%
82	56	19 ± 13%

Note : 200kΩ ≥ R ≥ 25kΩ
360pF ≥ C ≥ 50pF

CKO PIN OPTIONS

In a crystal controlled oscillator system, CKO is used as an output to the crystal network. As an option CKO can be a SYNC input as described above. As another option CKO can be a general purpose input, read into bit 2 of A (accumulator) upon execution of an INIL instruction. As another option, CKO can be a RAM power supply pin (V_R), allowing its connection to a standby/backup power supply to maintain the integrity of RAM data with minimum power drain when the main supply is inoperative or shut down to conserve power. Using either option is appropriate in applications where the ETL9444/L9445 system timing configuration does not require use of the CKO pin.

I/O OPTIONS

ETL9444/L9445 outputs have the following optional configurations, illustrated in figure 5.

a. Standard - an enhancement mode device to ground in con junction with a depletion-mode device to V_{CC}, compatible with LSTTL and CMOS input requirements. Available on SO, SK, and all D and G outputs.

b. Open-Drain - an enhancement-mode device to ground only, allowing external pull-up as required by the user's application. Available on SO, SK, and all D and G outputs.

c. Push-Pull - An enhancement-mode device to ground in conjunction with a depletion-mode device paralleled by an enhancement-mode device to V_{CC}. This configuration has been provided to allow for fast rise and fall times when driving capacitive loads. Available on SO and SK outputs only.

d. Standard L - same as a., but may be disabled. Available on L outputs only.

e. Open Drain L - same as b., but may be disabled. Available on L outputs only.

f. LED Direct Drive - an enhancement-mode device to ground and to V_{CC}, meeting the typical current sourcing requirements of the segments of an LED display. The sourcing device is clamped to limit current flow. These devices may be turned off under program control (See Functional Description, EN Register), placing the outputs in a high-impedance state to provide required LED

segment blanking for a multiplexed display. Available on L outputs only.

g. TRI-STATE® Push-Pull - an enhancement-mode device to ground and V_{CC}. These outputs are TRI-STATE outputs, allowing for connection of these outputs to a data bus shared by other bus drivers. Available on L outputs only.

ETL9444, L9445 inputs have the following optional configurations :

h. An on-chip depletion load device to V_{CC}.

i. A Hi-Z input which must be driven to a "1" or "0" by external components.

The above input and output configurations share common enhancement-mode and depletion-mode devices. Specifically, all configurations use one or more of six devices (numbered 1-6, respectively). Minimum and maximum current (I_{OUT} and V_{OUT} curves are given in figure 6 for each of these devices to allow the designer to effectively use these I/O configurations in designing a system.

The SO, SK outputs can be configured as shown in **a**., **b**., or **c**. The D and G outputs can be configured as shown in a. or b. Note that when inputting data to the G ports, the G outputs should be set to "1". The L outputs can be configured as in **d**., **e**., **f**. or **g**.

An important point to remember if using configuration **d**. or **f**. with the L drivers is that even when the L drivers are disabled, the depletion load device will source a small amount of current (see figure 6, device 2) ; however, when the L-lines are used as inputs, the disabled depletion device can not be relied on to source sufficient current to pull an input to logic "1".

RAM KEEP-ALIVE OPTION

Selecting CKO as the RAM power supply (V_R) allows the user to shut off the chip power supply (V_{CC}) and maintain data in the RAM.

To insure that RAM data integrity is maintained, the following conditions must be met :

1. $\overline{\text{RESET}}$ must go low before V_{CC} goes low during power off ; V_{CC} must go high before $\overline{\text{RESET}}$ goes high on power-up.
2. V_R must be within the operating range of the chip, and equal to $V_{CC} \pm 1V$ during normal operation.
3. V_R must be $\geq 3.3V$ with V_{CC} off.

ETL9445

If the ETL9444 ls bonded as a 24-pin device, it becomes the ETL9445, illustrated in figure 2, ETL9444 Connection Diagrams. Note that the ETL9445 does not contain the four general purpose IN inputs (IN_3-IN_0). Use of this option precludes, of course, use of the IN options and the interrupt feature, which uses IN_1. All other options are available for the ETL9445.

Figure 5 : Output Configurations.

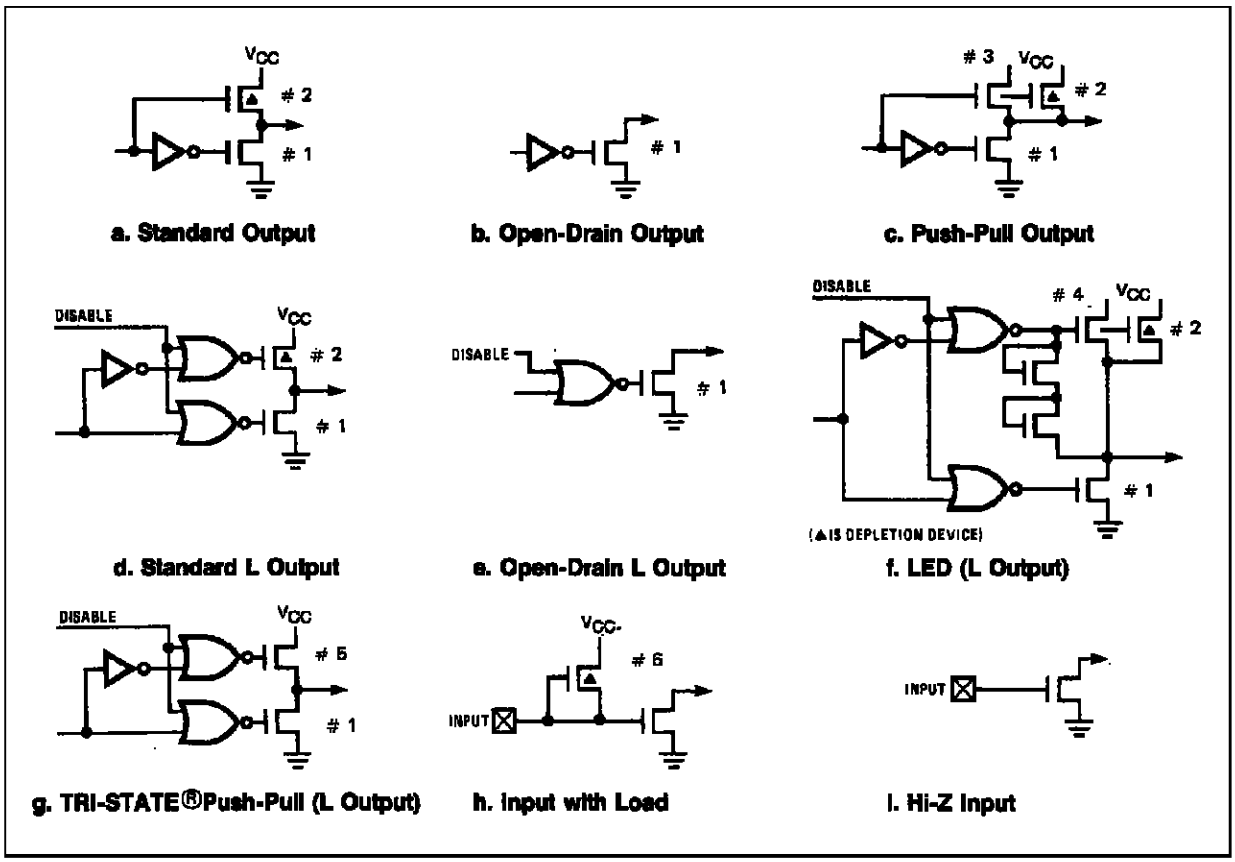


Figure 6 : ETL9444/L9445 Input/output Characteristics.

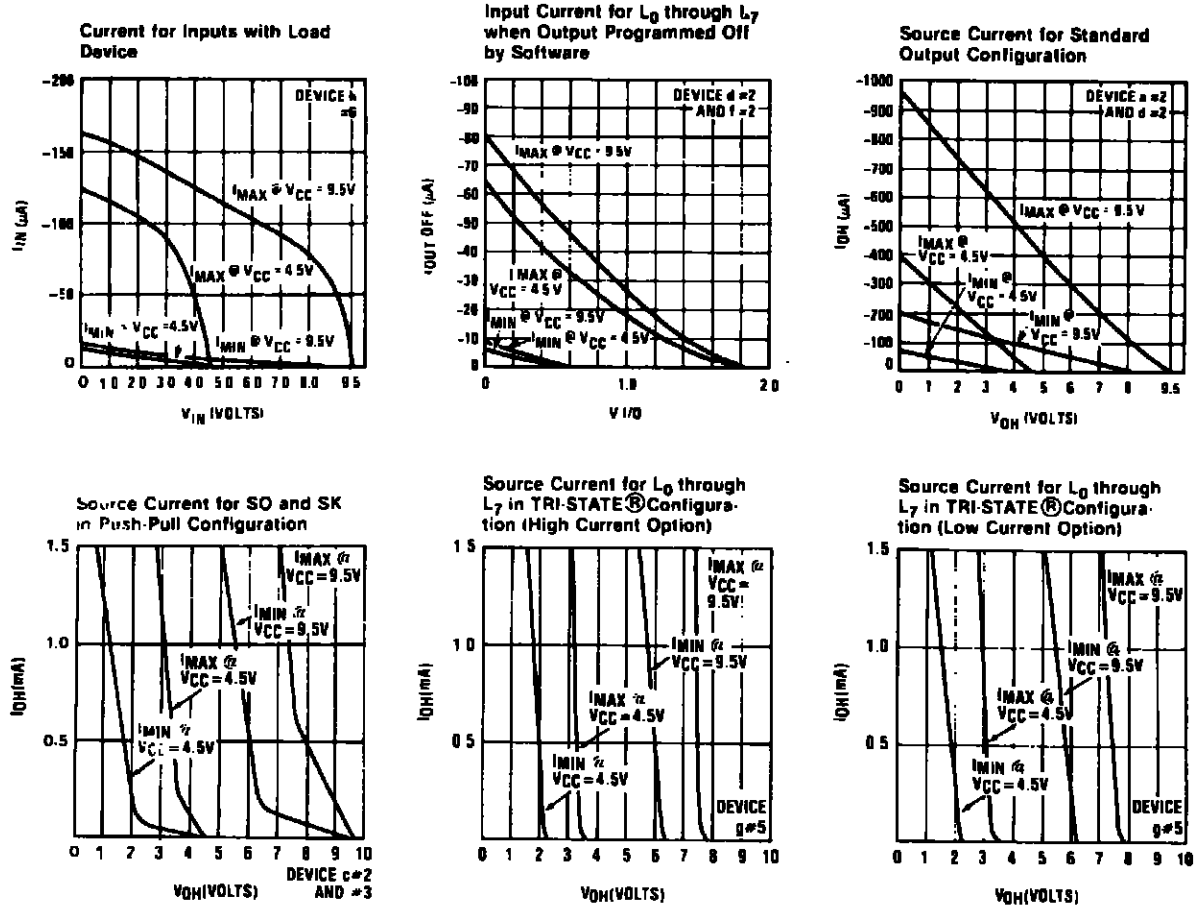


Figure 6a : ETL9444/L9445 Input/output Characteristics.

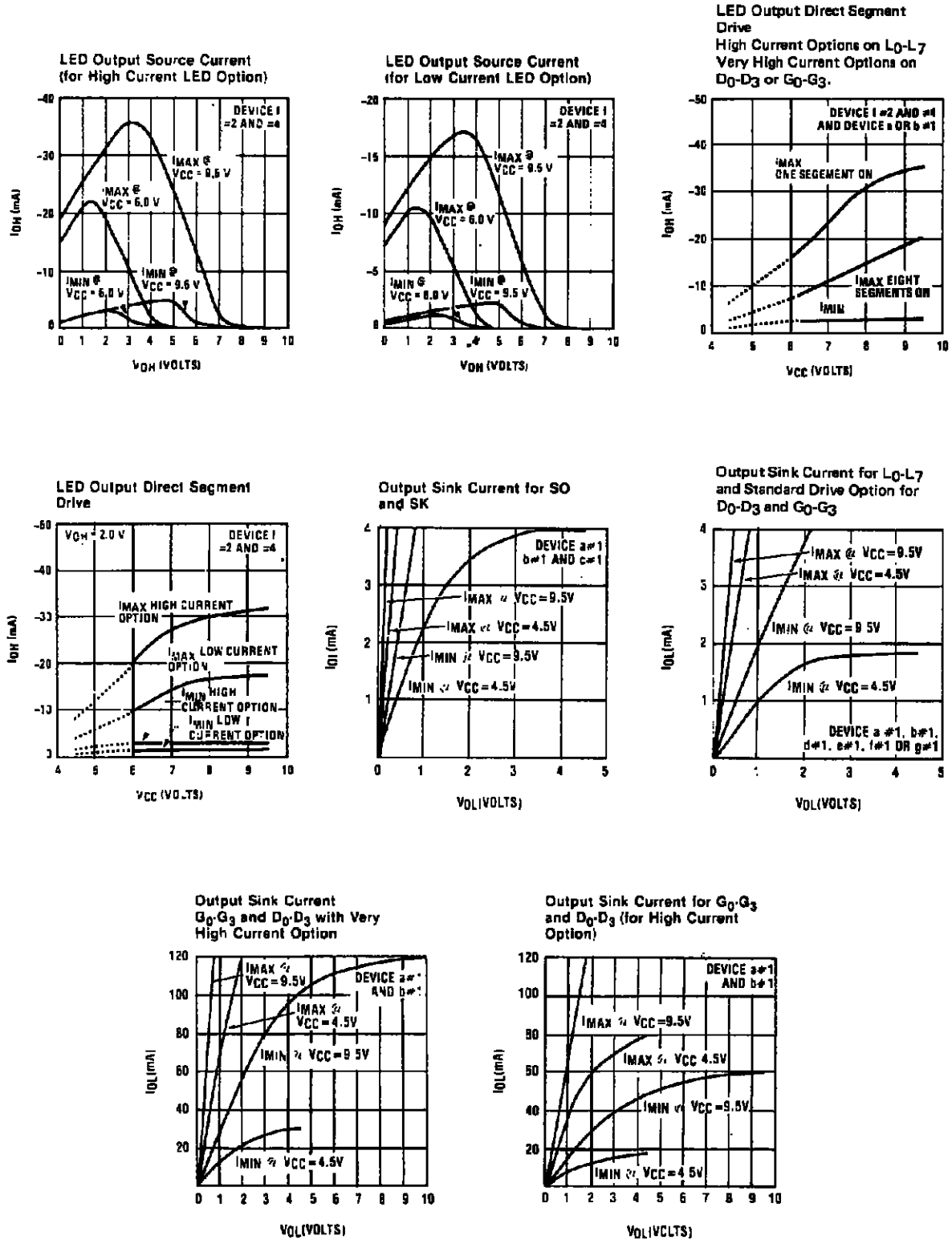
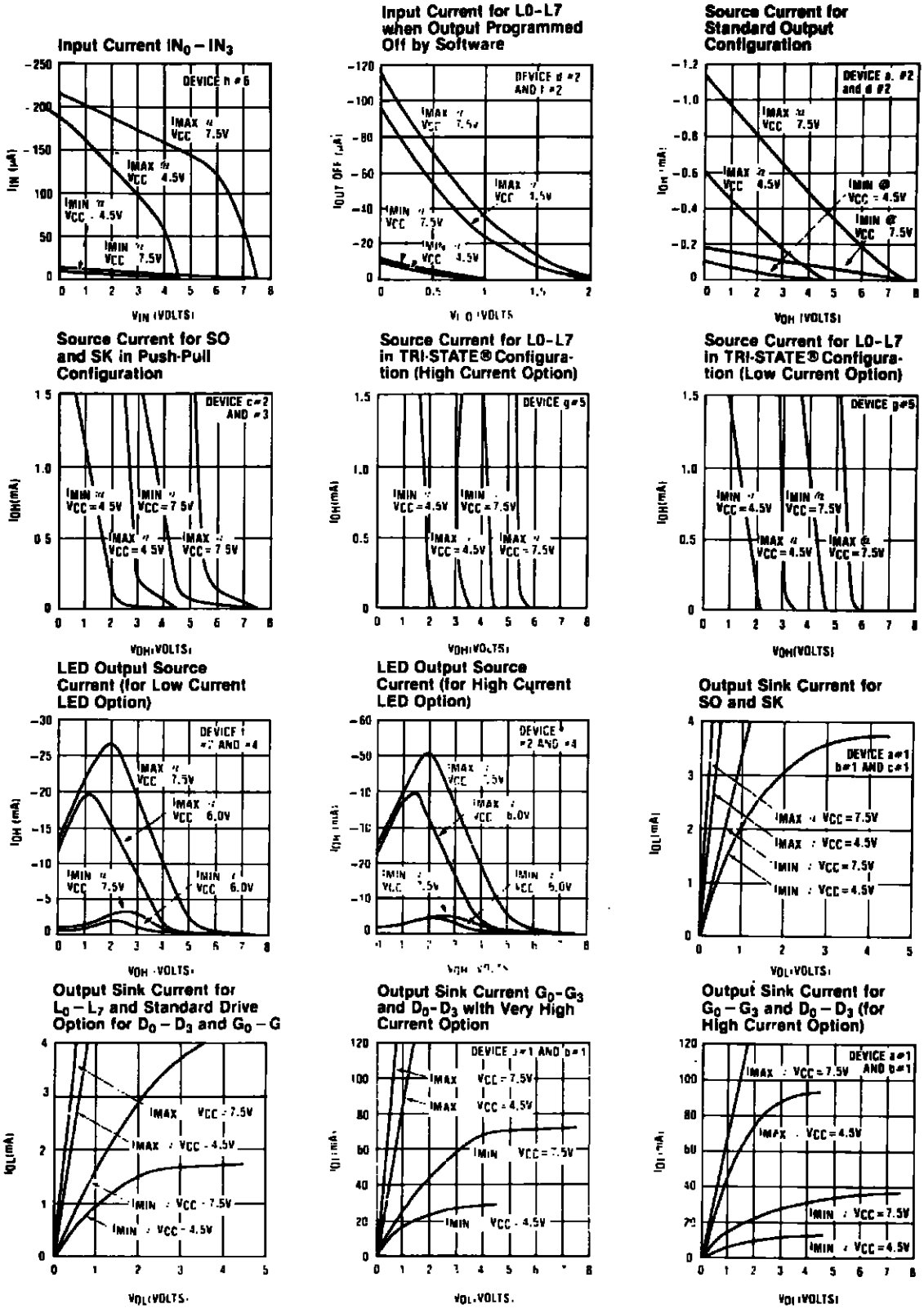


Figure 6b : ETL9344/L9345 Input/output Characteristics.



ETL9444/L9445, ETL9344/L9345 INSTRUCTION SET

Table 1 is a symbol table providing internal architecture, instruction operand and operational symbols used in the instruction set table.

Table 2 provides the mnemonic, operand, machine code, data flow, skip conditions, and description associated with each instruction in the ETL9444/L9445 instruction set.

Table 1 : ETL9444/9445 ETL9344/9345 Instruction Set Table Symbols.

INTERNAL ARCHITECTURE SYMBOLS

Symbol	Definition
A	4-bit Accumulator
B	7-bit RAM Address Register
Br	Upper 3 Bits of B (register address)
Bd	Lower 4 Bits of B (digit address)
C	1-bit Carry Register
D	4-bit Data Output Port
EN	4-bit Enable Register
G	4-bit Register to Latch Data for G I/O Port
IL	Two 1-bit latches associated with the IN_3 or IN_0 inputs.
IN	4-bit Input Port
L	8-bit TRI-STATE® I/O Port
M	4-bit contents of RAM memory pointed to by B register.
PC	11-bit ROM Address Register (program counter)
Q	8-bit Register to Latch Data for L I/O Port
SA	11-bit Subroutine Save Register A
SB	11-bit Subroutine Save Register B
SC	11-bit Subroutine Save Register C
SIO	4-bit Shift Register and Counter
SK	Logic-controlled Clock Output

INSTRUCTION OPERAND SYMBOLS

Symbol	Definition
d	4-bit Operand Field, 0-15 Binary (RAM digit select)
r	3-bit Operand Field, 0-7 Binary (RAM register select)
a	11-bit Operand Field, 0-2047 Binary (ROM address)
y	4-bit Operand Field, 0-15 Binary (immediate data)
RAM(s)	Contents of RAM location addressed by s.
ROM(t)	Contents of ROM location addressed by t.

OPERATIONAL SYMBOLS

Symbol	Definition
+	Plus
-	Minus
→	Replaces
↔	Is exchanged with.
=	Is equal to.
$\overline{A}$	The one's complement of A.
⊕	Exclusive-OR
:	Range of Values

Table 2 : ETL9444/L9445 Instruction Set.

ARITHMETIC INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
ASC		30	|0 0 1 1|0 0 0 0|	A + C + RAM(B) → A Carry → C	Carry	Add with Carry Skip on Carry
ADD		31	|0 0 1 1|0 0 0 1|	A + RAM(B) → A	None	Add RAM to A
ADT		4A	|0 1 0 0|1 0 1 0|	A + 10_{10} → A	None	Add Ten to A
AISC	y	5-	|0 1 0 1| y |	A + y → A	Carry	Add Immediate Skip on Carry (y ≠ 0)
CASC		10	|0 0 0 1|0 0 0 0|	$\overline{A}$ + RAM(B) + C → A Carry → C	Carry	Complement and Add with Carry, Skip on Carry
CLRA		00	|0 0 0 0|0 0 0 0|	0 → A	None	Clear A
COMP		40	|0 1 0 0|0 0 0 0|	$\overline{A}$ → A	None	Ones Complement of A to A
NOP		44	|0 1 0 0|0 1 0 0|	None	None	No Operation
RC		32	|0 0 1 1|0 0 1 0|	"0" → C	None	Reset C
SC		22	|0 0 1 0|0 0 1 0|	"1" → C	None	Set C
XOR		02	|0 0 0 0|0 0 1 0|	A ⊕ RAM(B) → A	None	Exclusive-OR Ram with A

TRANSFER OF CONTROL INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
JID		FF	|1 1 1 1|1 1 1 1|	ROM ($PC_{10:8}$ A, M) → $PC_{7:0}$	None	Jump Indirect (note 3)
JMP	a	6–	|0 1 1 0|0| $a_{10:8}$ | | $a_{7:0}$ |	A → PC	None	Jump
JP	a		|1| $a_{6:0}$ | (pages 2, 3 only) or |1 1| $a_{5:0}$ | (all other pages)	A → $PC_{6:0}$ A → $PC_{5:0}$	None	Jump within Page (note 4)
JSRP	a		|1 0| $a_{5:0}$ |	PC + 1 → SA → SB → SC 00010 → $PC_{10:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (note 5)
JSR	a	6–	|0 1 1 0|1| $a_{10:8}$ | | $a_{7:0}$ |	PC + 1 → SA → SB → SC a → PC	None	Jump to Subroutine
RET		48	|0 1 0 0|1 0 0 0|	SC → SB → SA → PC	None	Return from Subroutine
RETSK		49	|0 1 0 0|1 0 0 1|	SC → SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip

MEMORY REFERENCE INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
CAMQ		33 3C	|0 0 1 1|0 0 1 1| |0 0 1 1|1 1 0 0|	$A \rightarrow Q_{7:4}$ RAM (B) $\rightarrow Q_{3:0}$	None	Copy A, RAM to Q
CQMA		33 2C	|0 0 1 1|0 0 1 1| |0 0 1 0|1 1 0 0|	$Q_{7:4} \rightarrow$ RAM(B) $Q_{3:0} \rightarrow A$	None	Copy Q to RAM A
LD	r	–5	| 0 0| r|0 1 0 1| (r = 0:3)	RAM(B) $\rightarrow$ A Br $\oplus$ r $\rightarrow$ Br	None	Load RAM into A, Exclusive-OR Br with r
LDD	r.d	23	|0 0 1 0|0 0 1 1| |0 | r | d |	RAM(r.d) $\rightarrow$ A	None	Load A with RAM pointed to directly by r.d.
LQID		BF	|1 0 1 1|1 1 1 1|	ROM ($PC_{10:8}$A.M) $\rightarrow$ Q SB $\rightarrow$ SC	None	Load Q Indirect (note 3)
RMB	0 1 2 3	4C 45 42 43	|0 1 0 0|1 1 0 0| |0 1 0 0|0 1 0 1| |0 1 0 0|0 0 1 0| |0 1 0 0|0 0 1 1|	0 $\rightarrow$ RAM $(B)_0$ 0 $\rightarrow$ RAM $(B)_1$ 0 $\rightarrow$ RAM $(B)_2$ 0 $\rightarrow$ RAM $(B)_3$	None	Reset RAM Bit
SMB	0 1 2 3	4D 47 46 4B	|0 1 0 0|1 1 0 1| |0 1 0 0|1 1 0 1| |0 1 0 0|0 1 1 0| |0 1 0 0|1 0 1 1|	1 $\rightarrow$ RAM $(B)_0$ 1 $\rightarrow$ RAM $(B)_1$ 1 $\rightarrow$ RAM $(B)_2$ 1 $\rightarrow$ RAM $(B)_3$	None	Set RAM Bit
STII	y	7–	|0 1 1 1| y |	y $\rightarrow$ RAM (B) Bd + 1 $\rightarrow$ Bd	None	Store Memory Immediate and Increment Bd
X	r	–6	|0 0| r |0 1 1 0| (r = 0:3)	RAM (B) $\leftrightarrow$ A Br $\oplus$ r $\rightarrow$ Br	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	r.d	23	|0 0 1 0|0 0 1 1| |1 | r | d |	RAM (r.d) $\leftrightarrow$ A	None	Exchange A with RAM pointed to directly by r.d.
XDS	r	–7	|0 0| r |0 1 1 1| (r = 0:3)	RAM (B) $\leftrightarrow$ A Bd – 1 $\rightarrow$ Bd Br $\oplus$ r $\rightarrow$ Br	Bd Decrements Past 0	Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r
XIS	r	–4	|0 0| r |0 1 0 0| (r = 0:3)	RAM (B) $\leftrightarrow$ A Bd + 1 $\rightarrow$ Bd Br $\oplus$ r $\rightarrow$ Br	Bd Increments Past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r

REGISTER REFERENCE INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
CAB		50	|0 1 0 1|0 0 0 0|	A → Bd	None	Copy A to Bd
CBA		4E	|0 1 0 0|1 1 1 0|	Bd → A	None	Copy Bd to A
LBI	r.d	33	|0 0| r | (d-1) | (r = 0:3) (d = 0.9:15) or |0 0 1 1|0 0 1 1| | 1 | r | d | (any r, any d)	r.d → B	Skip until not a LBI	Load B Immediate with r.d (note 6)
LEI	y	33 6–	|0 0 1 1|0 0 0 1| |0 1 1 0| y |	y → EN	None	Load EN Immediate (note 7)
XABR		12	|0 0 0 1|0 0 1 0|	A → Br (0 → A_3)	None	Exchange A with Br

TEST INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
SKC		20	|0 0 1 0|0 0 0 0|		C = "1"	Skip if C is true.
SKE		21	|0 0 1 0|0 0 0 1|		A = RAM(B)	Skip if A Equals RAM
SKGZ		33 21	|0 0 1 1|0 0 1 1| |0 0 1 0|0 0 0 1|		$G_{3:0}$ = 0	Skip if G is zero (all 4 bits).
SKGBZ	 0 1 2 3	33 01 11 03 13	|0 0 1 1|0 0 1 1| 1st Byte |0 0 0 0|0 0 0 1| |0 0 0 1|0 0 0 1| |0 0 0 0|0 0 1 1| |0 0 0 1|0 0 1 1| 2nd Byte	 G_0 = 0 G_1 = 0 G_2 = 0 G_3 = 0	Skip if G Bit is zero.
SKMBZ	0 1 2 3	01 11 03 13	|0 0 0 0|0 0 0 1| |0 0 0 1|0 0 0 1| |0 0 0 0|0 0 1 1| |0 0 0 1|0 0 1 1|		$RAM(B)_0$ = 0 $RAM(B)_1$ = 0 $RAM(B)_2$ = 0 $RAM(B)_3$ = 0	Skip if RAM bit is zero.
SKT		41	|0 1 0 0|0 0 0 1|		A time-base counter carry has occured since last test.	Skip on Timer (note 3)

INPUT/OUTPUT INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
ING		33 2A	|0 0 1 1|0 0 1 1| |0 0 1 0|1 0 1 0|	G → A	None	Input G Ports to A
ININ		33 28	|0 0 1 1|0 0 1 1| |0 0 1 0|1 0 0 0|	IN → A	None	Input IN Inputs to A (note 2)
INIL		33 29	|0 0 1 1|0 0 1 1| |0 0 1 0|1 0 0 1|	IL_3, CKO, "0", IL_0 → A	None	Input IL Latches to A (note 3)
INL		33 2E	|0 0 1 1|0 0 1 1| |0 0 1 0|1 1 1 0|	$L_{7:4}$ → RAM(B) $L_{3:0}$ → A	None	Input L Ports to RAM, A
OBD		33 3E	|0 0 1 1|0 0 1 1| |0 0 1 1|1 1 1 0|	Bd → D	None	Output Bd to D Outputs
OGI	y	33 5–	|0 0 1 1|0 0 1 1| |0 1 0 1| y |	y → G	None	Output to G Ports Immediate
OMG		33 3A	|0 0 1 1|0 0 1 1| |0 0 1 1|1 0 1 0|	RAM(B) → G	None	Output RAM to G Ports
XAS		4F	|0 1 0 0|1 1 1 1|	A ↔ SIO, C → SKL	None	Exchange A with SIO (note 3)

Notes : 1.All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.

2.The ININ instruction is not available on the 24-pin ETL9445 or ETL9345 since these devices do not contain the IN inputs.

3.For additional information on the operation of the XAS, JID, LQUID, INIL and SKT instructions, see below.

4.The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

5.A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3, JSRP may not jump to the last word in page 2.

6.LBI is a single-byte instruction if d = 0, 9, 10, 11, 12, 13, 14 or 15. The machine code for the lower 4 bits equals the binary value of the "d" data minus 1, e.g., to load the lower four bits of B (Bd) with the value 9 (1001_2), the lower 4 bits of the LBI instruction equal 8 (1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111_2).

7.Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (See Functional Description, EN Register).

The following information is provided to assist the user in understanding the operation of several unique instructions and to provide notes useful to programmers in writing ETL9444/L9445 programs.

XAS INSTRUCTION

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output. (See Functional Description, EN Register, above). If SIO is selected as a shift register, an XAS instruction must be performed once every 4 instruction cycles to effect a continuous data stream.

JID INSTRUCTION

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the contents of ROM addressed by the 11-bit word, $PC_{10:8}$ A, M. PC_{10}, PC_9 and PC_8 are not affected by this instruction.

Note that JID requires 2 instruction cycles to execute.

INIL INSTRUCTION

INIL (Input IL Latches to A) inputs 2 latches, IL_3 and IL_0 (see figure 7) and CKO into A. The IL_3 and IL_0 latches are set if a low-going pulse ("1" to "0") has

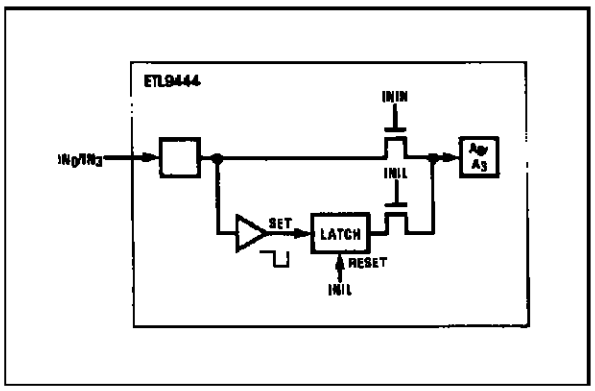
occurred on the IN_3 and IN_0 inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction times. Execution of an INIL inputs IL_3 and IL_0 into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN_3 and IN_0 lines. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO into A2. If CKO has not been so programmed, a "1" will be placed in A2. A "0" is always placed in A1 upon the execution of an INIL. The general purpose inputs IN_3-IN_0 are input to A upon execution of an ININ instruction. (see table 2, ININ instruction). INIL is useful in recognizing pulses of short duration or pulses which occur too often to be read conveniently by an ININ instruction.

Note : IL latches are not cleared on reset : IL_3 and IL_0 not input on ETL9444/L9445.

LQID INSTRUCTION

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 11-bit word PC_{10}, PC_9, PC_8, A, M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack ($PC + 1 \rightarrow SA \rightarrow SB \rightarrow SC$) and replaces the least significant 8 bits of PC as follows : $A – PC_{7:4}$, RAM $(B) \rightarrow PC_{3:0}$, leaving PC_{10}, PC_9 and PC_8 unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" ($SC \rightarrow SB \rightarrow SA \rightarrow PC$), restoring the saved value of PC to continue sequential program execution. Since LQID pushes $SB \rightarrow SC$, the previous contents of SC are lost. Also, when LQID pops the stack, the previously pushed contents of SB are left in SC. The net result is that the contents of SB are placed in SC ($SB \rightarrow SC$). Note that LQID takes two instruction cycle times to execute.

Figure 7 : INIL Hardware Implementation.



SKT INSTRUCTION

The SKT (Skip On Timer) instruction tests the state of an internal 10-bit time-base counter. This counter divides the instruction cycle clock, frequency by 1024 and provides a latched indication of counter overflow. The SKT instruction tests this latch, executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction, therefore, allow the ETL9344/L9345 to generate its own time-base for real-time processing rather than relying on an external input signal.

For example, using a 2.097MHz crystal as the time-base to the clock generator, the instruction cycle clock frequency will be 65kHz (crystal frequency ÷ 32) and the binary counter output pulse frequency will be 64Hz. For time-of-day or similar real-time processing, the SKT instruction can call a routine which increments a "seconds" counter every 64 ticks.

INSTRUCTION SET NOTES

a. The first word of a ETL9444/L9445 program (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, one instruction cycle time is devoted to skipping each byte of the skipped instruction. Thus all program paths except JID and LQID take the same number of cycle times whether instructions are skipped or executed. JID and LQID instructions take 2 cycles if executed and 1 cycle if skipped.

c. The ROM is organized into 32 pages of 64 words each. The Program Counter is an 11-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID or LQID instruction is located in the last word of a page, the instruction operates as if it were in the next page. For example : a JP located in the last work of a page will jump to a location in the next page. Also, a LQID or JID located in the last word of page 3, 7, 11, 15, 19, 23 or 27 will access data in the next group of four pages.

OPTION LIST

The ETL9444/L9445 mask programmable options are assigned numbers which correspond with the ETL9444 pins.

The following is a list of ETL9444 options. When specifying ETL9445 chip, Options 9, 10, 19, and 20 must all be set to zero. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Option 1 = 0 : Ground Pin - no options available

Option 2 : CKO Output
- = 0 : clock generator output to crystal/resonator (0 not allowable value if option 3 = 3)
- = 1 : pin is RAM power supply (V_R) input
- = 2 : general purpose input. load device to V_{CC}
- = 3 : general purpose input, Hi-Z

Option 3 : CKI Input
- = 0 : oscillator input divided by 32 (2MHz max.)
- = 1 : oscillator input divided by 16 (1MHz max.)
- = 2 : oscillator input divided by 8 (500kHz max.)
- = 3 : single-pin RC controlled oscillator divided by 4
- = 4 : oscillator input divided by 4 (Schmitt)

Option 4 : RESET Input
- = 0 : load device to V_{CC}
- = 1 : Hi-Z input

Option 5 : L_7 Driver
- = 0 : Standard output
- = 1 : Open-drain output
- = 2 : High current LED direct segment drive output
- = 3 : High current TRI-STATE® push-pull output
- = 4 : Low-current LED direct segment drive output
- = 5 : Low-current TRI-STATE® push-pull output

Option 6 : L_6 Driver
same as Option 5

Option 7 : L_5 Driver
same as Option 5

Option 8 : L_4 Driver
same as Option 5

Option 9 : IN_1 Input
- = 0 : load device to V_{CC}
- = 1 : Hi-Z input

Option 10 : IN_2 Input
same as Option 9

Option 11 : V_{CC} pin
- = 0 : 4.5V to 6.3V operation
- = 1 : 4.5V to 9.5V operation

Option 12 : L_3 Driver
same as Option 5

Option 14 : L_2 Driver
same as Option 5

Option 14 : L_1 Driver
same as Option 5

Option 15 : L_0 Driver
same as Option 5

Option 16 : SI Input
same as Option 9

Option 17 : SO Driver
- = 0 : standard output
- = 1 : open-drain output
- = 2 : push-pull output

Option 18 : SK Driver
same as Option 17

Option 19 : IN_0 Input
same as Option 9

Option 20 : IN_3 Input
same as Option 9

Option 21 : G_0 I/O Port
- = 0 : very-high current standard output
- = 1 : very-high current open-drain output
- = 2 : high current standard output
- = 3 : high current open-drain output
- = 4 : standard LSTTL output (fanout = 1)
- = 5 : open-drain LSTTL output (fanout = 1)

Option 22 : G_1 I/O Port
same as Option 21

Option 23 : G_2 I/O Port
same as Option 21

Option 24 : G_3 I/O Port
same as Option 21

Option 25 : D_3 Output
same as Option 21

Option 26 : D_2 Output
same as Option 21

Option 27 : D_1 Output
same as Option 21

Option 28 : D_0 Output
same as Option 21

Option 29 : L Input Levels
- = 0 : standard TTL input levels ("0" = 0.8V, "1" = 2.0V)

= 1 : higher voltage input levels
("0" = 1.2V, "1" = 3.6V)

Option 30 : IN Input Levels
same as Option 29

Option 31 : G Input Levels
same as Option 29

Option 32 : SI Input Levels
same as Option 29

Option 33 : RESET Input
= 0 : Schmitt trigger input
= 1 : standard TTL input levels
= 2 : higher voltage input levels

Option 34 : CKO Input Levels (CKO = input Option 2 = 2.3)
same as Option 29

Option 35 COP Bonding
= 0 : ETL9444 (28-pin device)
= 1 : ETL9445 (24-pin device)
= 2 : both 28 and 24 pin versions

TEST MODE (Non-Standard Operation)

The SO output has been configured to provide for standard test procedures for the custom-programmed ETL9444. With SO forced to logic "1", two test modes are provided, depending upon the value of SI :

a. RAM and Internal Logic Test Mode (SI = 1)

b. ROM Test Mode (SI = 0)

These special test modes should not be employed by the user ; they are intended for manufacturing test only.

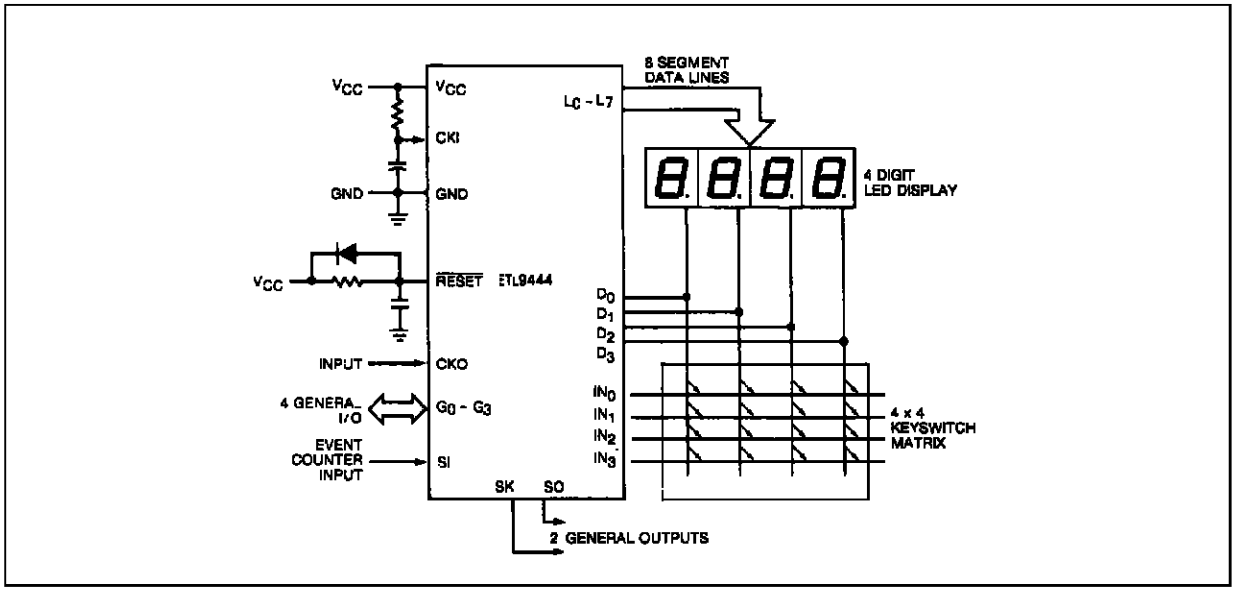
APPLICATION EXAMPLE :

ETL9444 General Controller

Figure 8 shows and interconnect diagram for a ETL9444 used as a general controller. Operation of the system is as follows :

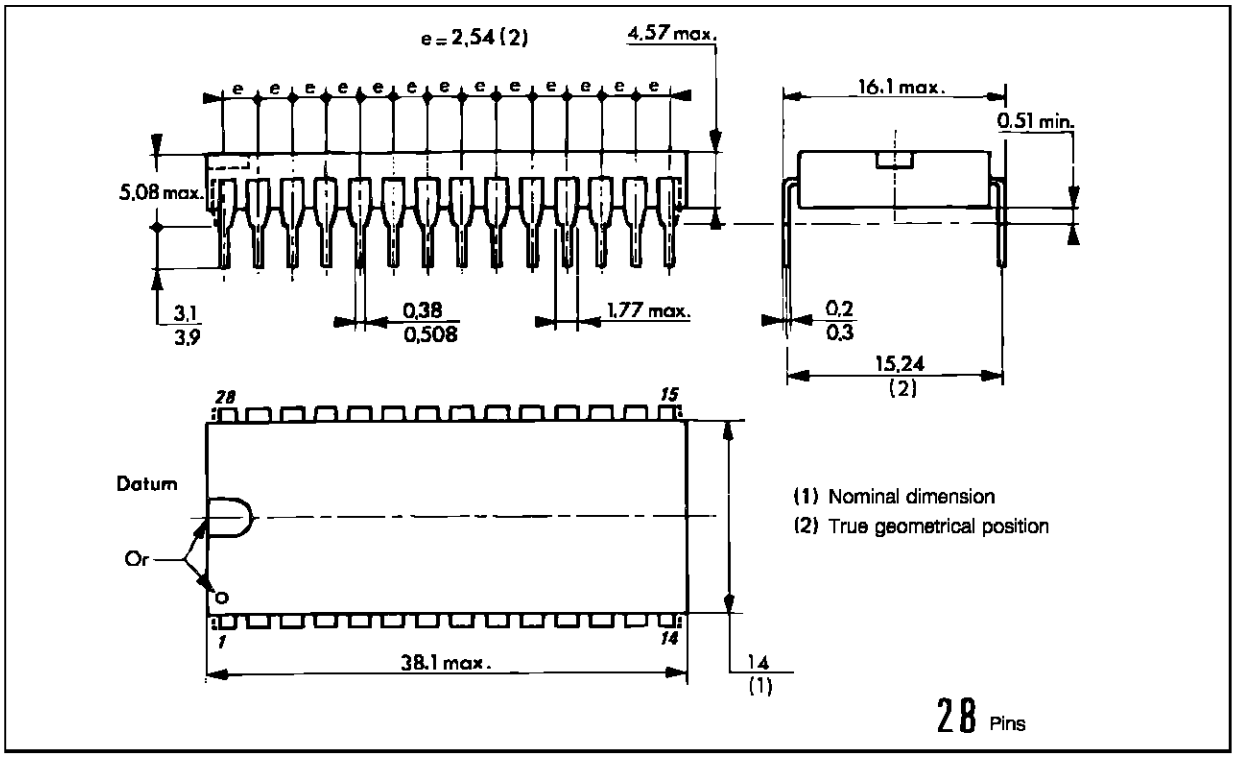
1. The L_7-L_0 outputs are configured as LED Direct Drive outputs, allowing direct connection to the segments of the display.
2. The D_3-D_0 outputs drive the digits of the multiplexed display directly and scan the columns of the 4 x 4 keyboard matrix.
3. The IN_3-IN_0 inputs are used to input the 4 rows of the keyboard matrix. Reading the IN lines in conjunction with the current value of the D outputs allows detection, debouncing, and decoding of any one of the 16 keyswitches.
4. CKI is configured as a single-pin oscillator input allowing system timing to be controlled by a single-pin RC network. CKO is therefore available for use as a general-purpose input.
5. SI is selected as the input to a binary counter input. With SIO used as a binary counter, SO and SK can be used as general purpose outputs.
6. The 4 bidirectional G I/O ports (G_3-G_{-0}) are available for use as required by the user's application.
7. Normal reset operation is selected.

Figure 8 : ETL9444 Keyboard/display Interface.

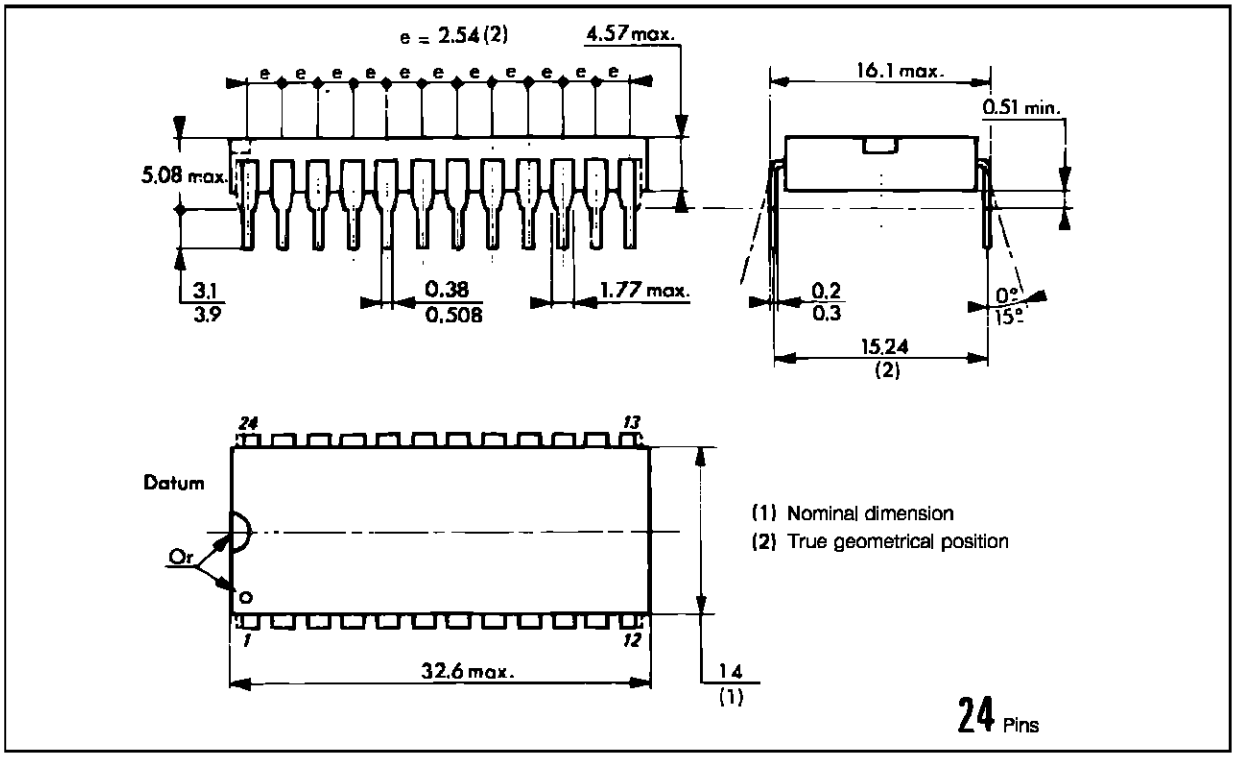


PHYSICAL DIMENSIONS

28–PINS – PLASTIC PACKAGE



24–PINS – PLASTIC PACKAGE



Information furnished is believed to be accurate and reliable. However, SGS-THOMSON Microelectronics assumes no responsability for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of SGS-THOMSON Microelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied.
SGS-THOMSON Microelectronics products are not authorized for use as critical components in life support devices or systems without the express written approval of SGS-THOMSON Microelectronics.

© 1994 SGS-THOMSON Microelectronics - All rights reserved.

Purchase of I^2C Components by SGS-THOMSON Microelectronics conveys a license under the Philips I^2C Patent. Rights to use these components in an I^2C system is granted provided that the system conforms to the I^2C Standard Specification as defined by Philips.

SGS-THOMSON Microelectronics Group of Companies

Australia - Brazil - France - Germany - Hong Kong - Italy - Japan - Korea - Malaysia - Malta - Morocco The Netherlands - Singapore - Spain
Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.