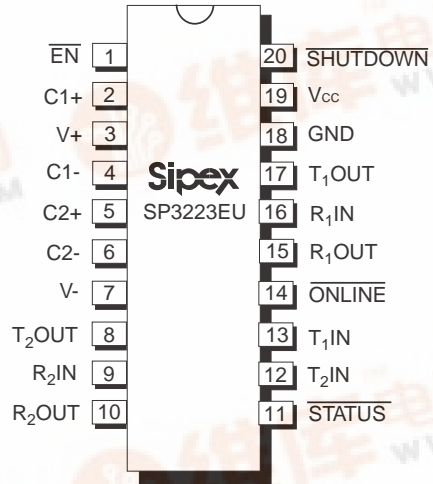




# SP3223EU/3243EU

## High Speed Intelligent +3.0V to +5.5V RS-232 Transceivers

- Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
- Interoperable with EIA/TIA-232 and adheres to EIA/TIA-562 down to a +2.7V power source
- **AUTO ON-LINE**<sup>®</sup> circuitry automatically wakes up from a 1 $\mu$ A shutdown
- Regulated Charge Pump Yields Stable RS-232 Outputs Regardless of V<sub>CC</sub> Variations
- Enhanced ESD Specifications:
  - ±15kV Human Body Model
  - ±15kV IEC1000-4-2 Air Discharge
  - ±8kV IEC1000-4-2 Contact Discharge
- 1000 Kbps minimum transmission rate
- Ideal for High Speed RS-232 Applications



Now Available in Lead Free Packaging

### DESCRIPTION

The SP3223EU and 3243EU products are RS-232 transceiver solutions intended for portable or hand-held applications such as notebook and palmtop computers. The "U" series is based on Sipex's SP3223E/3243E series and has been enhanced for high speed. The data rate is improved to 1000kbps, easily meeting the demands of high speed RS-232 applications. The SP3223EU and 3243EU use an internal high-efficiency, charge-pump power supply that requires only 0.1 $\mu$ F capacitors in 3.3V operation. This charge pump and Sipex's driver architecture allow the SP3223EU/3243EU series to deliver compliant RS-232 performance from a single power supply ranging from +3.0V to +5.5V. The SP3223EU is a 2-driver/2-receiver device, and the SP3243EU is a 3-driver/5-receiver device, ideal for laptop/notebook computer and PDA applications. The SP3243EU includes one complementary receiver that remains alert to monitor an external device's Ring Indicate signal while the device is shutdown.

The AUTO ON-LINE<sup>®</sup> feature allows the device to automatically "wake-up" during a shutdown state when an RS-232 cable is connected and a connected peripheral is turned on. Otherwise, the device automatically shuts itself down drawing less than 1 $\mu$ A.

### SELECTION TABLE

Device	Power Supplies	RS-232 Drivers	RS-232 Receivers	External Components	Auto-Online Circuitry	TTL 3-State	No. of Pins
SP3223EU	+3.0V to +5.5V	2	2	4 capacitors	YES	YES	20
SP3243EU	+3.0V to +5.5V	3	5	4 capacitors	YES	YES	28



## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

$V_{CC}$ .....	-0.3V to +6.0V
$V+$ (NOTE 1).....	-0.3V to +7.0V
$V-$ (NOTE 1).....	+0.3V to -7.0V
$V+ +  V- $ (NOTE 1).....	+13V
$I_{CC}$ (DC $V_{CC}$ or GND current).....	$\pm 100$ mA

### Input Voltages

$TxIN$ , $\overline{ONLINE}$ , SHUTDOWN, EN (SP3223EU).....	-0.3V to +6.0V
$RxIN$ .....	$\pm 25$ V

### Output Voltages

$TxOUT$ .....	$\pm 13.2$ V
$RxOUT$ , STATUS.....	-0.3V to ( $V_{CC} + 0.3$ V)

### Short-Circuit Duration

$TxOUT$ .....	Continuous
Storage Temperature.....	-65°C to +150°C

## Power Dissipation per package

20-pin PDIP (derate 16.0mW/°C above +70°C).....	1300mW
20-pin SSOP (derate 9.25mW/°C above +70°C).....	750mW
20-pin TSSOP (derate 11.1mW/°C above +70°C).....	900mW
28-pin SOIC (derate 12.7mW/°C above +70°C).....	1000mW
28-pin SSOP (derate 11.2mW/°C above +70°C).....	900mW
28-pin TSSOP (derate 13.2mW/°C above +70°C).....	1059mW
32-pin MLPQ (derate 29.4mW/°C above +70°C).....	2352mW

**NOTE 1:**  $V+$  and  $V-$  can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

## ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for  $V_{CC} = +3.0$ V to +5.5V with  $T_{AMB} = T_{MIN}$  to  $T_{MAX}$ , C1 - C4 = 0.1 $\mu$ F. Typical values apply at  $V_{CC} = +3.3$ V or +5.0V and  $T_{AMB} = 25^\circ$ C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DC CHARACTERISTICS					
Supply Current, AUTO ON-LINE®		1.0	10	$\mu$ A	All $RxIN$ open, $\overline{ONLINE} = GND$ , SHUTDOWN = $V_{CC}$ , $V_{CC} = +3.3$ V, $T_{AMB} = +25^\circ$ C, $TxIN = GND$ or $V_{CC}$
Supply Current, Shutdown		1.0	10	$\mu$ A	SHUTDOWN = GND, $V_{CC} = +3.3$ V, $T_{AMB} = +25^\circ$ C, $TxIN = V_{CC}$ or GND
Supply Current, AUTO ON-LINE® Disabled		0.3	1.0	mA	$\overline{ONLINE} = \overline{SHUTDOWN} = V_{CC}$ , no load, $V_{CC} = +3.3$ V, $T_{AMB} = +25^\circ$ C, $TxIN = GND$ or $V_{CC}$
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold LOW HIGH	2.4		0.8	V V	$V_{CC} = +3.3$ V or +5.0V, $TxIN$ , $\overline{EN}$ (SP3223EU), $\overline{ONLINE}$ , SHUTDOWN
Input Leakage Current		$\pm 0.01$	$\pm 1.0$	$\mu$ A	$TxIN$ , $\overline{EN}$ , $\overline{ONLINE}$ , SHUTDOWN, $T_{AMB} = +25^\circ$ C, $V_{IN} = 0$ V to $V_{CC}$
Output Leakage Current		$\pm 0.05$	$\pm 10$	$\mu$ A	Receivers disabled, $V_{OUT} = 0$ V to $V_{CC}$
Output Voltage LOW			0.4	V	$I_{OUT} = 1.6$ mA
Output Voltage HIGH	$V_{CC} - 0.6$	$V_{CC} - 0.1$		V	$I_{OUT} = -1.0$ mA
DRIVER OUTPUTS					
Output Voltage Swing	$\pm 5.0$	$\pm 5.4$		V	All driver outputs loaded with 3K $\Omega$ to GND, $T_{AMB} = +25^\circ$ C
Output Resistance	300			$\Omega$	$V_{CC} = V+ = V- = 0$ V, $V_{OUT} = \pm 2$ V
Output Short-Circuit Current		$\pm 35$	$\pm 60$	mA	$V_{OUT} = 0$ V
Output Leakage Current			$\pm 25$	$\mu$ A	$V_{CC} = 0$ V or 3.0V to 5.5V, $V_{OUT} = \pm 12$ V, Drivers disabled

## ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for  $V_{CC} = +3.0V$  to  $+5.5V$  with  $T_{AMB} = T_{MIN}$  to  $T_{MAX}$ ,  $C1 - C4 = 0.1\mu F$ . Typical values apply at  $V_{CC} = +3.3V$  or  $+5.0V$  and  $T_{AMB} = 25^{\circ}C$ .

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>RECEIVER INPUTS</b>					
Input Voltage Range	-25		25	V	
Input Threshold LOW	0.6	1.2		V	$V_{CC} = 3.3V$
Input Threshold LOW	0.8	1.5		V	$V_{CC} = 5.0V$
Input Threshold HIGH		1.5	2.4	V	$V_{CC} = 3.3V$
Input Threshold HIGH		1.8	2.4	V	$V_{CC} = 5.0V$
Input Hysteresis		0.3		V	
Input Resistance	3	5	7	k $\Omega$	
<b>AUTO ON-LINE® CIRCUITRY CHARACTERISTICS (ONLINE = GND, SHUTDOWN = <math>V_{CC}</math>)</b>					
STATUS Output Voltage LOW			0.4	V	$I_{OUT} = 1.6mA$
STATUS Output Voltage HIGH	$V_{CC} - 0.6$			V	$I_{OUT} = -1.0mA$
Receiver Threshold to Drivers Enabled ( $t_{ONLINE}$ )		200		$\mu S$	Figure 19
Receiver Positive or Negative Threshold to STATUS HIGH ( $t_{STSH}$ )		0.5		$\mu S$	Figure 19
Receiver Positive or Negative Threshold to STATUS LOW ( $t_{STSL}$ )		20		$\mu S$	Figure 19
<b>TIMING CHARACTERISTICS</b>					
Maximum Data Rate	1000			Kbps	$R_L = 3K\Omega$ , $C_L = 250pF$ , one driver active
Receiver Propagation Delay $t_{PHL}$ $t_{PLH}$		0.15 0.15		$\mu s$	Receiver input to Receiver output, $C_L = 150pF$
Receiver Output Enable Time		200		ns	Normal operation
Receiver Output Disable Time		200		ns	Normal operation
Driver Skew		100		ns	$ t_{PHL} - t_{PLH} $
Receiver Skew		50		ns	$ t_{PHL} - t_{PLH} $
Transition-Region Slew Rate		90		V/ $\mu s$	$V_{CC} = 3.3V$ , $R_L = 3K\Omega$ , $T_{AMB} = 25^{\circ}C$ , measurements taken from $-3.0V$ to $+3.0V$ or $+3.0V$ to $-3.0V$

## TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for  $V_{CC} = +3.3V$ , 1000kbps data rate, all drivers loaded with  $3k\Omega$ ,  $0.1\mu F$  charge pump capacitors, and  $T_{AMB} = +25^{\circ}C$ .

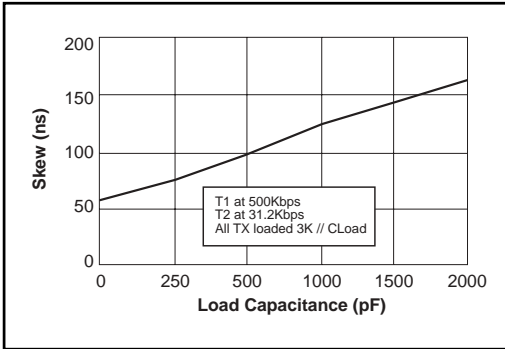


Figure 1. Transmitter Skew VS. Load Capacitance for the 3223EU / 3243EU

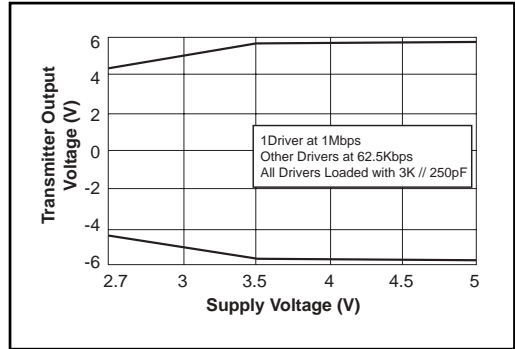


Figure 2. Transmitter Output Voltage VS. Supply Voltage for the SP3223EU

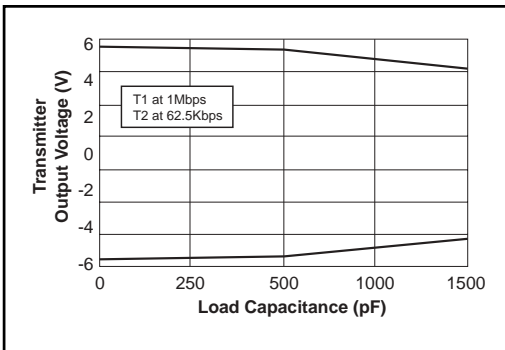


Figure 3. Transmitter Output Voltage VS. Load Capacitance for the SP3223EU

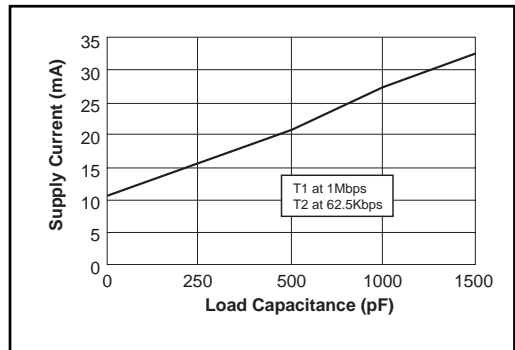


Figure 4. Supply Current VS. Load Capacitance for the SP3223EU

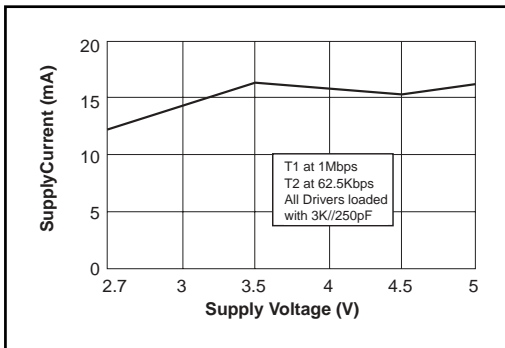


Figure 5. Supply Current VS. Supply Voltage for the SP3223EU

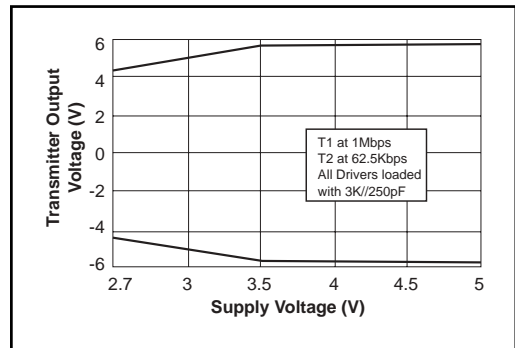


Figure 6. Transmitter Output Voltage VS. Supply Voltage for the SP3223EU

## TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for  $V_{CC} = +3.3V$ , 1000kbps data rate, all drivers loaded with  $3k\Omega$ ,  $0.1\mu F$  charge pump capacitors, and  $T_{AMB} = +25^{\circ}C$ .

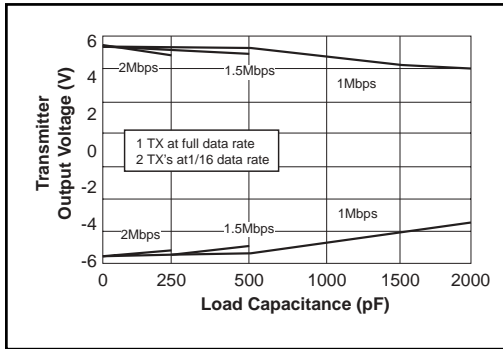


Figure 7. Transmitter Output Voltage VS. Load Capacitance for the SP3243EU

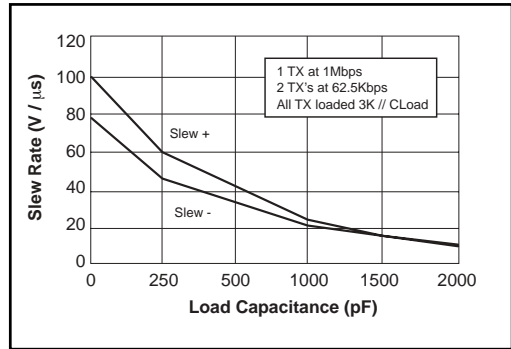


Figure 8. Slew Rate VS. Load Capacitance for the SP3243EU

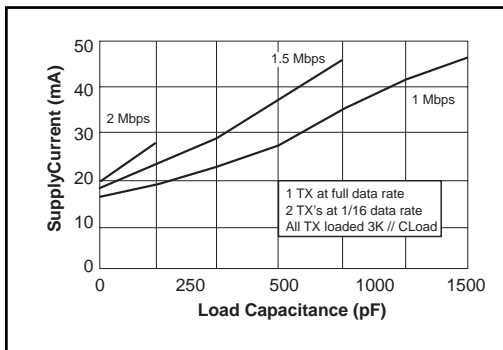


Figure 9. Supply Current VS. Load Capacitance for the SP3243EU

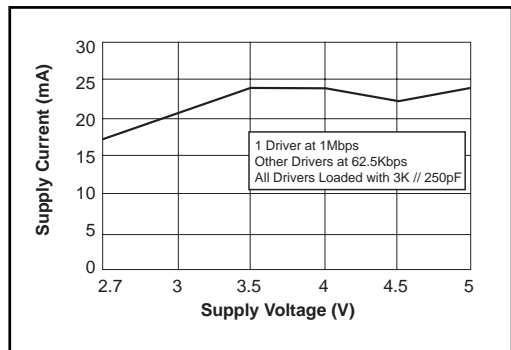


Figure 10. Supply Current VS. Supply Voltage for the SP3243EU

NAME	FUNCTION	PIN NUMBER		
		SP3223EU	SP3243EU	SP3243EUCR MLPQ
EN	Receiver Enable. Apply logic LOW for normal operation. Apply logic HIGH to disable the receiver outputs (high-Z state).	1	-	-
C1+	Positive terminal of the voltage doubler charge-pump capacitor.	2	28	28
V+	Regulated +5.5V output generated by the charge pump.	3	27	26
C1-	Negative terminal of the voltage doubler charge-pump capacitor.	4	24	22
C2+	Positive terminal of the inverting charge-pump capacitor.	5	1	29
C2-	Negative terminal of the inverting charge-pump capacitor.	6	2	31
V-	Regulated -5.5V output generated by the charge pump.	7	3	32
R <sub>1</sub> IN	RS-232 receiver input.	16	4	2
R <sub>2</sub> IN	RS-232 receiver input.	9	5	3
R <sub>3</sub> IN	RS-232 receiver input.	-	6	4
R <sub>4</sub> IN	RS-232 receiver input.	-	7	5
R <sub>5</sub> IN	RS-232 receiver input.	-	8	6
R <sub>1</sub> OUT	TTL/CMOS receiver output.	15	19	17
R <sub>2</sub> OUT	TTL/CMOS receiver output.	10	18	16
$\overline{R_2}$ OUT	Non-inverting receiver-2 output, active in shutdown.	-	20	18
R <sub>3</sub> OUT	TTL/CMOS receiver output.	-	17	15
R <sub>4</sub> OUT	TTL/CMOS receiver output.	-	16	14
R <sub>5</sub> OUT	TTL/CMOS receiver output.	-	15	13
$\overline{\text{STATUS}}$	TTL/CMOS Output indicating online and shutdown status.	11	21	19
T <sub>1</sub> IN	TTL/CMOS driver input.	13	14	12
T <sub>2</sub> IN	TTL/CMOS driver input.	12	13	11
T <sub>3</sub> IN	TTL/CMOS driver input.	-	12	10
$\overline{\text{ONLINE}}$	Apply logic HIGH to override Auto-Online circuitry keeping drivers active ( $\overline{\text{SHUTDOWN}}$ must also be logic HIGH, refer to Table 2).	14	23	21
T <sub>1</sub> OUT	RS-232 driver output.	17	9	7
T <sub>2</sub> OUT	RS-232 driver output.	8	10	8
T <sub>3</sub> OUT	RS-232 driver output.	-	11	9
GND	Ground.	18	25	23
V <sub>CC</sub>	+3.0V to +5.5V supply voltage.	19	26	25
$\overline{\text{SHUTDOWN}}$	Apply logic LOW to shut down drivers and charge pump. This overrides all AUTO ON-LINE® circuitry and $\overline{\text{ONLINE}}$ (refer to Table 2).	20	22	20
NC	No Connection	-	-	1,24,27,30

**Table 1. Device Pin Description**

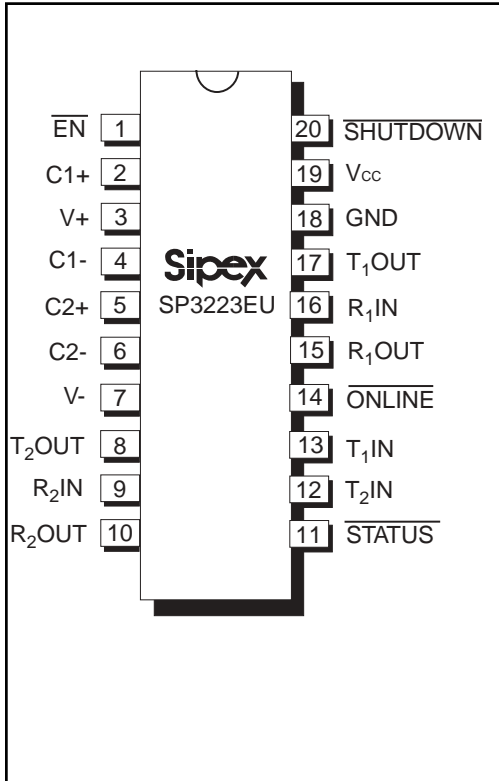


Figure 11. SP3223EU Pinout Configuration

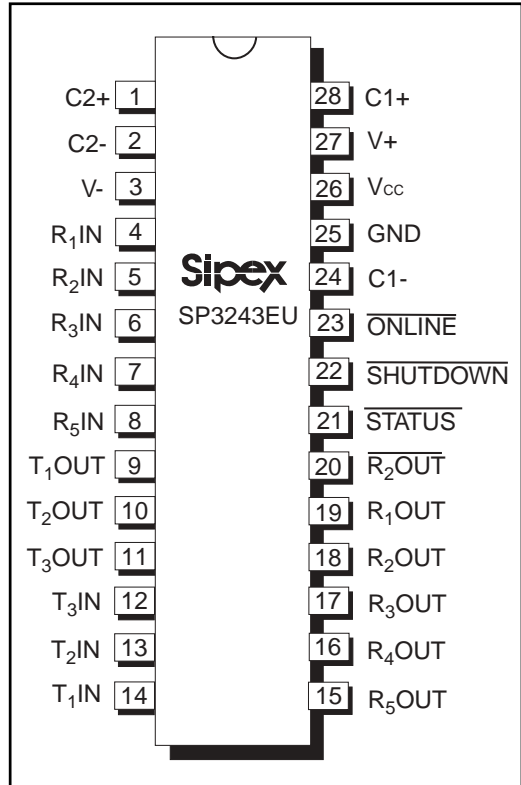


Figure 12. SP3243EU Pinout Configuration

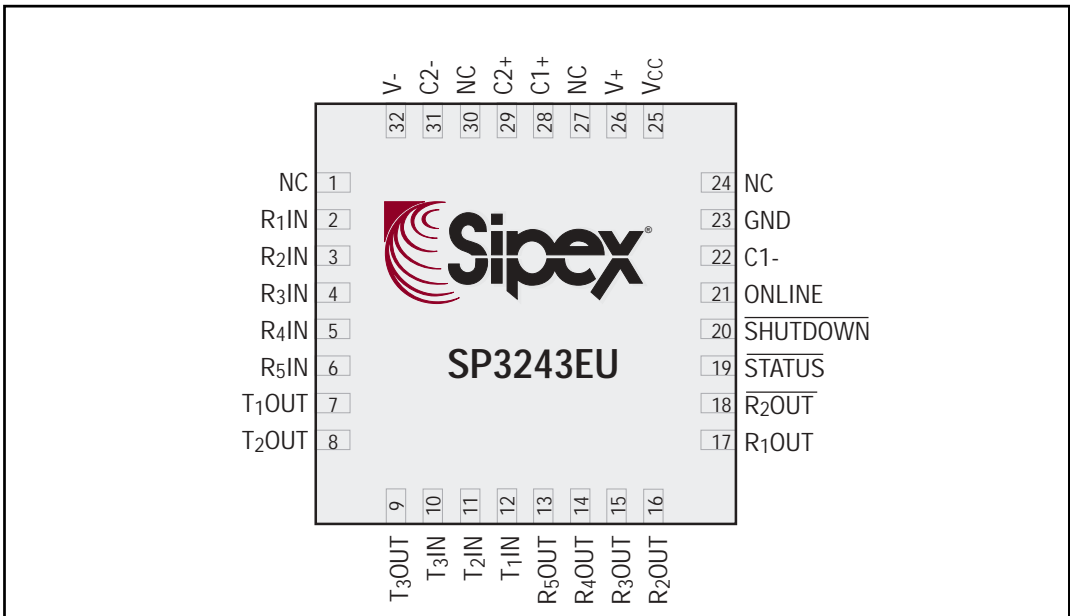


Figure 13. SP3243EU MLPQ Pinout Configuration

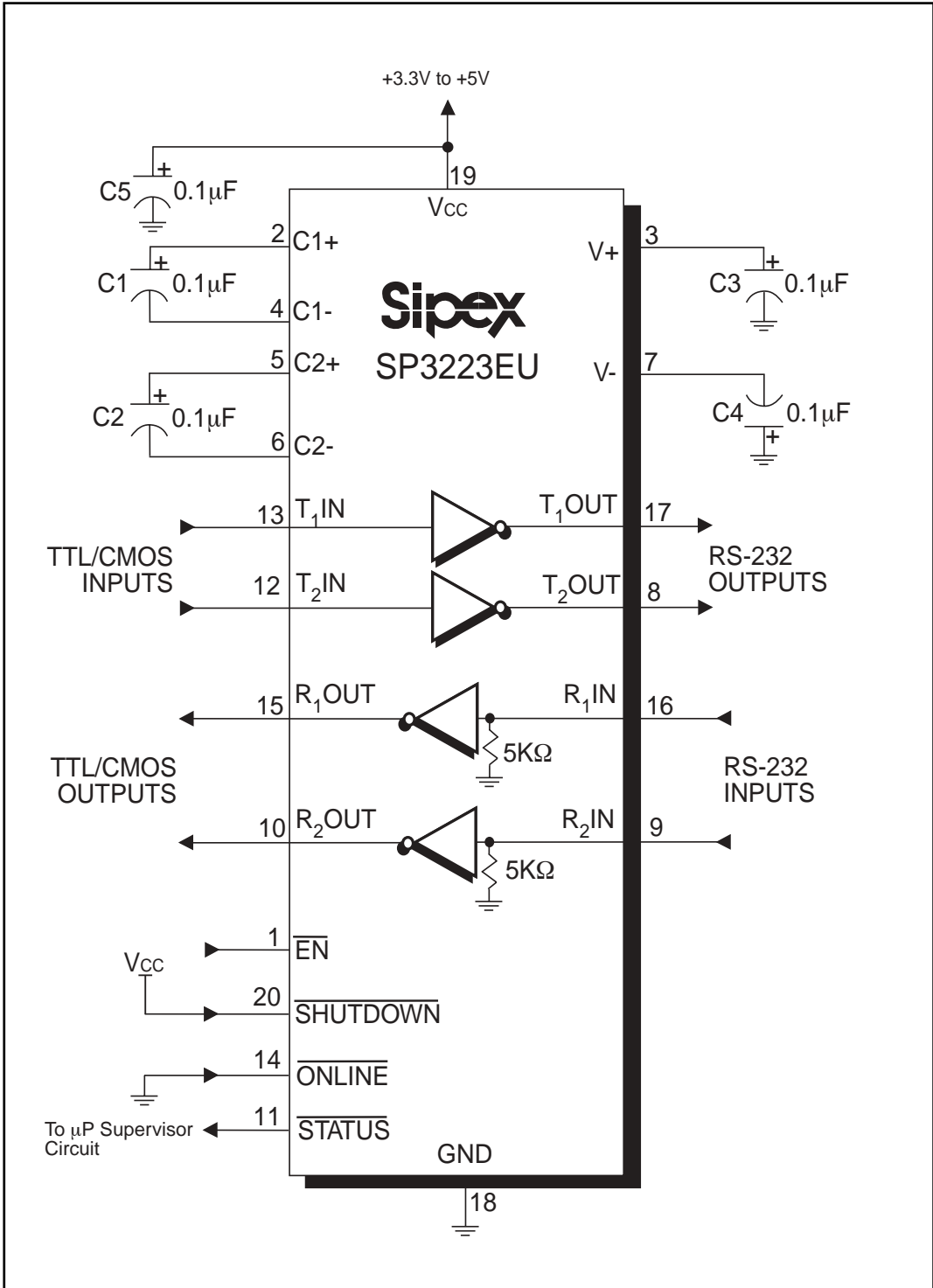


Figure 14. SP3223EU Typical Operating Circuit



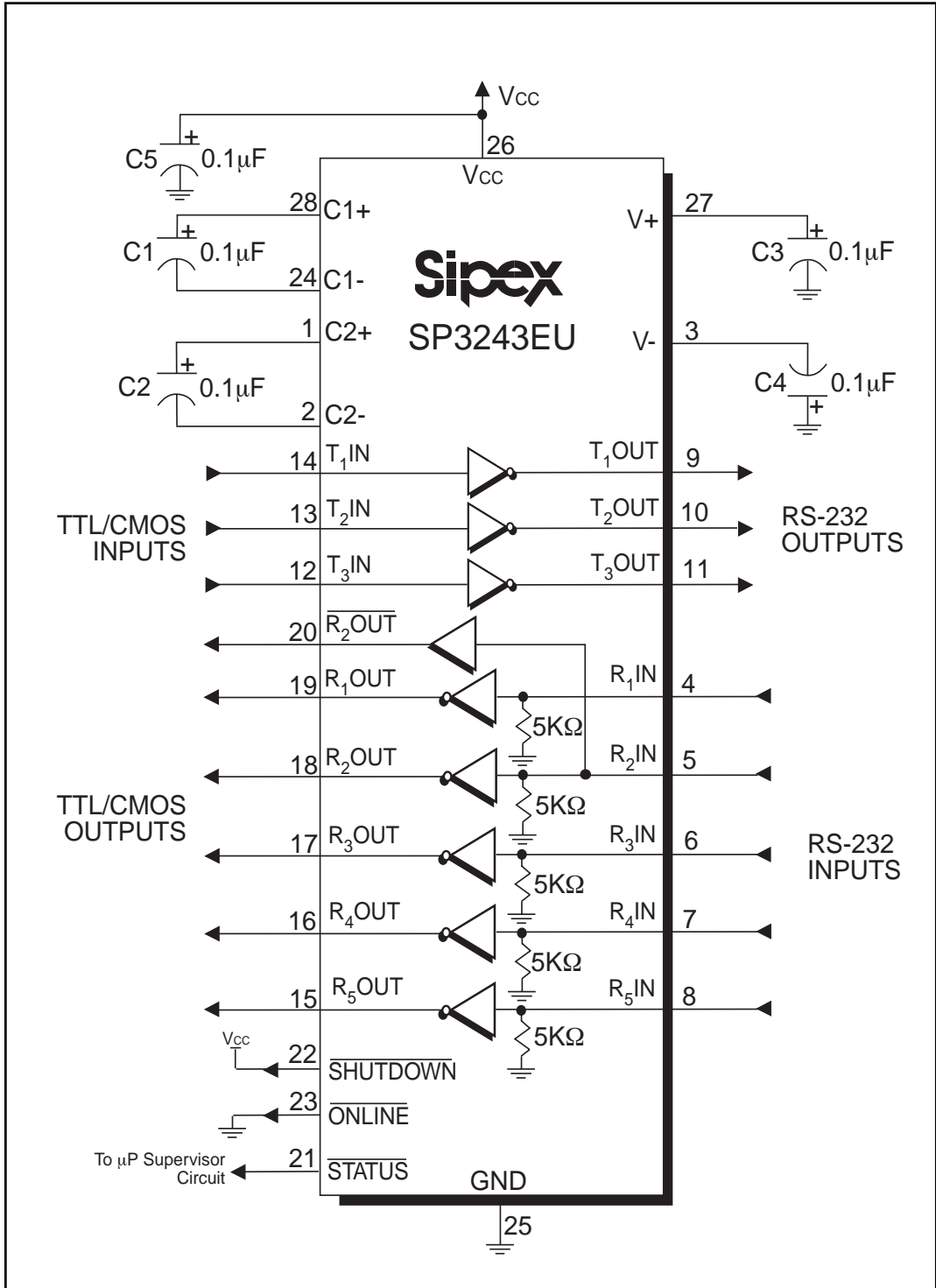


Figure 15. SP3243EU Typical Operating Circuit

## DESCRIPTION

The SP3223EU and SP3243EU transceivers meet the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The SP3223EU and SP3243EU devices feature Sipex's proprietary and patented (U.S.-- 5,306,954) on-board charge pump circuitry that generates  $\pm 5.5V$  RS-232 voltage levels from a single +3.0V to +5.5V power supply. The SP3223EU and SP3243EU devices can operate at a data rate of 1000kbps fully loaded.

The SP3223EU is a 2-driver/2-receiver device, and the SP3243EU is a 3-driver/5-receiver device, ideal for portable or hand-held applications. The SP3243EU includes one complementary always-active receiver that can monitor an external device (such as a modem) in shutdown. This aids in protecting the UART or serial controller IC by preventing forward biasing of the protection diodes where  $V_{CC}$  may be disconnected.

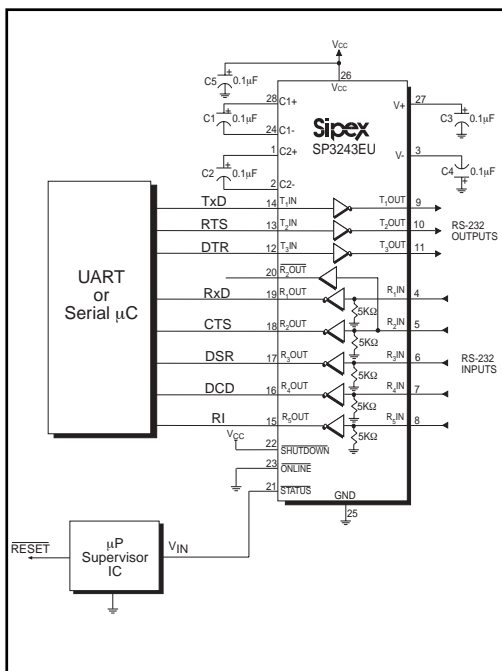


Figure 16. Interface Circuitry Controlled by Microprocessor Supervisory Circuit

The SP3223EU and SP3243EU series is an ideal choice for power sensitive designs. The SP3223EU and SP3243EU devices feature AUTO ON-LINE<sup>®</sup> circuitry which reduces the power supply drain to a 1 $\mu$ A supply current. In many portable or hand-held applications, an RS-232 cable can be disconnected or a connected peripheral can be turned off. Under these conditions, the internal charge pump and the drivers will be shut down. Otherwise, the system automatically comes online. This feature allows design engineers to address power saving concerns without major design changes.

## THEORY OF OPERATION

The SP3223EU and SP3243EU series is made up of four basic circuit blocks:

1. Drivers
2. Receivers
3. the Sipex proprietary charge pump, and
4. AUTO ON-LINE<sup>®</sup> circuitry.

### Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to 5.0V EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is  $\pm 5.4V$  with no load and  $\pm 5V$  minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. These drivers comply with the EIA-TIA-232-F and all previous RS-232 versions. Unused drivers inputs should be connected to GND or  $V_{CC}$ .

The drivers have a minimum data rate of 1000kbps fully loaded with 3k $\Omega$  in parallel with 250pF, ensuring compatibility with PC-to-PC communication software.

DEVICE: SP3223EU			
$\overline{\text{SHUTDOWN}}$	$\overline{\text{EN}}$	T <sub>x</sub> OUT	R <sub>x</sub> OUT
0	0	High Z	Active
0	1	High Z	High Z
1	0	Active	Active
1	1	Active	High Z

DEVICE: SP3243EU			
$\overline{\text{SHUTDOWN}}$	T <sub>x</sub> OUT	R <sub>x</sub> OUT	$\overline{\text{R}}_2$ OUT
0	High Z	High Z	Active
1	Active	Active	Active

Table 2.  $\overline{\text{SHUTDOWN}}$  and  $\overline{\text{EN}}$  Truth Tables  
 Note: In AUTO ON-LINE® Mode where  $\overline{\text{ONLINE}} = \text{GND}$  and  $\overline{\text{SHUTDOWN}} = \text{V}_{\text{CC}}$  the device will shut down if there is no activity present at the Receiver inputs.

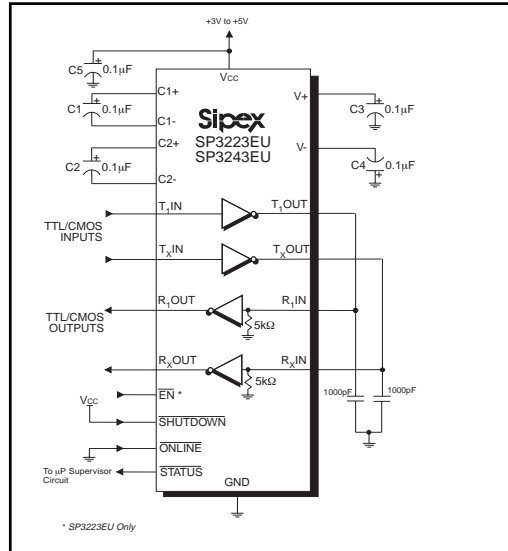


Figure 17. Loopback Test Circuit for RS-232 Driver Data Transmission Rates

Figure 17 shows a loopback test circuit used to test the RS-232 Drivers. Figure 18 shows the test results where one driver was active at 1Mbps and all three drivers loaded with an RS-232 receiver in parallel with a 250pF capacitor. Figure 19 shows the test results of the loopback circuit with all drivers active at 250kbps with typical RS-232 loads in parallel with 1000pF capacitors. A superior RS-232 data transmission rate of 1Mbps

makes the SP3223EU/3243EU series an ideal match for high speed LAN and personal computer peripheral applications.

## Receivers

The receivers convert  $\pm 5.0\text{V}$  EIA/TIA-232 levels to TTL or CMOS logic output levels. The SP3223EU receivers have an inverting output that can be disabled by using the  $\overline{\text{EN}}$  pin.

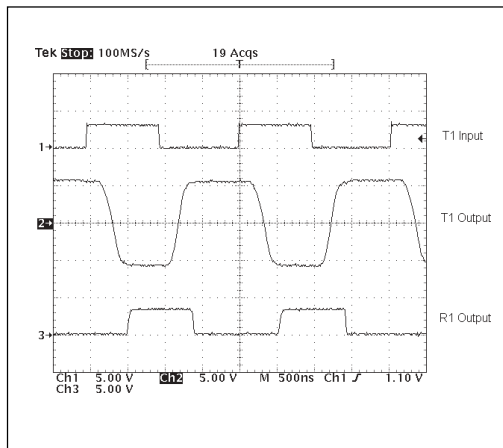


Figure 18. Loopback Test results at 1Mbps

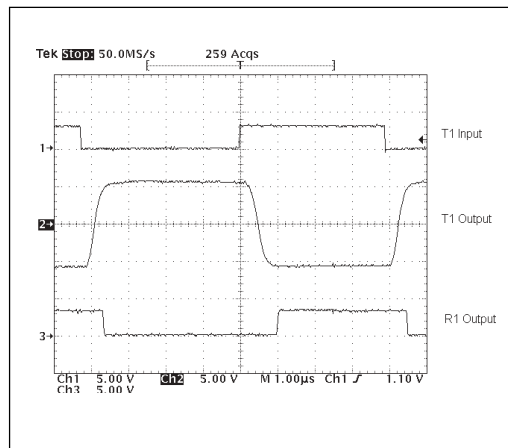


Figure 19. Loopback Test results at 250Kbps

Receivers are active when the AUTO ON-LINE® circuitry is enabled or when in shutdown. During the shutdown, the receivers will continue to be active. If there is no activity present at the receivers for a period longer than 100µs or when SHUTDOWN is enabled, the device goes into a standby mode where the circuit draws 1µA. Driving EN to a logic HIGH forces the outputs of the receivers into high-impedance. The truth table logic of the SP3223EU and SP3243EU driver and receiver outputs can be found in Table 2.

The SP3243EU includes an additional non-inverting receiver with an output R<sub>2</sub>OUT. R<sub>2</sub>OUT is an extra output that remains active and monitors activity while the other receiver outputs are forced into high impedance. This allows Ring Indicator (RI) from a peripheral to be monitored without forward biasing the TTL/CMOS inputs of the other devices connected to the receiver outputs.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal 5KΩ pulldown resistor to ground will commit the output of the receiver to a HIGH state.

## Charge Pump

The charge pump is a Sipex-patented design (U.S. 5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages 5.5V regardless of the input voltage ( $V_{CC}$ ) over the +3.0V to +5.5V range. This is important to maintain compliant RS-232 levels regardless of power supply fluctuations.

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pump is enabled. If the output voltages exceed a magnitude of 5.5V, the charge pump is disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

### Phase 1

—  $V_{SS}$  charge storage — During this phase of the clock cycle, the positive side of capacitors  $C_1$  and  $C_2$  are initially charged to  $V_{CC}$ .  $C_1^+$  is then switched to GND and the charge in  $C_1^-$  is transferred to  $C_2^-$ . Since  $C_2^+$  is connected to  $V_{CC}$ , the voltage potential across capacitor  $C_2$  is now 2 times  $V_{CC}$ .

### Phase 2

—  $V_{SS}$  transfer — Phase two of the clock connects the negative terminal of  $C_2$  to the  $V_{SS}$  storage capacitor and the positive terminal of  $C_2$  to GND. This transfers a negative generated voltage to  $C_3$ . This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to  $C_3$ , the positive side of capacitor  $C_1$  is switched to  $V_{CC}$  and the negative side is connected to GND.

### Phase 3

—  $V_{DD}$  charge storage — The third phase of the clock is identical to the first phase — the charge transferred in  $C_1$  produces  $-V_{CC}$  in the negative terminal of  $C_1$ , which is applied to the negative side of capacitor  $C_2$ . Since  $C_2^+$  is at  $V_{CC}$ , the voltage potential across  $C_2$  is 2 times  $V_{CC}$ .

### Phase 4

—  $V_{DD}$  transfer — The fourth phase of the clock connects the negative terminal of  $C_2$  to GND, and transfers this positive generated voltage across  $C_2$  to  $C_4$ , the  $V_{DD}$  storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to  $C_4$ , the positive side of capacitor  $C_1$  is switched to  $V_{CC}$  and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both  $V^+$  and  $V^-$  are separately generated from  $V_{CC}$ , in a no-load condition  $V^+$  and  $V^-$  will be symmetrical. Older charge pump approaches that generate  $V^-$  from  $V^+$  will show a decrease in the magnitude of  $V^-$  compared to  $V^+$  due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 250kHz. The external capacitors can be as low as  $0.1\mu\text{F}$  with a 16V breakdown voltage rating.

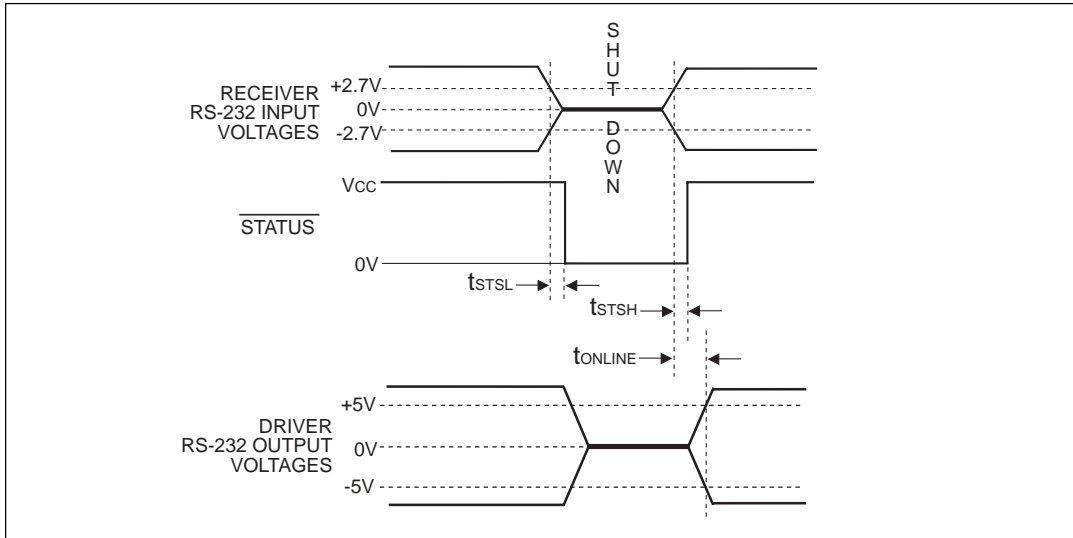


Figure 20. AUTO ON-LINE® Timing Waveforms

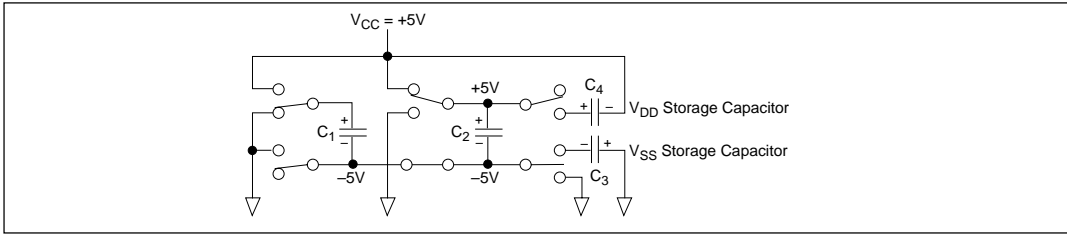


Figure 21. Charge Pump — Phase 1

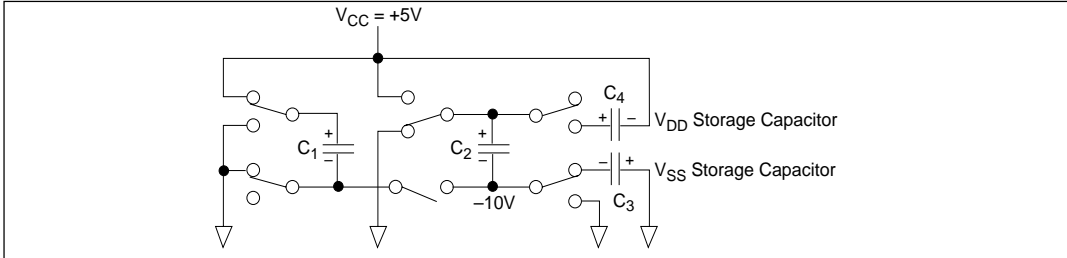


Figure 22. Charge Pump — Phase 2

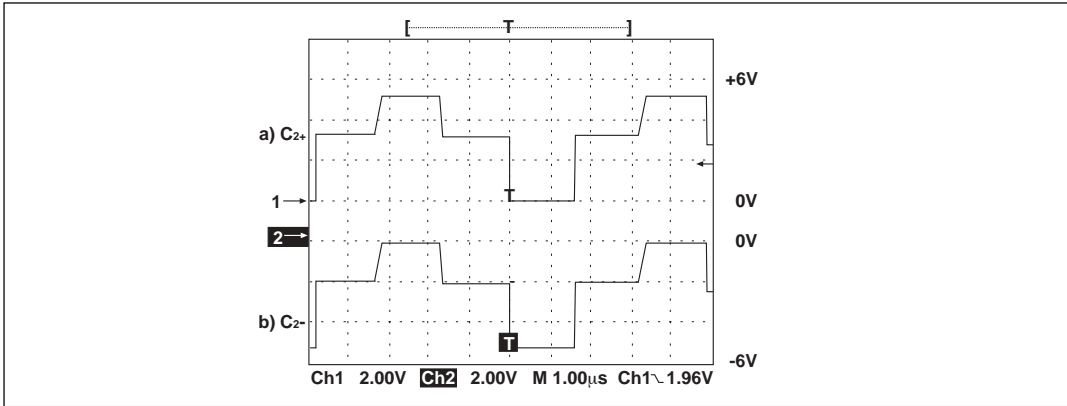


Figure 23. Charge Pump Waveforms

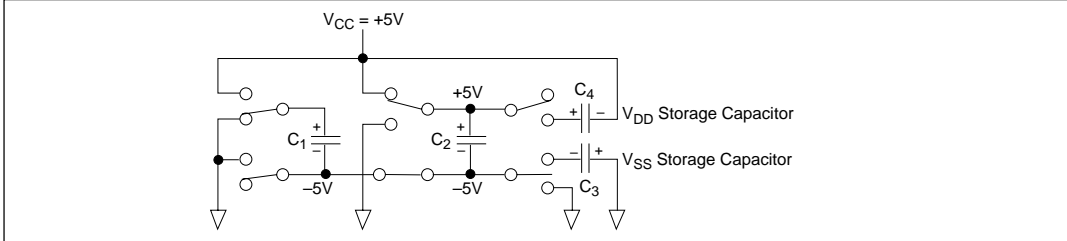


Figure 24. Charge Pump — Phase 3

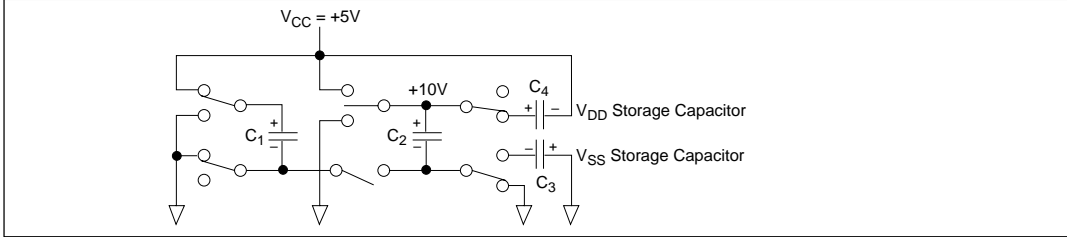


Figure 25. Charge Pump — Phase 4

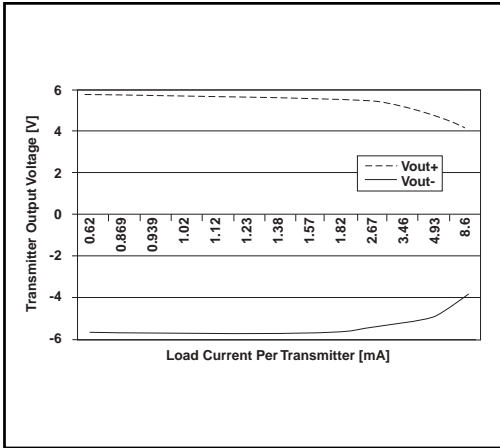


Figure 26. SP3243EU Driver Output Voltages vs. Load Current per Transmitter

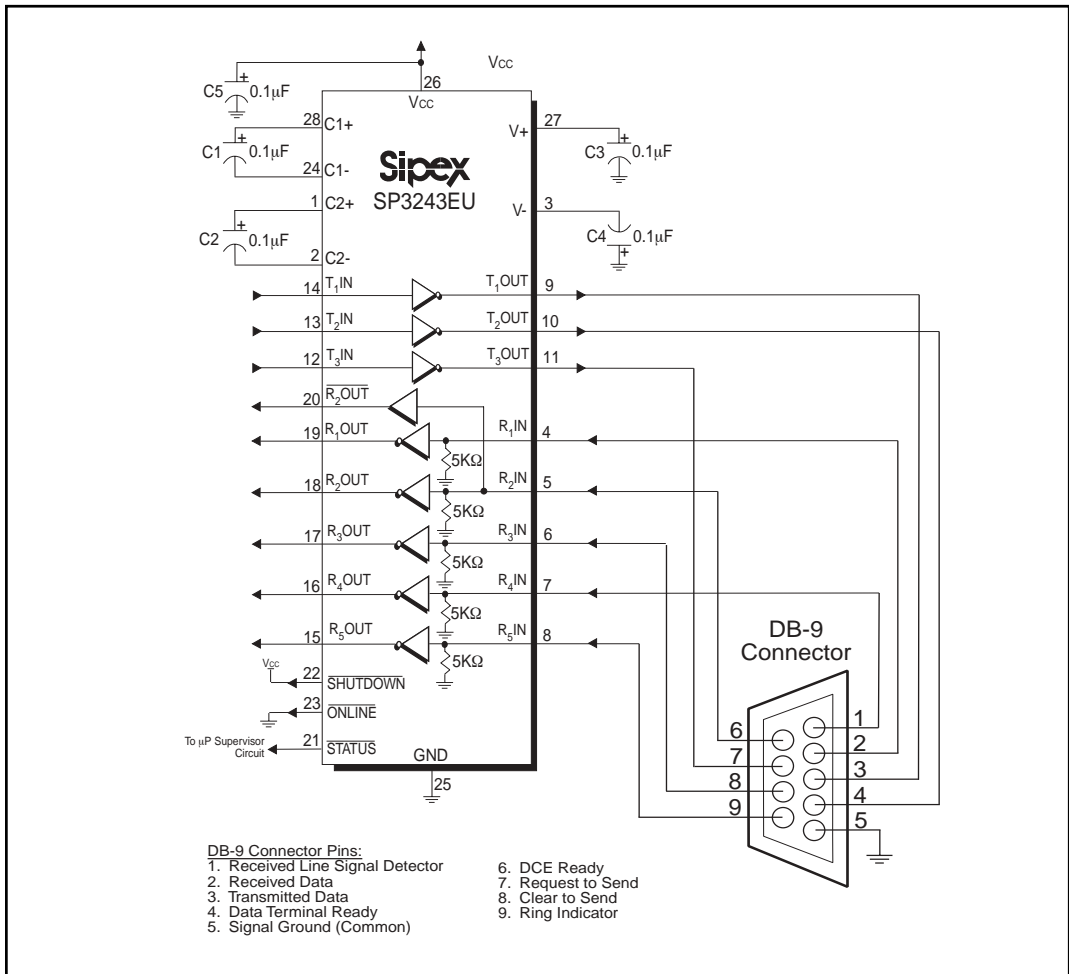


Figure 27. Circuit for the connectivity of the SP3243EU with a DB-9 connector

RS-232 SIGNAL AT RECEIVER INPUT	$\overline{\text{SHUTDOWN}}$ INPUT	$\overline{\text{ONLINE}}$ INPUT	$\overline{\text{STATUS}}$ OUTPUT	TRANSCEIVER STATUS
YES	HIGH	LOW	HIGH	Normal Operation <b>(Auto-Online)</b>
NO	HIGH	HIGH	LOW	Normal Operation
NO	HIGH	LOW	LOW	Shutdown <b>(Auto-Online)</b>
YES	LOW	HIGH / LOW	HIGH	Shutdown
NO	LOW	HIGH / LOW	LOW	Shutdown

Table 3. AUTO ON-LINE<sup>®</sup> Logic

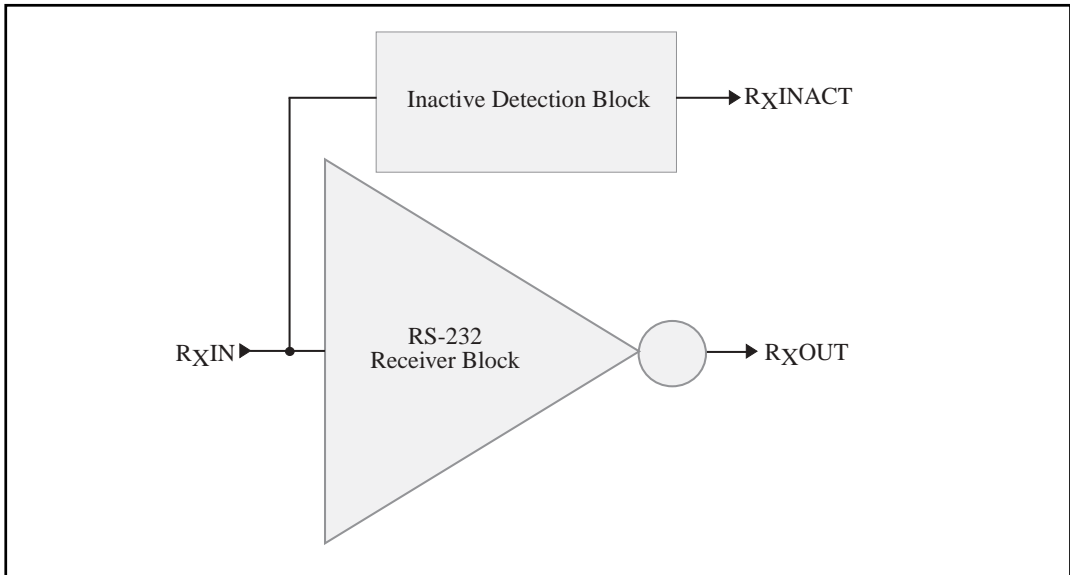


Figure 28. Stage I of AUTO ON-LINE<sup>®</sup> Circuitry

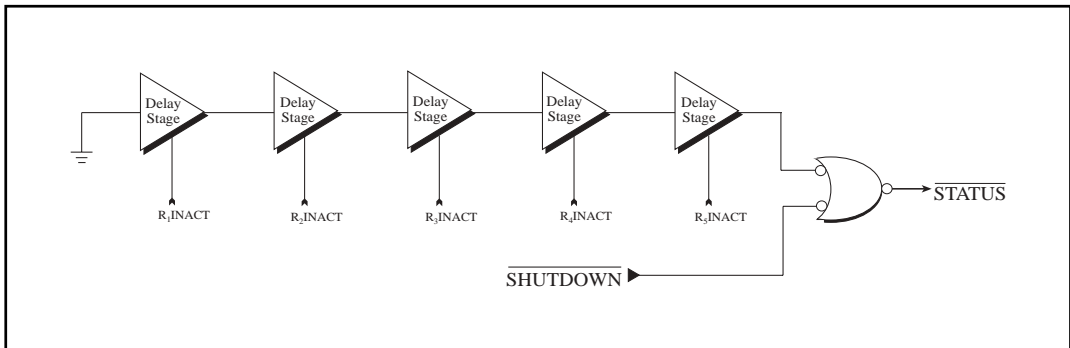


Figure 29. Stage II of AUTO ON-LINE<sup>®</sup> Circuitry



## AUTO ON-LINE® Circuitry

The SP3223EU and SP3243EU devices have a patent pending AUTO ON-LINE® circuitry on board that saves power in applications such as laptop computers, palmtop (PDA) computers and other portable systems.

The SP3223EU and SP3243EU devices incorporate an AUTO ON-LINE® circuit that automatically enables itself when the external transmitters are enabled and the cable is connected. Conversely, the AUTO ON-LINE® circuit also disables most of the internal circuitry when the device is not being used and goes into a standby mode where the device typically draws 1mA. This function can also be externally controlled by the  $\overline{\text{ONLINE}}$  pin. When this pin is tied to a logic LOW, the AUTO ON-LINE® function is active. Once active, the device is enabled until there is no activity on the receiver inputs. The receiver input typically sees at least  $\pm 3\text{V}$ , which are generated from the transmitters at the other end of the cable with a  $\pm 5\text{V}$  minimum. When the external transmitters are disabled or the cable is disconnected, the receiver inputs will be pulled down by their internal  $5\text{k}\Omega$  resistors to ground. When this occurs over a period of time, the internal transmitters will be disabled and the device goes into a shutdown or standby mode. When  $\overline{\text{ONLINE}}$  is HIGH, the AUTO ON-LINE® mode is disabled.

The AUTO ON-LINE® circuit has two stages:

- 1) Inactive Detection
- 2) Accumulated Delay

The first stage, shown in Figure 28, detects an inactive input. A logic HIGH is asserted on  $R_x\text{INACT}$  if the cable is disconnected or the external transmitters are disabled. Otherwise,  $R_x\text{INACT}$  will be at a logic LOW. This circuit is duplicated for each of the other receivers.

The second stage of the AUTO ON-LINE® circuitry, shown in Figure 29, processes all the receiver's  $R_x\text{INACT}$  signals with an accumulated delay that disables the device to a  $1\mu\text{A}$  supply current.

The  $\overline{\text{STATUS}}$  pin goes to a logic LOW when the cable is disconnected, the external transmitters are disabled, or the SHUTDOWN pin is invoked. The typical accumulated delay is around  $20\mu\text{s}$ .

When the SP3223EU and SP3243EU drivers or internal charge pump are disabled, the supply current is reduced to  $1\mu\text{A}$ . This can commonly occur in hand-held or portable applications where the RS-232 cable is disconnected or the RS-232 drivers of the connected peripheral are turned off.

The AUTO ON-LINE® mode can be disabled by the  $\overline{\text{SHUTDOWN}}$  pin. If this pin is a logic LOW, the AUTO ON-LINE® function will not operate regardless of the logic state of the  $\overline{\text{ONLINE}}$  pin. Table 3 summarizes the logic of the AUTO ON-LINE® operating modes. The truth table logic of the SP3223EU and SP3243EU driver and receiver outputs can be found in Table 2.

The  $\overline{\text{STATUS}}$  pin outputs a logic LOW signal if the device is shutdown. This pin goes to a logic HIGH when the external transmitters are enabled and the cable is connected.

When the SP3223EU and SP3243EU devices are shut down, the charge pumps are turned off.  $V+$  charge pump output decays to  $V_{CC}$ , the  $V-$  output decays to GND. The decay time will depend on the size of capacitors used for the charge pump. Once in shutdown, the time required to exit the shut down state and have valid  $V+$  and  $V-$  levels is typically  $200\mu\text{s}$ .

For easy programming, the  $\overline{\text{STATUS}}$  can be used to indicate DTR or a Ring Indicator signal. Tying  $\overline{\text{ONLINE}}$  and  $\overline{\text{SHUTDOWN}}$  together will bypass the AUTO ON-LINE® circuitry so this connection acts like a shutdown input pin.

## ESD TOLERANCE

The SP3223EU/3243EU series incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least  $\pm 15\text{kV}$  without damage nor latch-up.

There are different methods of ESD testing applied:

- a) MIL-STD-883, Method 3015.7
- b) IEC1000-4-2 Air-Discharge
- c) IEC1000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semi-conductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in Figure 30. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-1000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC1000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during

normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC1000-4-2 is shown on Figure 31. There are two methods within IEC1000-4-2, the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

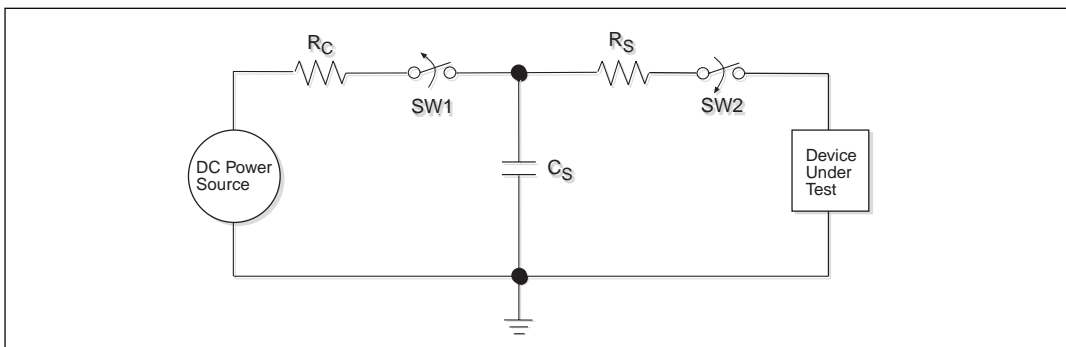


Figure 30. ESD Test Circuit for Human Body Model

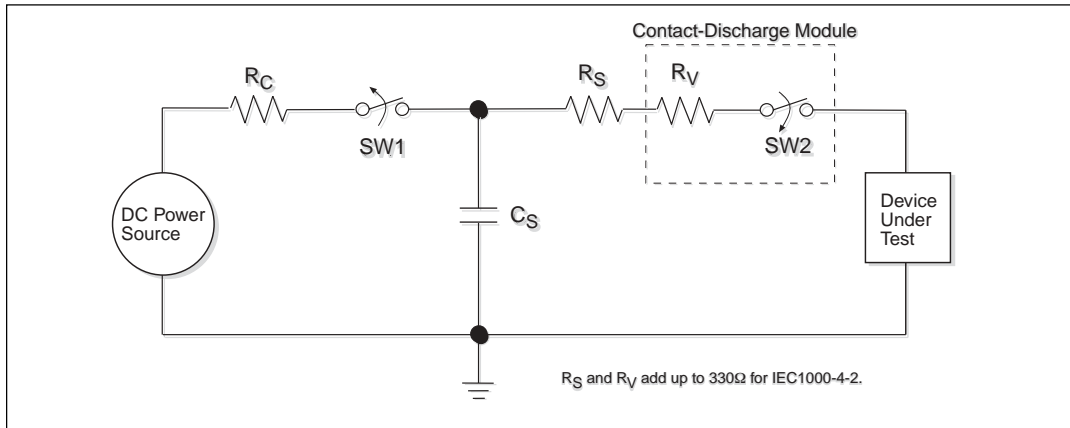


Figure 31. ESD Test Circuit for IEC1000-4-2

The circuit models in Figures 30 and 31 represent the typical ESD testing circuit used for all three methods. The  $C_S$  is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through  $R_S$ , the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor ( $R_S$ ) and the source capacitor ( $C_S$ ) are 1.5kΩ and 100pF, respectively. For IEC-1000-4-2, the current limiting resistor ( $R_S$ ) and the source capacitor ( $C_S$ ) are 330Ω and 150pF, respectively.

The higher  $C_S$  value and lower  $R_S$  value in the IEC1000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

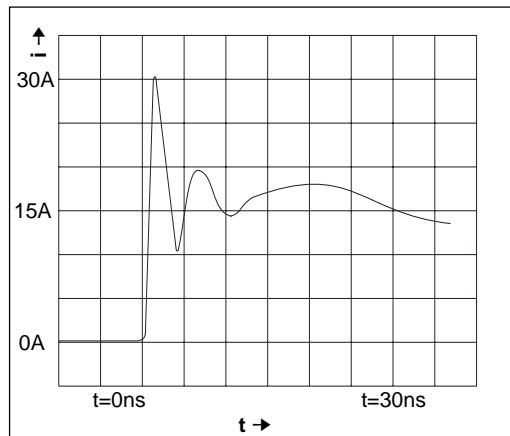
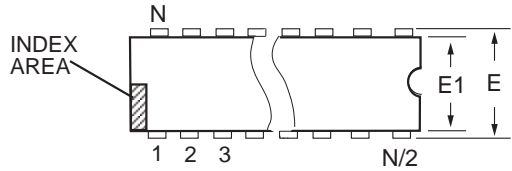
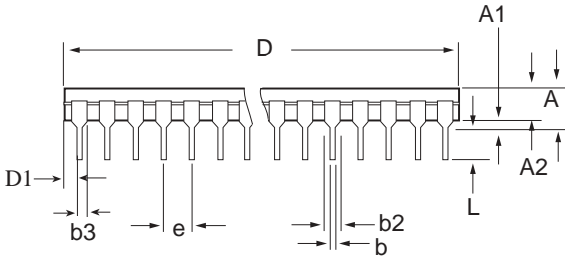


Figure 32. ESD Test Waveform for IEC1000-4-2

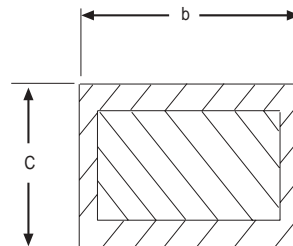
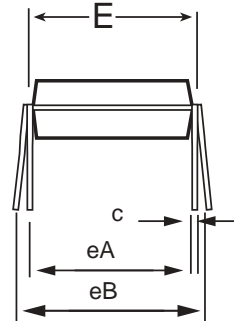
DEVICE PIN TESTED	HUMAN BODY MODEL	IEC1000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	±15kV	±15kV	±8kV	4
Receiver Inputs	±15kV	±15kV	±8kV	4

Table 4. Transceiver ESD Tolerance Levels

**PACKAGE: 20 PIN PDIP**

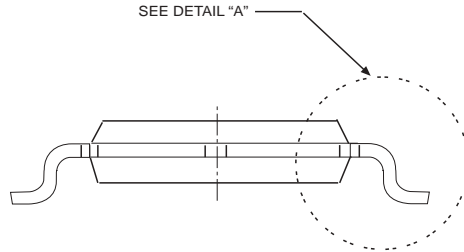
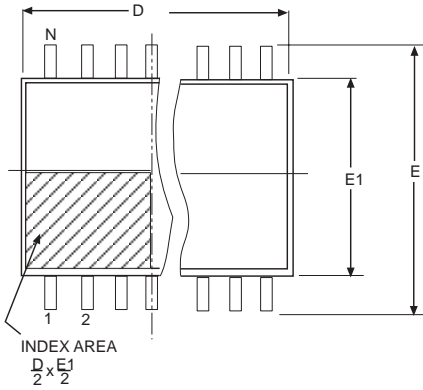


20 PIN PDIP JEDEC MS-001 (AD) Variation	Dimensions in inches		
	MIN	NOM	MAX
A	-	-	.210
A1	.015	-	-
A2	.115	.130	.195
b	.014	.018	.022
b2	.045	.060	.070
b3	.030	.039	.045
c	.008	.010	.014
D	.980	1.030	1.060
D1	.005	-	-
E	.300	.310	.325
E1	.240	.250	.280
e	.100 BSC		
eA	.300 BSC		
eB	-	-	.430
L	.115	.130	.150

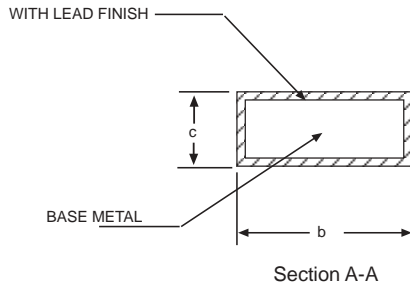
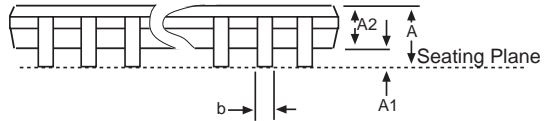
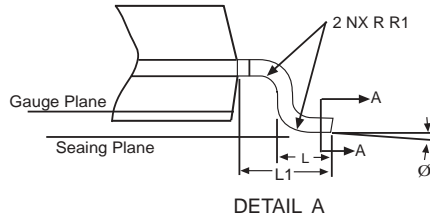


**20 pin PDIP**

# PACKAGE: 20 PIN SSOP

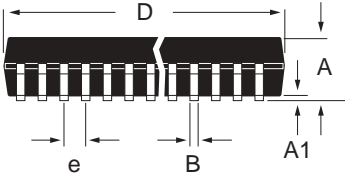
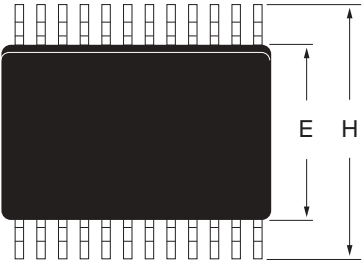


20 PIN SSOP JEDEC MO-150 (AE) Variation	Dimensions in (mm)		
	MIN	NOM	MAX
A	-	-	2.0
A1	0.05	-	-
A2	1.65	1.75	1.85
b	0.22	-	0.38
c	0.09	-	0.25
D	6.90	7.20	7.50
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
L	0.55	0.75	0.95
L1	1.25 REF		
∅	0°	4°	8°



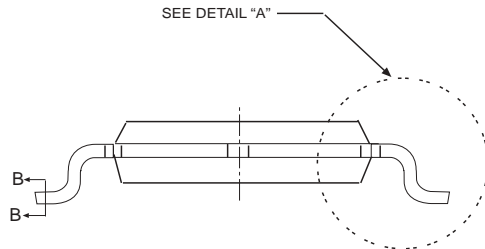
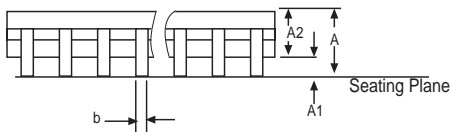
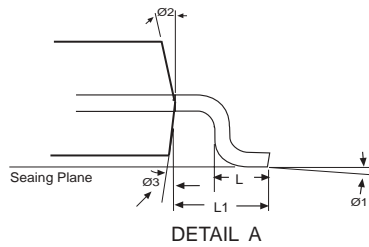
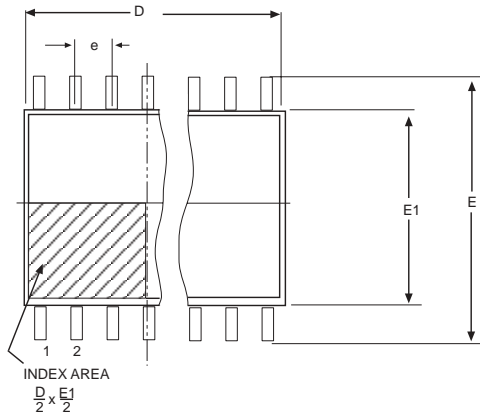
## 20 PIN SSOP

**PACKAGE: PLASTIC  
SMALL OUTLINE (SOIC)  
(WIDE)**

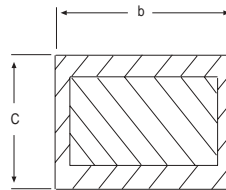


DIMENSIONS (Inches) Minimum/Maximum (mm)	28-PIN
A	0.090/0.104 (2.29/2.649)
A1	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)
D	0.697/0.713 (17.70/18.09)
E	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)
$\emptyset$	0°/8° (0°/8°)

# PACKAGE: 20 PIN TSSOP

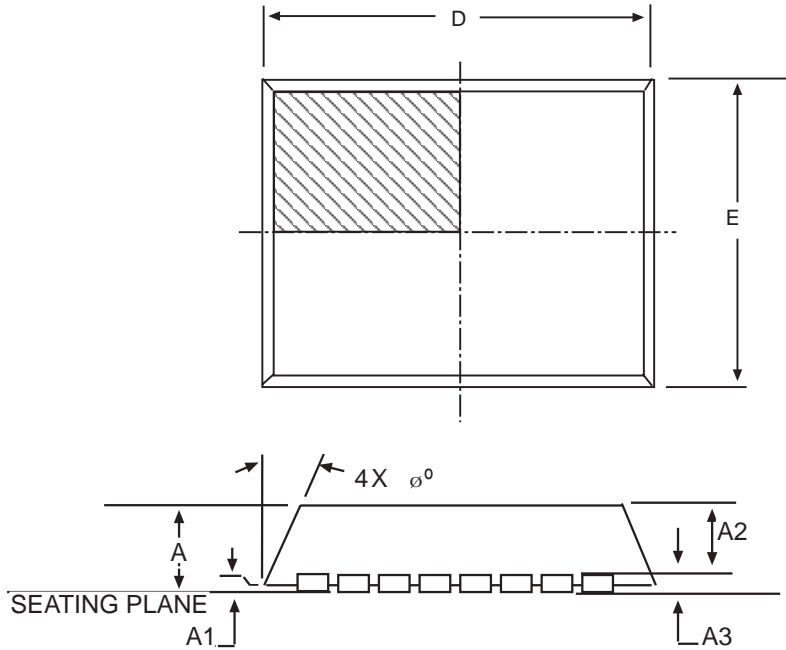


20 PIN TSSOP JEDEC MO-153 (AC) Variation	Dimensions in (mm)		
	MIN	NOM	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	6.40	6.50	6.60
E	6.40 BSC		
E1	4.30	4.40	4.50
e	0.65 BSC		
Ø1	0°	-	8°
Ø2	12° REF		
Ø3	12° REF		
L	0.45	0.60	0.75
L1	1.00 REF		

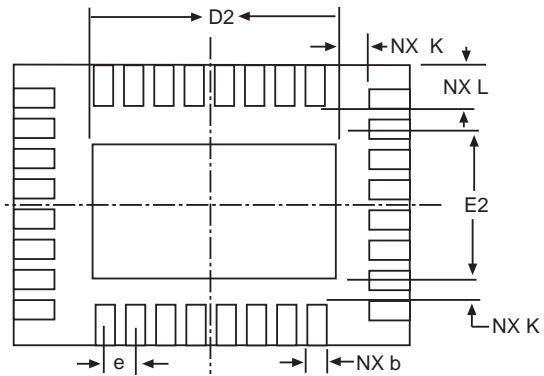


## 20 PIN TSSOP

# PACKAGE: 32 PIN QFN



32 PIN QFN JEDEC MO220 (VHHD-4)	Dimensions in (mm)		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	0	0.65	1.00
A3	0.20 REF		
D	5.00 BSC		
E	5.00 BSC		
e	0.50 BSC		
b	0.18	0.25	0.30
∅	0°	-	14°
D2	3.50	3.65	3.80
E2	3.50	3.65	3.80
L	0.35	0.40	0.45
K	0.20	-	-
N	32		
ND	8		
NE	8		



32 PIN QFN



## ORDERING INFORMATION

Part Number	Temperature Range	Package Types
SP3223EUCP .....	0°C to +70°C .....	20-pin PDIP
SP3223EUCA .....	0°C to +70°C .....	20-pin SSOP
SP3223EUCA/TR .....	0°C to +70°C .....	20-pin SSOP
SP3223EUCY .....	0°C to +70°C .....	20-pin TSSOP
SP3223EUCY/TR .....	0°C to +70°C .....	20-pin TSSOP
SP3243EUCT .....	0°C to +70°C .....	28-pin WSOIC
SP3243EUCT/TR .....	0°C to +70°C .....	28-pin WSOIC
SP3243EUCA .....	0°C to +70°C .....	28-pin SSOP
SP3243EUCA/TR .....	0°C to +70°C .....	28-pin SSOP
SP3243EUCY .....	0°C to +70°C .....	28-pin TSSOP
SP3243EUCY/TR .....	0°C to +70°C .....	28-pin TSSOP
SP3243EUCR .....	0°C to +70°C .....	32-pin QFN
SP3223EUJEP .....	-40°C to +85°C .....	20-pin PDIP
SP3223EUJEA .....	-40°C to +85°C .....	20-pin SSOP
SP3223EUJEA/TR .....	-40°C to +85°C .....	20-pin SSOP
SP3223EUJEY .....	-40°C to +85°C .....	20-pin TSSOP
SP3223EUJEY/TR .....	-40°C to +85°C .....	20-pin TSSOP
SP3243EUJET .....	-40°C to +85°C .....	28-pin WSOIC
SP3243EUJET/TR .....	-40°C to +85°C .....	28-pin WSOIC
SP3243EUJEA .....	-40°C to +85°C .....	28-pin SSOP
SP3243EUJEA/TR .....	-40°C to +85°C .....	28-pin SSOP
SP3243EUJEY .....	-40°C to +85°C .....	28-pin TSSOP
SP3243EUJEY/TR .....	-40°C to +85°C .....	28-pin TSSOP
SP3243EUJER .....	-40°C to +85°C .....	32-pin QFN

Available in lead free packaging. To order add "-L" suffix to part number.

Example: SP3223EUJEA/TR = standard; SP3223EUJEA-L/TR = lead free

/TR = Tape and Reel

Pack quantity is 1,00 for SSOP, TSSOP and WSOIC.



ANALOG EXCELLENCE

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