19-0873; Rev 3; 8/95

MAXIM

5th Order, Zero DC Error, Lowpass Filter

General Description

The MAX280/MXL1062 are 5th-order all-pole instrumentation lowpass filters with no DC error. The filter uses an external resistor and capacitor to isolate the integrated circuit from the DC signal path, thus providing excellent DC accuracy.

The resistor and capacitor, along with the on-chip 4th-order switched capacitor filter, form a 5th-order lowpass filter. Two MAX280/MXL1062s can be cascaded to form a 10th-order lowpass filter.

The filter cutoff frequency is set by an internal clock which can be externally driven. The clock to cutoff-frequency ratio is 100:1, allowing clock ripple to be easily removed.

The MAX280 is an enhanced version of the MXL1062. Enchancements include tighter specifications on the internal clock oscillator frequency and the buffer amplifier offset voltage.

Applications

Anti-Aliasing Filter
Data Loggers
Digital Voltmeters
Weigh Scales
Strain Gauges

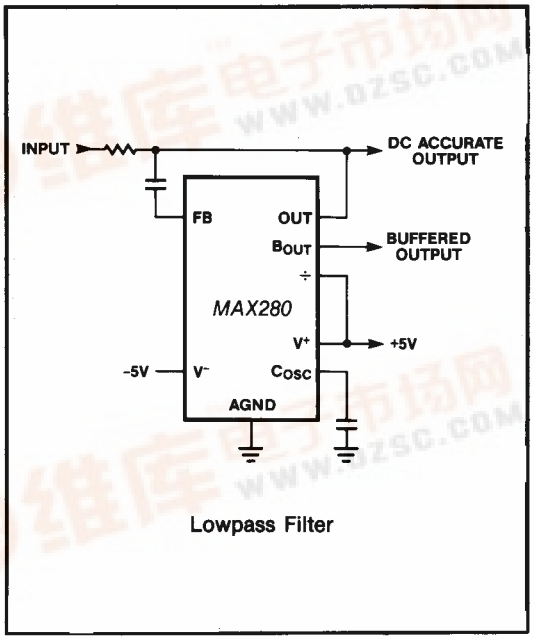
Features

- Lowpass Filter with No DC Error
- Low Passband Noise
- DC to 20kHz Cutoff Frequency
- 5th Order All Pole Filter
- Internal or External Clock
- Cascadable for Higher Order Rolloff
- Buffered Output Available
- 8-Pin DIP or 16-Pin SOIC

Ordering Information

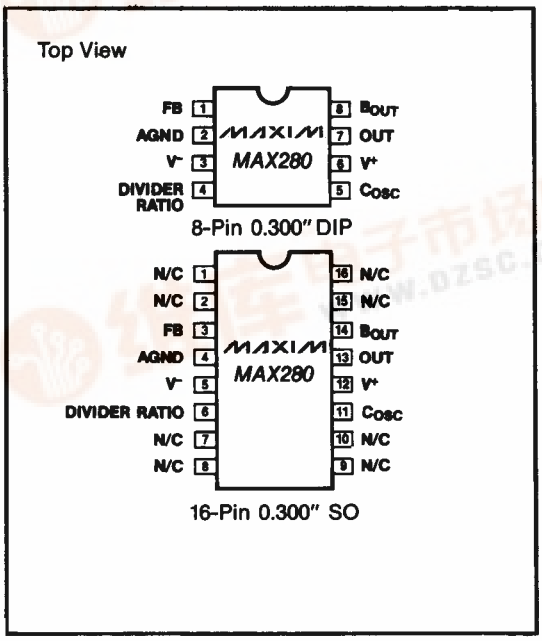
PART	TEMP. RANGE	PIN-PACKAGE
MAX280CPA	0°C to +70°C	8 Lead Plastic DIP
MAX280CWE	0°C to +70°C	16 Lead-Wide SO
MAX280EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX280EWE	-40°C to +85°C	16 Lead Wide SO
MAX280MJA	-55°C to +125°C	8 Lead CERDIP
MXL1062CN8	-40°C to +85°C	8 Lead Plastic DIP
MXL1062CJ8	-40°C to +85°C	8 Lead CERDIP
MXL1062CS	-40°C to +85°C	16 Lead Wide SO
MXL1062MJ8	-55°C to +125°C	8 Lead CERDIP

Typical Operating Circuit



Lowpass Filter

Pin Configurations



5th Order, Zero DC Error, Lowpass Filter

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V-) 18V
Input Voltage at Any Pin ..... V- -0.3V ≤ V_{IN} ≤ V+ +0.3V
Operating Temperature
MAX280CXX/MXL1062C ..... 0°C to +70°C
MAX280EXX ..... -40°C to +85°C
MAX280MXX/MXL1062M ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature Range (Soldering, 10sec) ..... +300°C
Power Dissipation
Plastic DIP (derate 6.25mW/°C above 70°C) 500mW
CERDIP (derate 8.00mW/°C above 70°C) 640mW
SO (derate 9.52mW/°C above 70°C) 762mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +5V, V^- = -5V, T_A = 25°C, unless otherwise specified, AC output measured at pin 7, Figure 1.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Dual Supply Single Supply			 ±2.375 4.75		 ±8.0 16.0	V
Power Supply Current	C_{OSC} (Pin 5 to V^-) = 100pF T_A = 25°C T_A = T_{MIN} to T_{MAX}			 5.0 5.0	 7.0 10.0	mA
Input Frequency Range				0-20		kHz
Filter Gain at f_{IN} = 0 f_{IN} = 0.5f_C (Note 1) f_{IN} = f_C f_{IN} = 2f_C f_{IN} = 4f_C	f_{CLK} = 100kHz, Pin 4 at V^+ C = 0.01µF, R = 25.78kΩ T_A = T_{MIN} to T_{MAX} T_A = T_{MIN} to T_{MAX} T_A = T_{MIN} to T_{MAX}		 -2 -28 -54	 0 -0.02 -3 -30 -60	 -0.3 	dB
Clock to Cutoff Frequency Ratio f_{CLK}/f_C	f_{CLK} = 100kHz, Pin 4 at V^+ C = 0.01µF, R = 25.78kΩ			100 ± 1		
Filter Gain at f_{IN} = 16kHz	f_{CLK} = 400kHz, Pin 4 at V^+ C = 0.01µF, R = 6.5kΩ T_A = T_{MIN} to T_{MAX}		-46	-52		dB
f_{CLK}/f_C Tempco	Same as above			10		ppm/°C
Filter Output (Pin 7) DC Swing	Pin 7 buffered with an ext op amp T_A = T_{MIN} to T_{MAX}		±3.5	±3.8		V
Clock Feedthrough				10		mV_{pp}
INTERNAL BUFFER						
Bias Current	T_A = 25°C T_A = T_{MIN} to T_{MAX}			2 170	50 1000	pA
Offset Voltage	 MXL1062			 2	 20	mV
Voltage Swing	R1 = 20kΩ; T_A = T_{MIN} to T_{MAX}		±3.5	±3.8		V
Short Circuit Current Source/Sink				30/2		mA
CLOCK (NOTE 2)						
Internal Oscillator Frequency	C_{OSC} (Pin 5 to V^-) = 100pF					kHz
		MXL1062	25	35	50	
	T_A = T_{MIN} to T_{MAX} C_{OSC} (Pin 5 to V^-) = 100pF					
		MXL1062	15	35	65	
Max Clock Frequency				4		MHz
C_{OSC} Input Sink/Source Current	T_A = T_{MIN} to T_{MAX}			25	80	µA

Note 1: f_C is the frequency where the gain is -3dB with respect to the input signal.
Note 2: The external or driven clock frequency is divided by either 1, 2, or 4 depending upon the voltage at pin 4. When pin 4 = V^+, f_{CLK}/f_C = 100; when pin 4 = GND, f_{CLK}/f_C = 200; pin 4 = V^-, f_{CLK}/f_C = 400.

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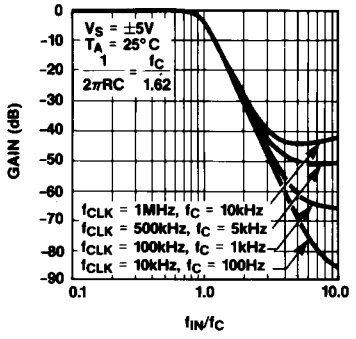
Pin Description

PIN #	NAME	FUNCTION
1	FB	External capacitor couples to the chip through this pin.
2	AGND	Ground. Connect to system ground for dual supply operation or mid-supply for single operation. This pin should be well bypassed using a large capacitor for single supply operation.
3	V^-	Negative supply voltage
4	DIVIDER RATIO	The oscillator frequency is divided by either 1, 2, or 4 depending upon the voltage on this pin. This in turn gives a clock to cutoff frequency ratio when tied to V^+ of 100:1; when tied to GND of 200:1; and when tied to V^- of 400:1.

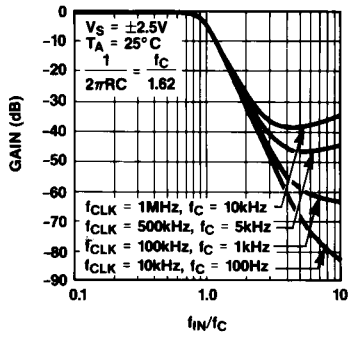
PIN #	NAME	FUNCTION
5	C_{OSC}	Clock input pin for external clock applications. For internal clock operation connect an external capacitor between this pin and V^-.
6	V^+	Positive supply voltage
7	OUT	Input to on-chip buffer amplifier
8	B_{OUT}	Output of buffer amplifier

Typical Operating Characteristics

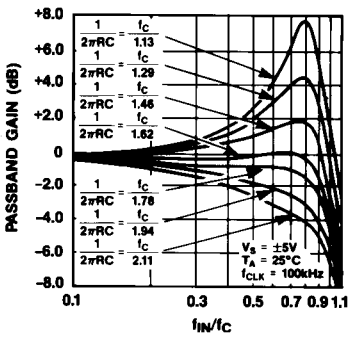
GAIN NORMALIZED TO CUTOFF FREQUENCY (V_S = ±5V)



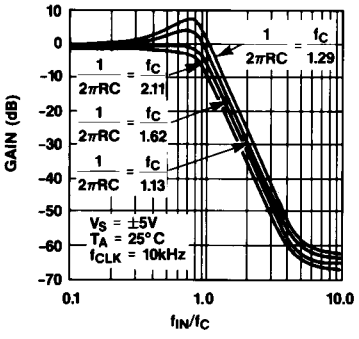
GAIN NORMALIZED TO CUTOFF FREQUENCY (V_S = ±2.5V)



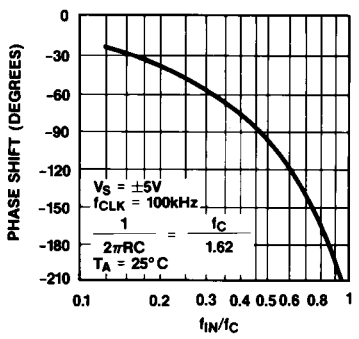
PASSBAND GAIN vs. INPUT FREQUENCY



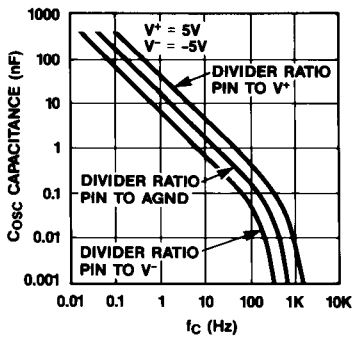
GAIN vs. INPUT FREQUENCY



PASSBAND PHASE SHIFT vs. INPUT FREQUENCY



CUTOFF FREQUENCY vs. C_{OSC}



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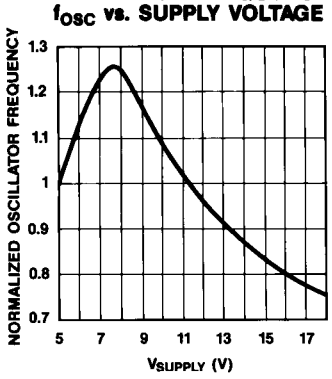
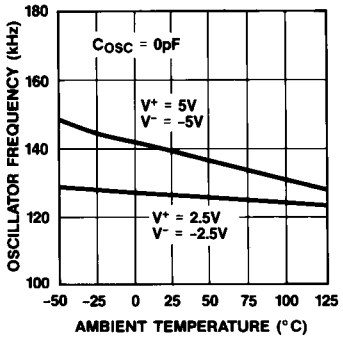
Typical Operating Characteristics (continued)

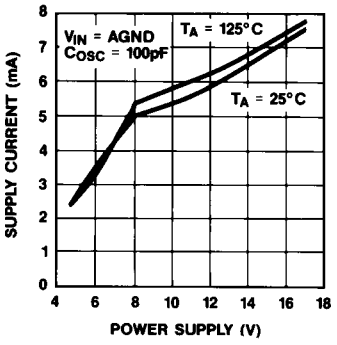
NORMALIZED OSCILLATOR FREQUENCY f_{OSC} vs. SUPPLY VOLTAGE



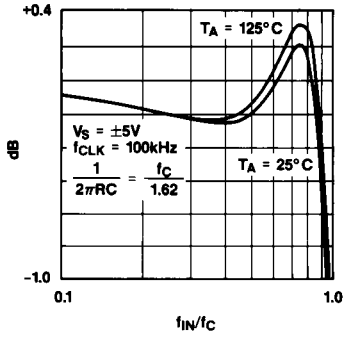
OSCILLATOR FREQUENCY, f_{OSC} vs. AMBIENT TEMPERATURE



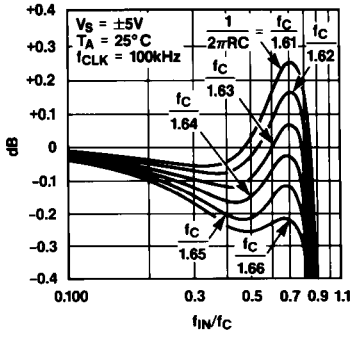
POWER SUPPLY CURRENT vs. POWER SUPPLY VOLTAGE



VARIATION OF PASSBAND GAIN WITH TEMPERATURE



PASSBAND GAIN vs. INPUT FREQUENCY



Introduction

Figure 1 illustrates the architecture of the circuit. The output voltage is sensed through an internal buffer, then applied to an internal switched capacitor network which drives the bottom plate of an external capacitor to form a 5th order lowpass filter. The input and output appear across an external resistor and the IC part of the overall filter handles only the AC path of the signal. The DC offsets of the buffer and the switched capacitor network are blocked by the capacitor and do not appear at the zero offset output pin.

Use of this external resistor and capacitor also automatically provides the required anti-aliasing filtering for the sampled filter. Further, low frequency noise in the filter IC is attenuated by the external capacitor since any noise at the FB pin goes through a highpass path to the filter output. The filter output pin is unbuffered. This signal can be buffered by the on-chip buffer or by a high accuracy op amp (such as a chopper stabilized op amp) to obtain a buffered DC accurate system. The on-chip buffer has an offset voltage of 2mV for the MAX280 and 20mV for the MXL1062. The offset voltage for both devices have a typical tempco of 1µV/°C.

Detailed Description

Clock Requirements

Using Divider Ratio

DIVIDER RATIO sets the ratio between the internal f_{CLK} (supplied to the MAX280/MXL1062) and f_{OSC} (the output at the DIVIDER RATIO pin). Connect DIVIDER RATIO to V^+ for a 1/1, to GND for a 1/2, and to V^- for a 1/4 f_{CLK}/f_{OSC} ratio.

Using Internal Oscillator

The internal 140kHz (nominal) oscillator frequency can be modified by connecting an external capacitor

in parallel with the on-chip 33pF capacitor; from the C_{OSC} pin to GND (or to V^- if the capacitor is polarized).

The clock frequency can be calculated by:

$$f_{OSC} = 140kHz\ (33pF/(33pF+C_{OSC}))\ (1)$$

Due to process tolerances, f_{OSC} can vary by ±62.5% in the MXL1062. In the MAX280, on-chip trimming reduces the f_{OSC} tolerance to ±19.5%. The oscillator frequency can be adjusted by adding a series potentiometer between the capacitor and the C_{OSC} pin as shown in Figure 2. The new frequency can be computed as:

$$f'_{OSC} = f_{OSC}/(1-4RC_{OSC}f_{OSC})\ (2)$$

where f_{OSC} is the value of the oscillator frequency when R = 0. When an external potentiometer is used, the new value of the oscillator frequency is always higher than the one calculated in (equation 1). To achieve a wide tuning range, calculate (equation 1) the ideal f_{OSC}, C_{OSC} pair, then double the value of C_{OSC} and use a 50k potentiometer to adjust f'_{OSC}. For example: to obtain a 1kHz oscillator frequency, C_{OSC} is 3900pF. By using 6800pF for C_{OSC} and a 50kΩ potentiometer, the clock frequency can be adjusted from 500Hz to 1.56kHz. The internal oscillation frequency can be measured directly at the C_{OSC} pin using a low capacitance probe.

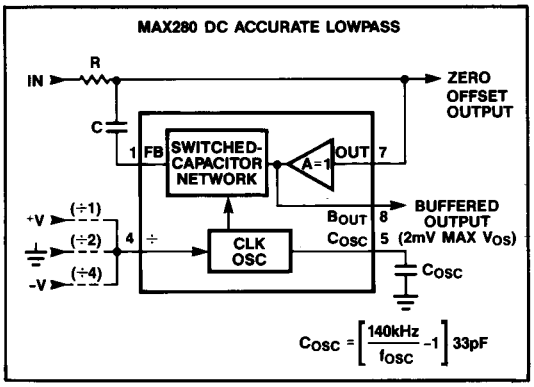


Figure 1. Block Diagram

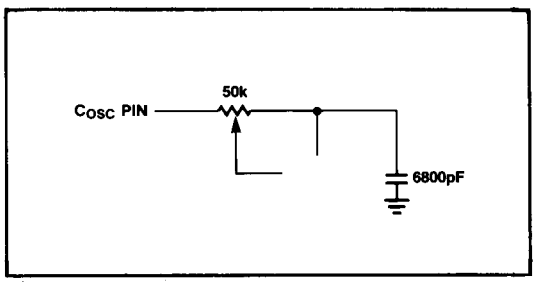


Figure 2. External Oscillator Trim

Using an External Clock

The internal switched capacitor filter requires a clock 100 times higher than the desired cutoff frequency. If an external clock is used the input on the C_{OSC} pin must swing close to the power rails (V^+,V^-). Although standard 74HC00 series CMOS gates do not guarantee CMOS levels with the source and sink currents of the C_{OSC} pin, they will in reality drive the C_{OSC} pin. CMOS gates conforming to standard B series output drive have the appropriate voltage levels and current to simultaneously drive several chips. The typical trip levels of the internal Schmitt trigger sensing C_{OSC} pin are:

POWER SUPPLY		TRIP LEVEL	
V^+ = +2.5V	V^- = -2.5V	V_{IH} = 0.9V	V_{IL} = -1.15V
V^+ = +5.0V	V^- = -5.0V	V_{IH} = 1.4V	V_{IL} = -2.1V
V^+ = +6.0V	V^- = -6.0V	V_{IH} = 1.7V	V_{IL} = -2.5V
V^+ = +5.0V	V^- = 0V	V_{IH} = 3.4V	V_{IL} = 1.35V
V^+ = +10V	V^- = 0V	V_{IH} = 6.4V	V_{IL} = 2.9V
V^+ = +15V	V^- = 0V	V_{IH} = 9.5V	V_{IL} = 4.1V

Choosing External Resistor and Capacitor Values

The external resistor and capacitor is used as part of a feedback loop for the filter and also forms one pole. The internal 4 pole switched capacitor filter is driven by a clock which also determines the filter cutoff frequency. For a maximally flat amplitude response, the clock should be 100 times the desired cutoff frequency and the resistor and capacitor should be chosen such that:

$$\frac{f_C}{1.62} = \frac{1}{2\pi RC}$$

where f_C = filter cutoff frequency, (-3dB point)

For example to implement a 10Hz cutoff filter, a 1kHz clock is required with $1/2\pi RC$ = 10Hz/1.62 = 6.17Hz.

Typically R is chosen to be around 20kΩ. The minimum value of R depends upon the maximum input signal, and the current sinking capability of the FB pin (typically 1mA). So for a 1V peak-to-peak signal, the minimum value of the resistor is 1kΩ.

The passband response for values of $1/(2\pi RC)$ around (f_C/1.62) can be seen on the Passband Gain vs. Input Frequency plot (see Typical Operating Characteristics). If maximum flatness is required (as in Butterworth filters), the RC product should be well controlled. When the input resistor and capacitor cutoff frequency approaches the cutoff frequency of the on-chip 4th order filter, response peaking becomes severe as can be seen in the response plots. However the attenuation slope is virtually unaffected by the resistor and capacitor since it is set by internal circuitry. This can be seen in the Gain vs. Input Frequency plot.

For wide temperature range applications NPO ceramic capacitors are recommended. Their tempcos are around ±20ppm and values are available to 0.1μF.

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Other ceramic capacitors are not recommended due to their large tempcos. Mylar, polystyrene and polypropylene capacitors all provide acceptable performance. Solid tantalum capacitors connected back-to-back and disc ceramic capacitors introduce additional passband errors (0.05-0.1dB).

Applications Information

Filter Input Voltage Range

Every node of the filter typically swings within 1V of both supplies. With the appropriate external resistor and capacitor values, the amplitude response of all the internal and external nodes should not exceed a gain of 0dB with the exception of the FB pin. The amplitude response of the FB pin, where some peaking may occur, is shown in Figure 3. For an input frequency around $0.8f_C$, the gain is 1.7V/V and, with ±5V supplies, the peak-to-peak input voltage should not exceed 4.7V. If the input voltage goes beyond this value, clipping and distortion of the output waveform may occur; however, the filter will not be damaged. The absolute maximum input voltage to any pin should not exceed the power supplies.

Internal Buffer

The internal output buffer of the FB pin and the OUT pin is part of the AC signal path. Hence capacitive loading greater than 30pF may cause gain errors in the passband around the cutoff frequency. The internal buffer can also be used as the filter output, however, there will be a few millivolts of output offset.

Filter Attenuation

The rolloff is 30dB/octave. When the clock rate is increased and hence the cutoff frequency is increased, the filter's maximum attenuation decreases as shown in the Typical Operating Characteristics. This decrease is caused by rolloff at higher frequencies of the loop gains of the various internal feedback paths and is not due to any increase in noise floor.

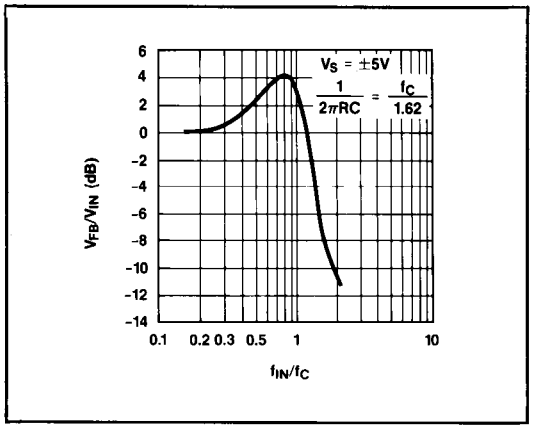

Figure 3. Amplitude Response of FB Pin

Filter Noise

The filter wideband noise is typically $90\mu V_{RMS}$ with ±5V supplies and typically $80\mu V_{RMS}$ for ±2.5V supplies or a +5V single supply. This value is nearly independent of the cutoff frequency. The noise spectral density, unlike conventional active filters, is nearly zero for frequencies below 0.1 f_C. Roughly 2/3 of the entire wideband noise is in the band DC to f_C.

Transient Response

Figure 4A shows the step response of the filter. This response approximates that of an ideal 5th order maximally flat (Butterworth) filter. The ringing in the transient response can be reduced by using a Bessel filter. The Bessel filter response can be approximated by setting $1/2\pi RC$ to $f_C/2$ instead of $f_C/1.62$. Figure 4B shows the step response of the Bessel approximation.

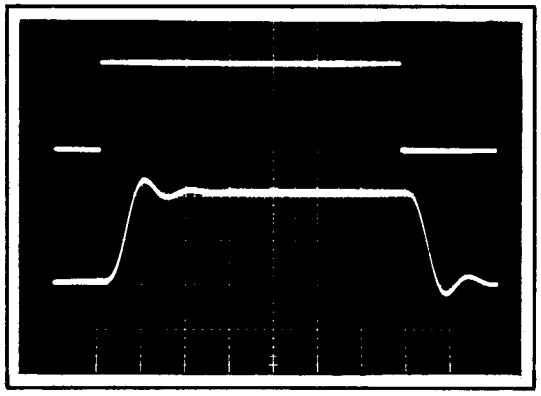

Figure 4A. Step Response of Butterworth Approximation

$\frac{1}{2\pi RC} = \frac{f_C}{1.62}$, *(1mS/div., 0.5V/div.)*

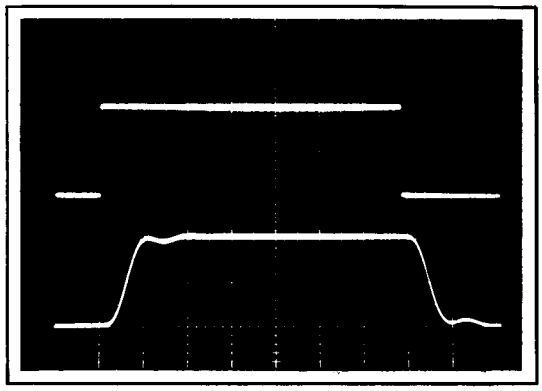

Figure 4B. Step Response of Bessel Approximation

$\frac{1}{2\pi RC} = \frac{f_C}{2}$ *(1mS/div., 0.5V/div.)*

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Anti-Aliasing

The internal 4th order switched capacitor filter is a sampled device and as such will alias unless preceded by a band limited signal, or a continuous non-sampled filter. The external resistor and capacitor used to form the 5th filter pole also automatically provides this function. Attenuation is greater than 43dB at the Nyquist frequency.

Single Supply Operation

Figure 5 shows a schematic for single supply operation. The AGND pin and the OUT pin should be biased at 1/2 supply. The value of the resistors R1 and R2 should be chosen to conduct 100μA or more. R' DC biases the buffer and C' isolates the buffer from the DC value of the output. Under these conditions the external resistor and capacitor should be adjusted such that $(1/2\pi RC) = f_C/1.84$. This accounts for the extra loading of the R',C' combination. R' and C' are not required if the input voltage has a DC value around 1/2 supply. If an external capacitor is used to activate the internal oscillator, its bottom plate should be tied to system ground. The AGND pin should also be bypassed by a decoupling capacitor.

Clock Feedthrough

Clock feedthrough can be reduced by using a resistor and capacitor at the buffered output pin provided that this pin is used as an output. If an external op amp is used to buffer the DC accurate output, an input resistor and capacitor can be used to eliminate clock feedthrough (see Figure 6) and further reduce the attenuation floor of the filter.

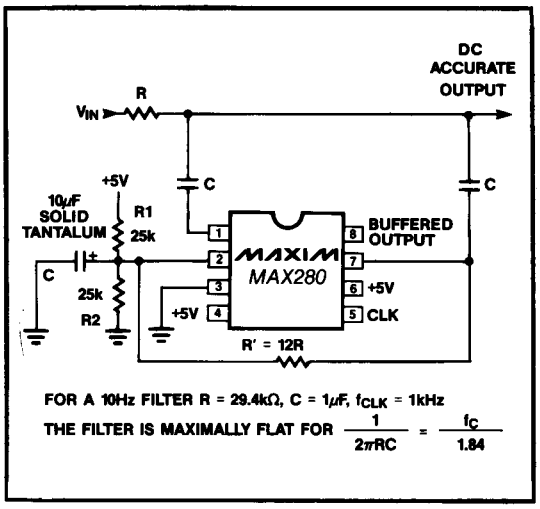
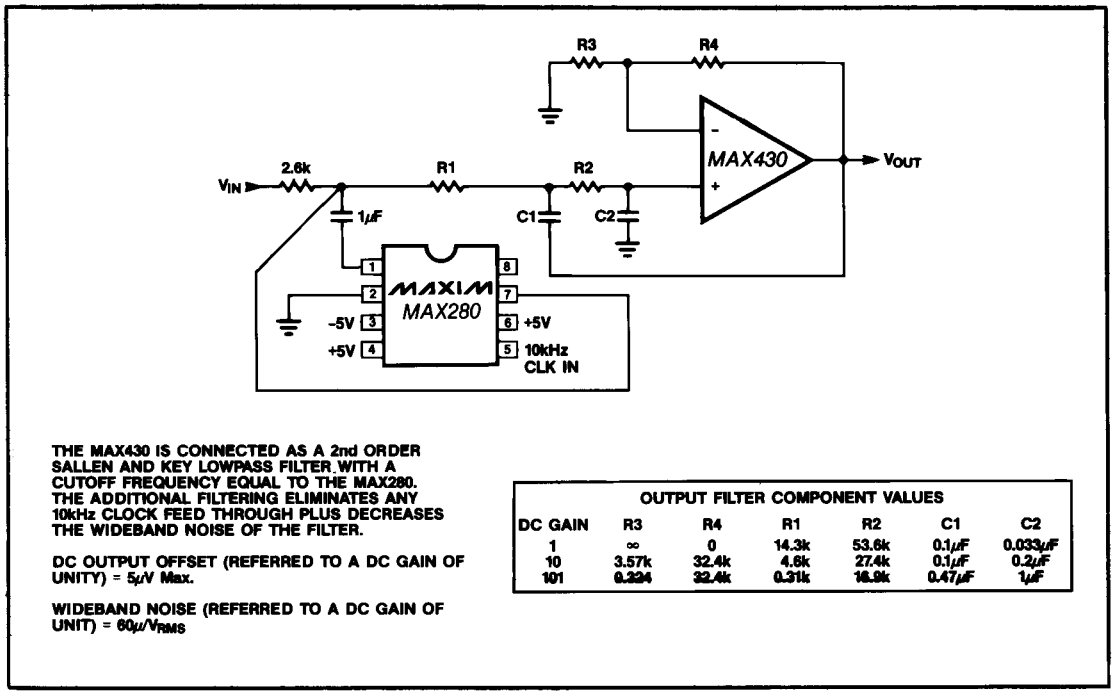


Figure 5. Single 5V Supply 5th Order LP Filter



OUTPUT FILTER COMPONENT VALUES

DC GAIN	R3	R4	R1	R2	C1	C2
1	∞	0	14.3k	53.6k	0.1μF	0.033μF
10	3.57k	32.4k	4.6k	27.4k	0.1μF	0.2μF
101	0.324	32.4k	0.31k	16.9k	0.47μF	1μF

Figure 6. 7th Order 100Hz Lowpass Filter with Continuous Output Filtering, Output Buffering and Gain Adjustment

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Cascading for Higher Order Filters

Two chips can be cascaded with or without intermediate buffers. Figure 7A shows a DC accurate 10th order lowpass filter. The unbuffered output of the first chip directly drives the next stage input. To minimize loading the first resistor and capacitor, the next stage R′ should be much larger. The recommended ratio of R/R′ is 117:1. The values chosen were $1/(2\pi RC) = f_C/1.57$ and $1/(2\pi R'C') = f_C/1.6$. For example, for f_C = 4.16kHz, f_{CLK} = 416kHz, R = 909Ω, R′ = 107kΩ, C = 0.066μF, C′ = 574pF. For this example the maximum passband error occurs around $0.5f_C$ and is -0.6dB. Figure 6B corrects for loading the buffered output when the first stage is used to drive the input of the next stage. This introduces a maximum DC error of 2mV over temperature using the MAX280. Now R and R′ can be similar in value and the passband gain error is reduced typically -0.15dB. The RC values used were $1/(2\pi RC) = f_C/1.59$ and $1/(2\pi R'C') = f_C/1.64$.

Creating Notch Filters

The MAX280/MXL1062 can be used to create a notch because the frequency, where it exhibits -180° phase shift, is inside its passband as shown in Figure 8A. It is repeatable and predictable from part-to-part. An input signal can be summed with the output of the filter to form a notch as shown in Figure 8B. The 180° phase shift of the MAX280/MXL1062 occurs at f_{CLK}/118.3 or 0.85 times the lowpass cutoff frequency. For instance, to obtain a 60Hz notch, the clock frequency should be 7.098kHz and the input $(1/2\pi RC)$ should be approximately 70.98Hz/1.63. The optional (R2C2) at the output filters the clock feedthrough. The $1/2\pi R2C2$ should be 12-15 times the notch frequency. The major advantage of this notch is its wide bandwidth. The input frequency range is not limited by the clock frequency because the MAX280/MXL1062 by itself does not alias.

The circuit of Figure 8C is an extension of the previous notch filter. The input signal is summed with the lowpass filter output through A1, as previously described; then, the output of A1 is again summed with the input voltage through A2.

R6 = R2 = R3 = R7 and R4 = R5 = 0.5R7, the output of A2, at least theoretically, should look like the output of MAX280/MXL1062, the B_{OUT} pin. If the ratio of

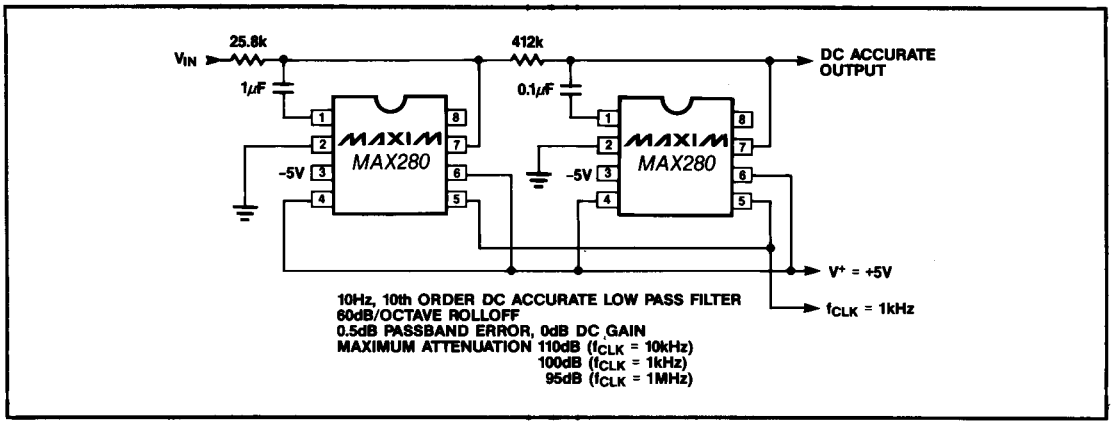


Figure 7A. Simple Cascading Technique

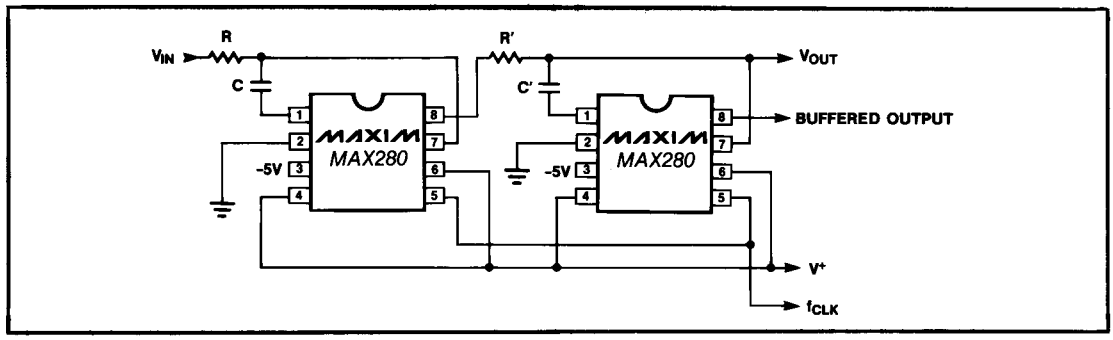


Figure 7B. Cascading Two MAX280/MXL1062s. The 2nd Stage is Driven by the Buffered Output of the First Stage.

(R6/R5) is slightly less than 2, a notch is introduced in the stopband of the filter as shown in Figure 8D. The overall filter response looks pseudoelliptic low-pass. The frequency of the notch is at $f_{CLK}/47.3$ and the value of the resistor ratio (R6/R5) should be equal to 1.935.

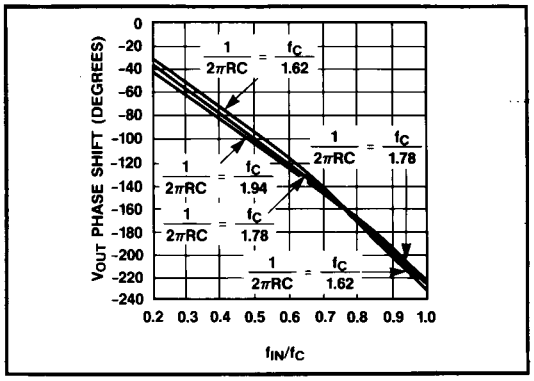


Figure 8A. Phase Response of the MAX280/MXL1062 for Various Input (R, C)s

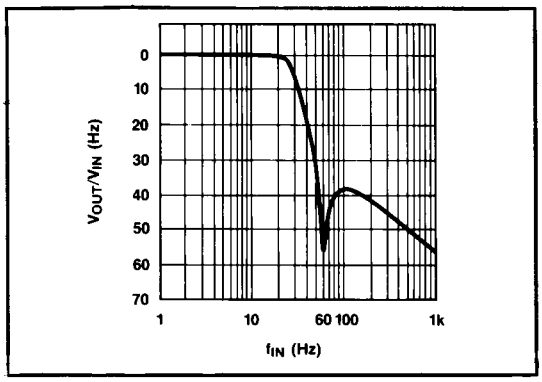


Figure 8D. Amplitude Response of the Filter

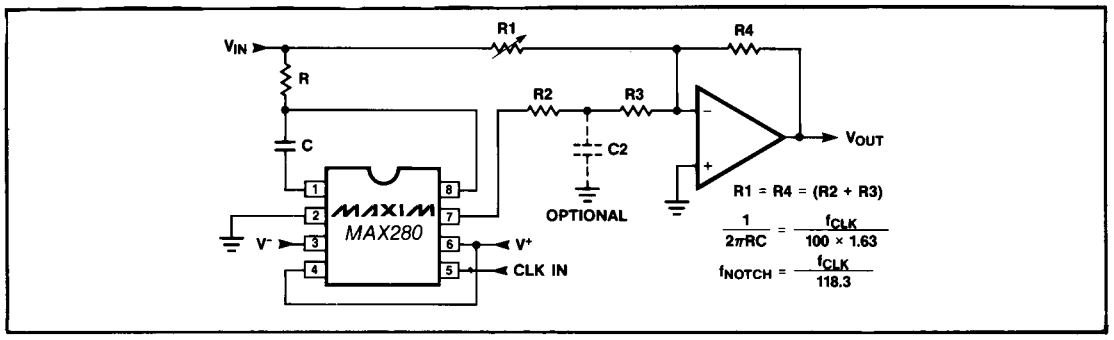


Figure 8B. Using the MAX280/MXL1062 to Create a Notch

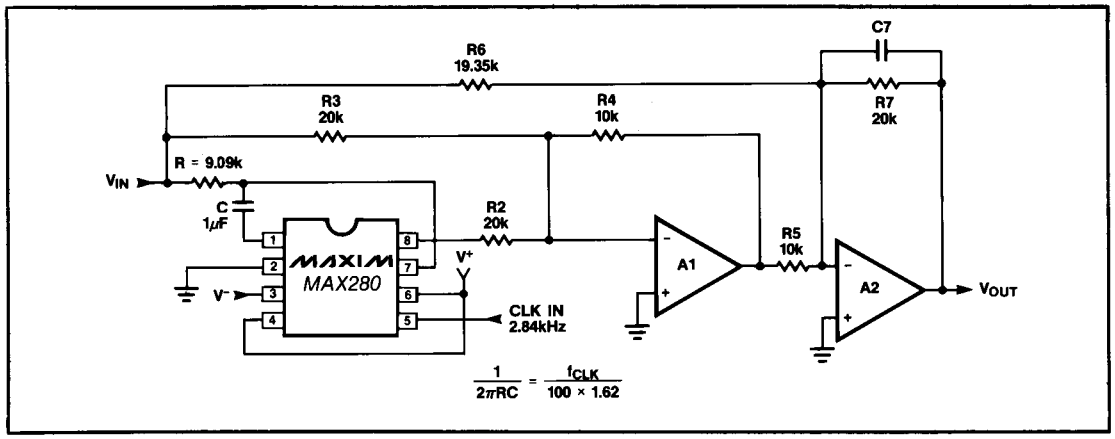
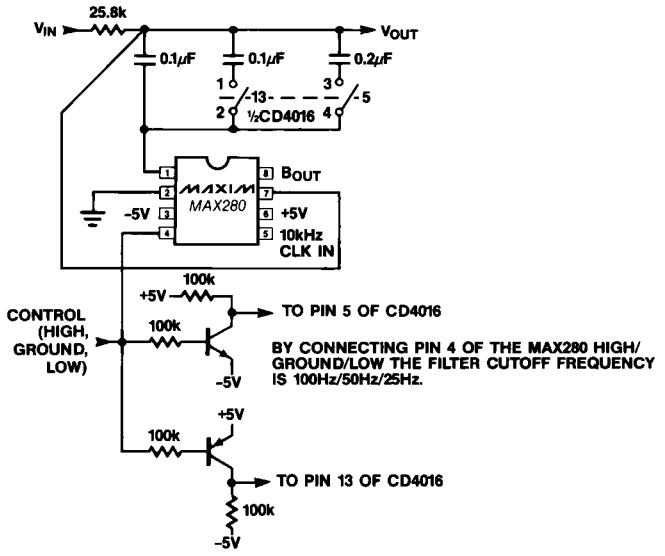


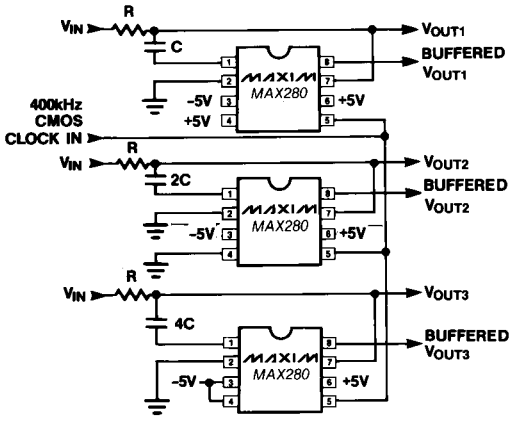
Figure 8C. A Lowpass Filter with a 60Hz Notch

5th Order, Zero DC Error, Lowpass Filter

Application Circuits

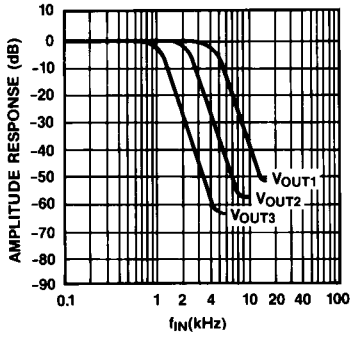


100Hz, 50Hz, 25Hz 5th Order DC Accurate LP Filter

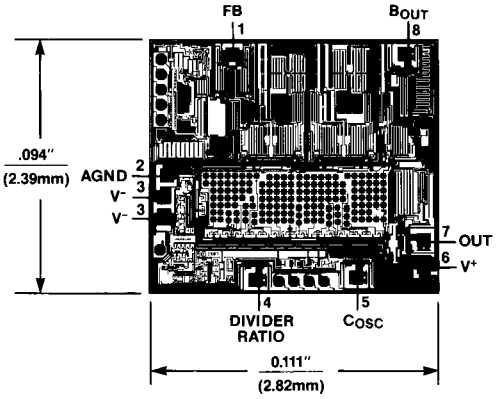


Octave Tuning with a Single Input Clock

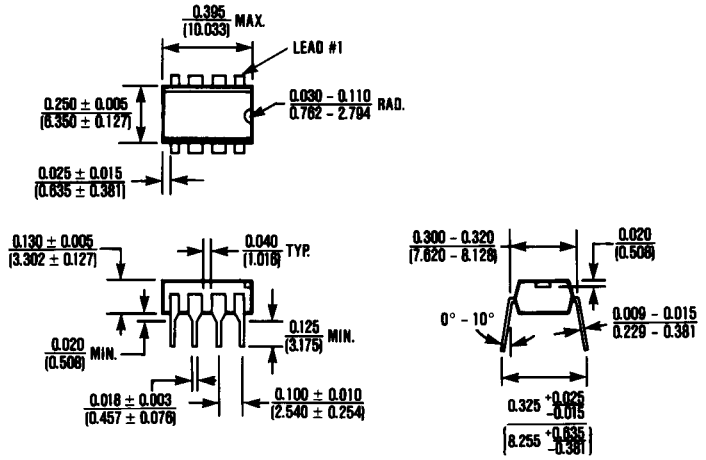
Amplitude Response for the Octave Tuning Circuit



Chip Topography



Package Information



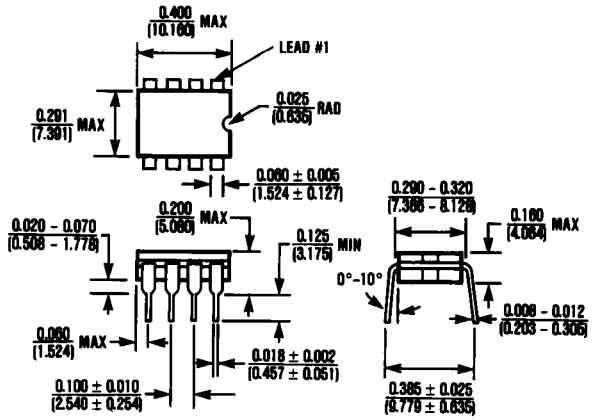
8 Lead Plastic DIP (PA)

θ_{JA} = 160°C/W

θ_{JC} = 75°C/W

5th Order, Zero DC Error, Lowpass Filter

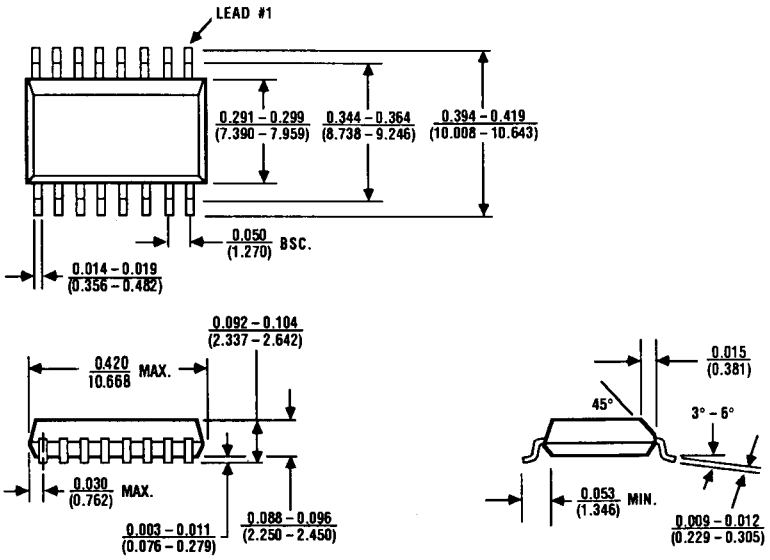
Package Information (continued)



8 Lead CERDIP (JA)

θ_{JA} = 125°C/W

θ_{JC} = 55°C/W



16 Lead Small Outline, Wide (WE)

θ_{JA} = 105°C/W

θ_{JC} = 60° C/W