

19-2763; Rev 1; 6/96

MAXIM

Calibrated 4-Channel 12-Bit ADC

MX7582

General Description

The MX7582 is a complete, calibrated 4-channel 12-bit A/D converter which maintains true 12-bit performance over the full operating temperature range without external adjustments. In addition, each 100 μ s conversion includes an auto-zero cycle which reduces zero errors to typically below 100 μ V.

CHIP SELECT, READ, and WRITE inputs are included for easy microprocessor interfacing without additional logic. 2-byte, 12-bit conversion data is provided over an 8-bit three-state output bus. Either byte may be read first. Two address bits control the 4-channel input multiplexer.

The MX7582's analog input range is 0V to +5V when using a +5V reference. All four high-impedance input channels have excellent matching (typically 0.05LSB).

Applications

- Digital-Signal Processing
- Audio and Telecom Processing
- High-Accuracy Process Control
- High-Speed Data Acquisition

Features

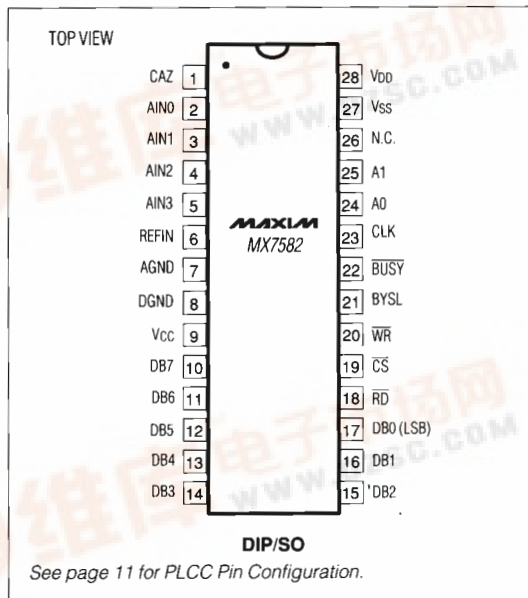
- ◆ True 12-Bit Performance without Adjustments
- ◆ Minimum External Components
- ◆ Four High-Impedance Input Channels
- ◆ Zero Error Typically <100 μ V
- ◆ Standard Microprocessor Interface
- ◆ 28-Pin DIP, Wide SO, and PLCC Packages

Ordering Information

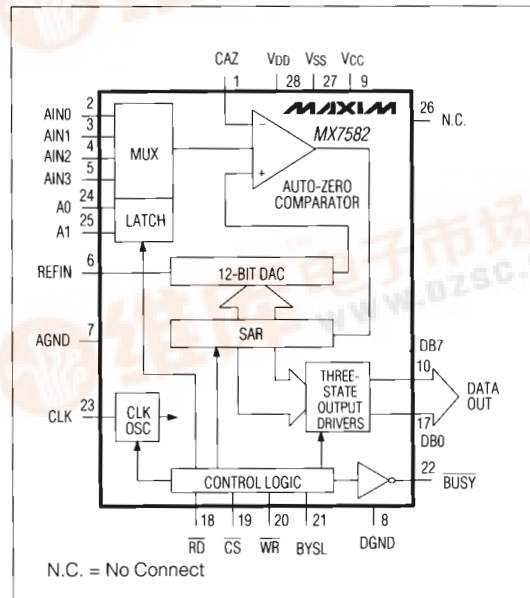
PART	TEMP. RANGE	PIN-PACKAGE
MX7582KN	0°C to +70°C	28 Plastic DIP
MX7582KCWI	0°C to +70°C	28 Wide SO**
MX7582KP	0°C to +70°C	28 PLCC
MX7582K/D	0°C to +70°C	Dice**
MX7582KEWI	-40°C to +85°C	28 Wide SO**
MX7582BQ	-40°C to +85°C	28 CERDIP*
MX7582BD	-40°C to +85°C	28 Ceramic SB
MX7582TQ	-55°C to +125°C	28 CERDIP*
MX7582TD	-55°C to +125°C	28 Ceramic SB

* Maxim reserves the right to ship Ceramic SB in lieu of CERDIP packages.
 ** Consult factory.

Pin Configurations



Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

V _{DD} to DGND	-0.3V, +17V	Power Dissipation (any Package)	
V _{SS} to DGND	+0.3V, -7V	to +75°C	100mW
AGND to DGND	-0.3V, REFIN +0.3V	Derate above +75°C by	10mW/°C
V _{CC} to V _{DD}	-0.3V, V _{DD} +0.3V	Operating Temperature Ranges	
V _{CC} to DGND	-0.3V, +7V	MX7582KCWI/KD/KN/KP	0°C to +70°C
REFIN to AGND	-0.3V, V _{DD} +0.3V	MX7582BD/BQ/KEWI	-40°C to +85°C
AIN0-AIN3 to AGND	-0.3V, V _{DD} +0.3V	MX7582TD/TQ	-55°C to +125°C
Digital Input Voltage to DGND	-0.3V, V _{DD} +0.3V	Storage Temperature Range	-65°C to +150°C
Digital Output Voltage to DGND	-0.3V, V _{DD} +0.3V	Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +15V, V_{CC} = +5V, V_{SS} = -5V, REFIN = +5.0V, f_{CLK} = 140kHz external, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution			12			Bits
Total Unadjusted Error (Note 1)	TUE				±1	LSB
Differential Nonlinearity	DNL	No missing codes guaranteed			±3/4	LSB
Full-Scale Error (Gain Error)		All channels, AIN0-AIN3			±1/4	LSB
Full-Scale Tempco		All channels, AIN0-AIN3		0.25		ppm/°C
Offset Error		All channels, AIN0-AIN3			±1/4	LSB
Offset Tempco		All channels, AIN0-AIN3		0.25		ppm/°C
Channel-to-Channel Mismatch		All channels, AIN0-AIN3			±1/4	LSB
ANALOG INPUT						
Input Voltage Range		REFIN = +5.0V	0		+5	V
On-Channel Input Capacitance	C _{AIN}			8		pF
Input Leakage Current	I _{AIN}	AIN0-AIN3; 0V to +5V T _A = +25°C T _A = T _{MIN} to T _{MAX}			10 100	nA
REFERENCE INPUT						
REFIN Range	V _{REFIN}	For specified performance		+5 ±5%		V
		Degraded transfer accuracy	+4		+6	
REFIN Input Current		REFIN = +5.0V			1.0	mA

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ELECTRICAL CHARACTERISTICS (continued)

(VDD = +15V, VCC = +5V, VSS = -5V, REFIN = +5.0V, fCLK = 140kHz external, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS (RD, CS, WR, BYSL, A0, A1)						
Input High Voltage	VIH	VCC = +5V ±5%	+2.4			V
Input Low Voltage	VIL	VCC = +5V ±5%			+0.8	V
Input Current	IIN	VIN = 0 to VCC; TA = +25°C TA = TMIN to TMAX			±1 ±10	μA
Input Capacitance	CIN	(Note 2)			10	pF
CLOCK						
Input High Voltage	VIH	VCC = +5V ±5%	+3.0			V
Input Low Voltage	VIL	VCC = +5V ±5%			+0.8	V
Input High Current	IiH	VCC = +5V ±5%			+1.5	mA
Input Low Current	IiL	VCC = +5V ±5%			±10	μA
LOGIC OUTPUTS (DB0-DB7, BUSY)						
Output High Voltage	VOH	VCC = +5V ±5%, ISOURCE = 200μA	+4.0			V
Output Low Voltage	VOL	VCC = +5V ±5%, ISINK = 1.6mA			+0.4	V
Floating State Leakage Current (DB0-DB7)	ILKG	VOUT = 0V to VCC			±1	μA
Floating State Output Capacitance (DB0-DB7)	COUT	(Note 2)			15	pF
CONVERSION TIME (Note 3)						
With External Clock		fCLK = 140kHz	100			μs
With Internal Clock		TA = +25°C. Use clock components shown in Figure 6.	100		150	μs
POWER REQUIREMENTS (Note 4)						
Power-Supply Voltage	VDD			+15		V
	VSS			-5		
	VCC			+5		
VDD Supply Rejection		VDD = +14.25V to +15.75V, VSS = -5V		±0.03		LSB
VSS Supply Rejection		VSS = -4.75V to -5.25V, VDD = +15V		±0.02		LSB
Power-Supply Current	IDD	VIN = VIL or VIH		5.5	7.5	mA
	ISS			5.0	7.5	
	ICC			0.1	1.0	

Note 1: Includes: Full-Scale Error, Offset Error, Relative Accuracy.

Note 2: Guaranteed by design.

Note 3: Auto-zero cycle time included in Conversion Time.

Note 4: Power-supply current is measured when MX7582 is inactive (CS = WR = RD = BUSY = High).

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TIMING CHARACTERISTICS (Note 5, Figures 1 and 2)

(V_{DD} = +15V, V_{CC} = +5V, V_{SS} = -5V, REFIN = +5.0V.)

PARAMETER	SYMBOL	CONDITIONS	T _A = +25°C			T _A = -40°C to +85°C			T _A = -55°C to +125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
CS to WR Setup Time	t ₁		0			0			0			ns
WR Pulse Width	t ₂ (INT)	Internal Clock Operation	200			240			280			ns
WR Pulse Width	t ₂ (EXT)	External Clock Operation	10			10			10			μs
CS to WR Hold Time	t ₃		0			0			0			ns
WR to BUSY Propagation Delay	t ₄			80	200		95	250		110	300	ns
A0, A1 Valid to WR Setup Time	t ₅		0			0			0			ns
A0, A1 Valid to WR Hold Time	t ₆		20			20			20			ns
BUSY to CS Setup Time	t ₇	(Note 2)	0			0			0			ns
CS to RD Setup Time	t ₈		0			0			0			ns
RD Pulse Width	t ₉		200			240			280			ns
CS to RD Hold Time	t ₁₀		0			0			0			ns
BYSL to RD Setup Time	t ₁₁		50			50			50			ns
BYSL to RD Hold Time	t ₁₂		0			0			0			ns
RD to Valid Data (Note 6)	t ₁₃	(Bus Access Time)		60	200		75	240		85	280	ns
RD to Three-State Output (Note 7)	t ₁₄	(Bus Relinquish Time)	20		130	20		160	20		180	ns

Note 5: Data is timed from V_{OH}, V_{OL}; all input control signals are timed from a voltage level of +1.6V and specified with t_r = t_f = 20ns (10% to 90% of +5V).

Note 6: t₁₃, the time required for an output to cross 0.8V or 2.4V, is measured with the load circuits of Figure 3.

Note 7: t₁₄, the time required for the data lines to change 0.5V, is measured with the load circuits of Figure 4.

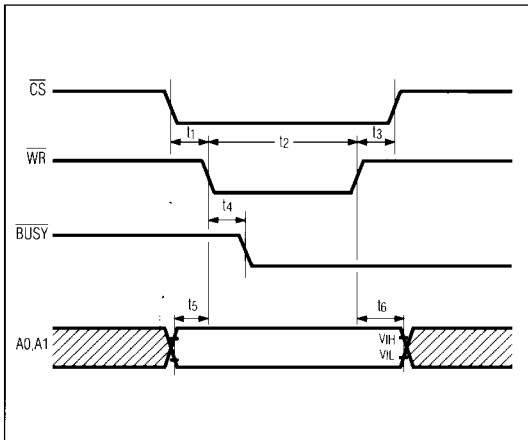


Figure 1. Start Cycle Timing

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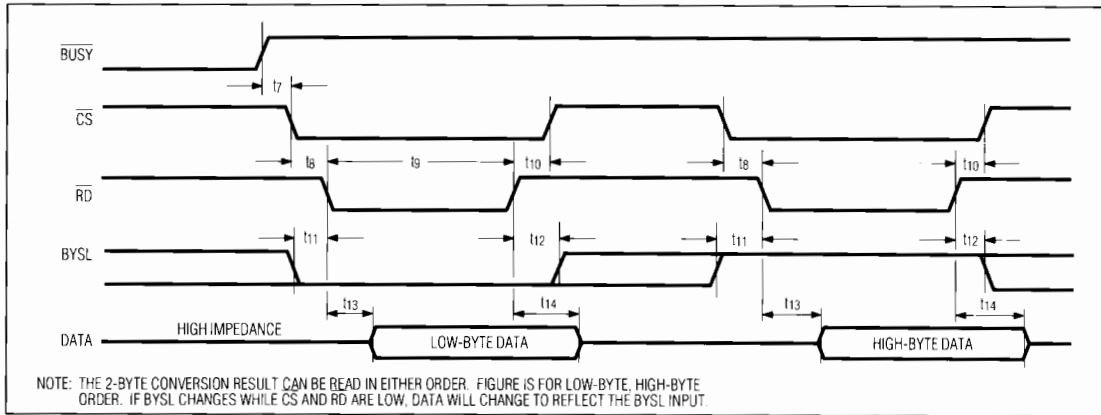


Figure 2. Read Cycle Timing

Pin Description

PIN	NAME	FUNCTION
1	CAZ	Auto-Zero Capacitor Input. Connect other end of capacitor to AGND.
2	AIN0	Analog Input for Channel 0
3	AIN1	Analog Input for Channel 1
4	AIN2	Analog Input for Channel 2
5	AIN3	Analog Input for Channel 3
6	REFIN	Voltage Reference Input. The MX7582 is specified with REF _{IN} = +5.0V.
7	AGND	Analog Ground
8	DGND	Digital Ground
9	VCC	Logic Supply. Digital inputs and outputs are TTL compatible for V _{CC} = +5V.
10-17	DB0-DB7	Three-State Data Outputs. Active when CS and RD are brought low. Individual pin functions depend upon BYTE SELECT (BYSL) input.

PIN	NAME	FUNCTION															
18	RD	READ Input. Used with CS to enable the three-state data outputs. RD is active low.															
19	CS	CHIP SELECT Input. Used with either RD or WR for control. CS is active low and is usually the decoded device address enable signal.															
20	WR	WRITE Input. In combination with CS, this active low signal starts a new conversion. The minimum WR pulse width is t ₂ (INT) when the MX7582 is driven by the on-chip clock. When an external clock is used, the minimum WR pulse width, t ₂ (EXT), must include the auto-zero cycle time.															
21	BYSL	BYTE SELECT. Use BYSL to select high- or low-byte output during a data READ operation. (RD, CS = low). See Data Bus Output Section.															
22	BUSY	Converter Status. BUSY is only low during conversion.															
23	CLK	CLOCK Input. Internal clock operation, with clock circuit shown in Figure 6, typically results in 120μs conversion time. This can be shortened by using an external 74HC clock source (Figure 8).															
24	A0	Address Input A0. See A1 description.															
25	A1	Address Input A1. Address Inputs A0 and A1 select the input channel. The address inputs are latched when WR returns high. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>A1</th> <th>A0</th> <th>Channel Selected</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>AIN0</td> </tr> <tr> <td>0</td> <td>1</td> <td>AIN1</td> </tr> <tr> <td>1</td> <td>0</td> <td>AIN2</td> </tr> <tr> <td>1</td> <td>1</td> <td>AIN3</td> </tr> </tbody> </table>	A1	A0	Channel Selected	0	0	AIN0	0	1	AIN1	1	0	AIN2	1	1	AIN3
A1	A0	Channel Selected															
0	0	AIN0															
0	1	AIN1															
1	0	AIN2															
1	1	AIN3															
26	N.C.	No Connection. leave pin unconnected.															
27	VSS	Negative Supply Voltage, -5V															
28	VDD	Positive Supply Voltage, +15V															

DATA BUS OUTPUT, CS, RD = LOW		
PIN	BYSL = HIGH	BYSL = LOW
10	BUSY (Note 8)	DB7
11	LOW (Note 9)	DB6
12	LOW (Note 9)	DB5
13	LOW (Note 9)	DB4
14	DB11 (MSB)	DB3
15	DB10	DB2
16	DB9	DB1
17	DB8	DB0 (LSB)

Note 8: High during a conversion, BUSY is a converter status flag.
Note 9: When BYSL is high, pins 11-13 output a logic low. The 12-bit digital result is in DB11-DB0. DB11 is the MSB.

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Detailed Operation Operating Information

Figure 5 shows an operational diagram for the MX7582. The only required passive components are a hold capacitor (CAZ) and timing components (RCLK, CCLK1, CCLK2) for the on-chip clock oscillator. Only CAZ is required when the MX7582 is used with an external clock. Individual pin functions are listed in the Pin Description table.

On-Chip Clock Operation

Figure 6 shows the clock circuitry for on-chip clock operation. Operating waveforms are shown in Figure 7.

The MX7582 is in the auto-zero mode when a conversion is complete (BUSY = High). When a new conversion is initiated (CS = Low, WR = Low), CAZ charges to a level equal to the analog input voltage minus the input offset voltage of the auto-zero comparator. The auto-zero cycle must extend at least 10µs into the new conversion.

When using an internal clock, it is not necessary for \overline{WR} to remain low for 10µs since auto-zero timing is automatically set by the MX7582. This is achieved by switching a constant current load across the clock capacitors, CCLK1 and CCLK2, causing the voltage at the CLK input pin to slowly decay from VCC (Figure 7). This occurs after \overline{WR} returns high. The Schmitt trigger circuit monitoring

the voltage on the CLK input ends the auto-zero cycle when its low-input trigger level is reached. At this point, the constant current load across the clock capacitors is removed allowing them to charge towards VCC via RCLK. When the voltage at the CLK input reaches the high-trigger level, the constant current load is replaced across CCLK1 and CCLK2. The most significant bit (MSB) decision is made when the low-trigger level is reached. This cycle repeats itself 12 times to provide 12 clock pulses for a complete conversion. The circuit arrangement of Figure 6 provides the relatively slow auto-zero cycle time at the beginning of a conversion while allowing the clock oscillator to speed up once the auto-zero cycle is complete.

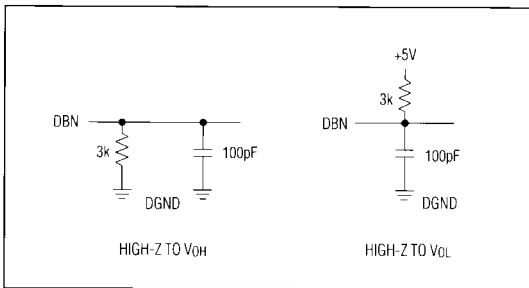


Figure 3. Load Circuits for Access Time Test (t_{13})

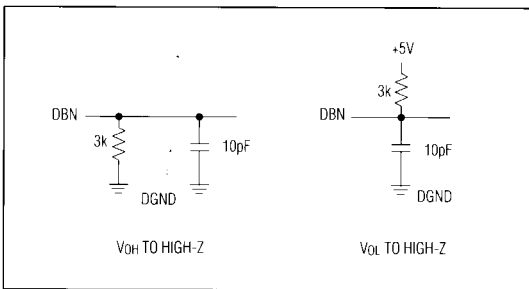


Figure 4. Load Circuits for Output Float Delay Test (t_{14})

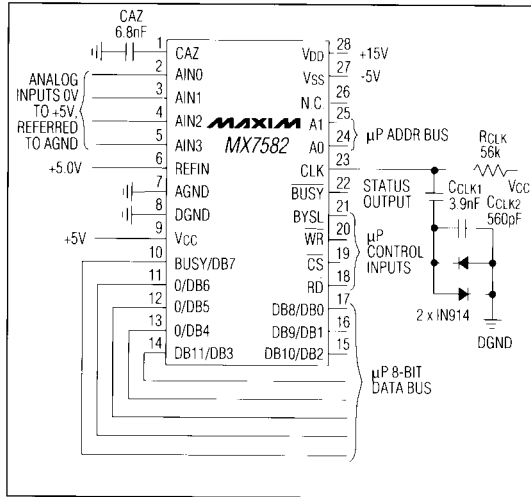


Figure 5. MX7582 Operational Diagram

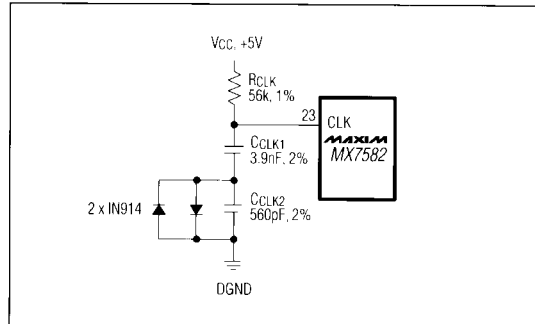


Figure 6. Circuitry Required for Internal Clock Operation

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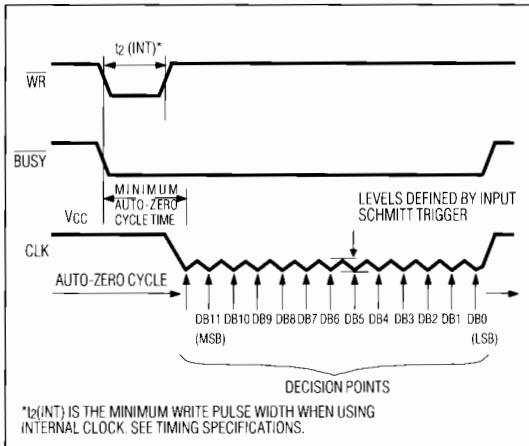


Figure 7. Operating Waveform - Internal Clock

External Clock Operation

For external clock operation, the CLK input is driven with a 74HC compatible clock source (Figure 8). RCLK, CCLK1 and CCLK2 are no longer required. To provide the minimum auto-zero cycle time of 10µs, the WR pulse width must be extended to the minimum WR pulse width, $t_2(EXT)$, since this is not provided automatically when using an external clock (Figure 9). It is essential that the CS input and the multiplexer address inputs (A0, A1) remain valid throughout the extended WR pulse width.

Since the MSB decision is made during the second falling edge of the clock input after WR returns high, the external clock source need not be synchronized with the extended WR pulse width.

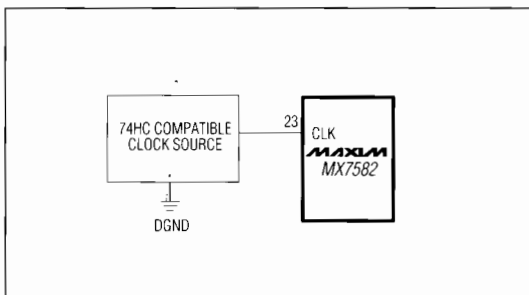


Figure 8. External Clock Operation

Reading Data

The 12-bit conversion result and the converter status flag are accessible over an 8-bit data bus. Data is available from the MX7582 with the least significant bit (LSB) right-justified. Two read operations are needed. The Byte Select (BYSL) input determines which byte is to be read first, 8 LSBs or 4 MSBs plus status flag.

It is necessary to wait for the end of a conversion to obtain valid 12-bit data from the MX7582's successive approximation register (SAR). If a read operation is performed during a conversion, the MX7582 will dump the existing contents of the SAR onto the data bus. There are three different methods to ensure correct operation:

1. Insert a software delay longer than the ADC conversion time between the conversion start and the data read operations.
2. BUSY is low during conversion and high at conversion end. Use this signal as an interrupt to the microprocessor.
3. Poll the converter status flag, BUSY, at user-defined intervals after a conversion start. The status flag is available on the DB7 pin during a high-byte READ. The flag is the left-most bit and can be shifted directly into the microprocessor's carry flag for testing. BUSY is high during a conversion.

A write operation to the MX7582 during a conversion will restart the conversion.

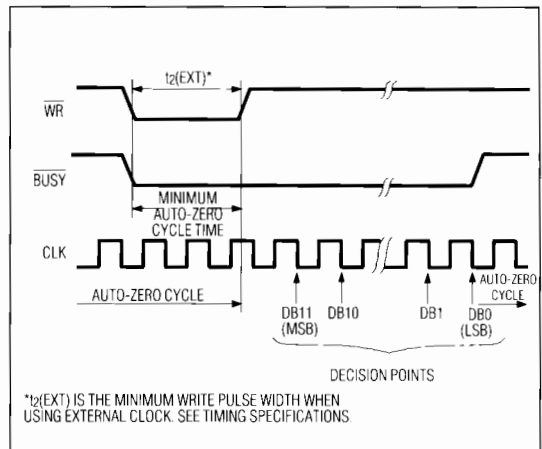


Figure 9. Operating Waveform - External Clock

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Application Hints

Auto-zero Capacitor (CAZ)

The auto-zero capacitor (CAZ) must be a low-leakage, low-dielectric absorption type such as polypropylene, polystyrene, or teflon. Connect the outside foil of CAZ to AGND to minimize noise. CAZ should be between 2.2nF to 6.8nF.

Clock

Series connected capacitors, CCLK1 and CCLK2, generate clock cycles by charging through an external resistor, RCLK, and discharging internally through a switch. Figure 10 shows typical conversion time vs. temperature when using the MX7582's on-chip clock. Due to variations in manufacturing, the actual operating frequency can differ from chip-to-chip by up to 20%. For this reason, it is suggested that an external clock be used under the following situations:

1. Applications needing a conversion time within 20% of 100 μ s, the shortest conversion time allowable for specified accuracy.
2. Applications that cannot accept conversion time variations, which may result from internal clock variations.

The internal clock may be adjusted by exchanging the RCLK resistor with a 50k Ω potentiometer in series with a 22k Ω resistor (Figure 6). Reducing the value of RCLK from 56k Ω to 47k Ω decreases the conversion time by approximately 15 μ s at room temperature.

Analog Inputs

The high-impedance analog inputs, AIN0-AIN3, allow simple analog interfacing. Signal sources from 0V to +5V may be connected directly to AIN without extra buffering for source impedances up to 5k Ω (Figure 11). The

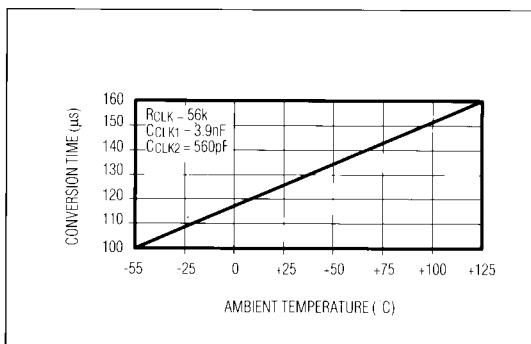


Figure 10. Typical Conversion Time vs. Temperature Using Internal Clock

input/output transfer characteristic and transition points for this input signal range are demonstrated in Figure 12 and Table 1. The MX7582 transfer characteristic transition points occur on integer multiples of 1LSB. The output code is natural binary, with: 1LSB = (Full Scale (FS)) / 4096 = (5/4096)V = 1.22mV.

For signal ranges other than 0V to +5V, use resistor divider networks to provide 0V to +5V signal ranges at the MX7582 input pins. The connection in Figure 13 shows a divider network on channel 0 for a 0V to +10V signal range. Resistors should be of the same type and manufacturer to ensure matched temperature coefficients. The source impedance must now be as low as possible since it adds to the resistor divider impedance. The full-scale error created by source impedance R_S is: $R_S / (R_1 + R_2 + R_S)$.

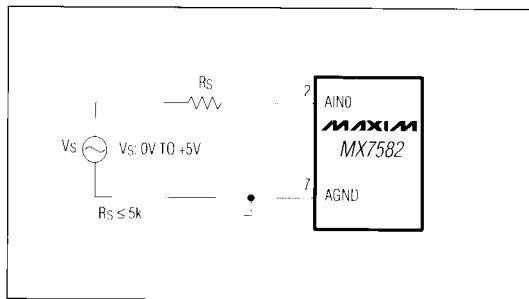


Figure 11. Unipolar 0V to +5V Operation

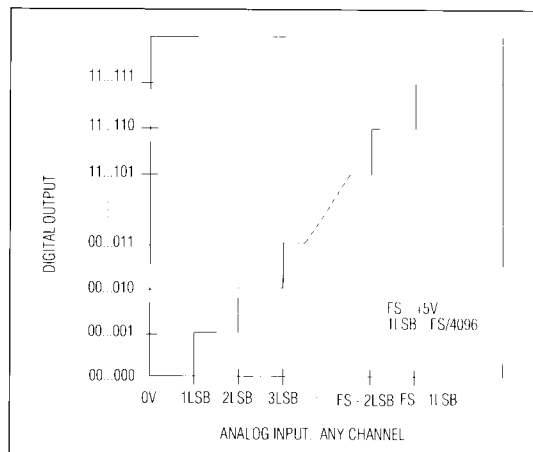


Figure 12. Ideal Input/Output Transfer Characteristic for Unipolar Circuit of Figure 11

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Figure 14 shows how bipolar signals (-5V to +5V) on channel 0 are accommodated by referencing a resistor divider network to REFIN. The signal source must be capable of sinking 0.5mA with the resistor values shown. Refer to Figure 15 and Table 2 for the input/output transfer characteristic and transition points for the ±5V signal range, respectively. The output code is offset binary with an LSB size of: $(FS)/(1/4096) = (10/4096)V = 2.44mV$.

To adjust bipolar zero error, apply 1.22mV (+1/2LSB) to AIN and adjust the offset of A1 so that the ADC output switches between 1000 0000 0000 and 1000 0000 0001.

Power-Supply Decoupling

Power supplies to the MX7582 should be bypassed with a 10µF electrolytic or tantalum capacitor in parallel with a 0.01µF disc ceramic capacitor for clean, high-frequency performance. Place all capacitors as close as possible to the MX7582.

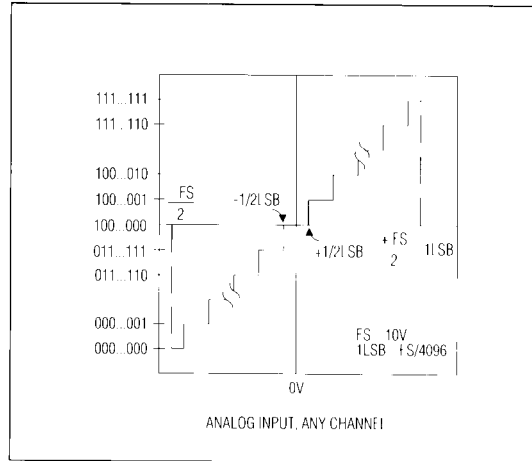


Figure 15. Ideal Input/Output Transfer Characteristic for Bipolar Circuit of Figure 14

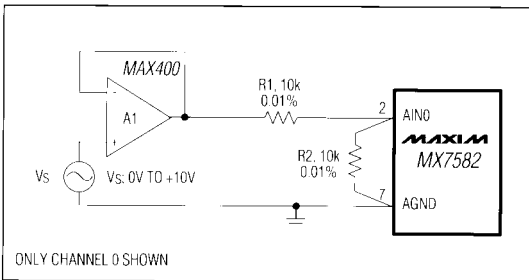


Figure 13. Unipolar 0V to +10V Operation

Table 1. Transition Points for Unipolar 0V to +5V Operation

Analog Input (V)	Digital Output
0.00122	0000 0000 0001
0.00244	0000 0000 0010
...	...
2.49878	0111 1111 1111
2.50000	1001 1111 1000
2.50122	1001 1111 1001
...	...
4.99756	1111 1111 1110
4.99878	1111 1111 1111

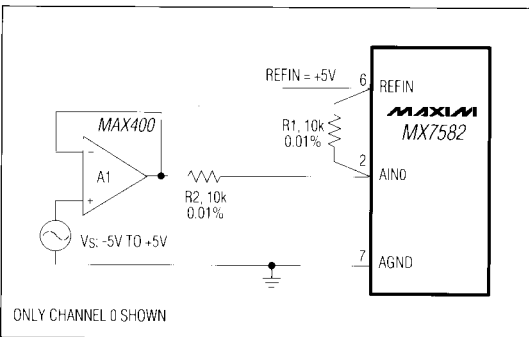


Figure 14. Bipolar -5V to +5V Operation

Table 2. Transition Points for Bipolar -5V to +5V Operation

Analog Input (V)	Digital Output
-4.99878	0000 0000 0001
-4.99634	0000 0000 0010
...	...
-0.00122	1000 0000 0000
+0.00122	1000 0000 0001
...	...
+4.99389	1111 1111 1110
+4.99634	1111 1111 1111

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Reference Circuit

Figure 16 shows how to set up a Maxim MX584LH to generate a reference voltage of +5.00V. An adjustment range of $\pm 75\text{mV}$ is provided by R2. Over the commercial temperature range, the MX584LH will contribute no more than $\pm 1\text{LSB}$ of gain error.

During a conversion, transient currents flow at the REFIN input. To prevent dynamic errors, place either a $10\mu\text{F}$ electrolytic or tantalum smoothing capacitor in parallel with a $0.01\mu\text{F}$ disc ceramic from the REFIN pin to AGND.

Layout

When designing a layout for a printed circuit board, keep digital and analog signal lines separated whenever possible. It is critical that no digital line run alongside an analog signal line or near the CAZ. Guard the analog inputs, the reference input and the auto-zero input with traces connected to AGND.

Establish a single-point analog ground (AGND) as close to the MX7582 as possible, isolated from the logic system. Connect the single-point analog ground to the digital system ground, which is attached to DGND at one point and as close as possible to the MX7582. The following should be returned to the analog ground point:

input-signal common, input guards, CAZ, and any bypass capacitors for the reference input and the analog supplies. Low-impedance analog and digital power-supply common returns with wide trace widths are essential for quiet operation of the MX7582.

Noise

To minimize the input noise coupling, input signal leads to AIN and signal return leads from AGND should be kept as short as possible. A shielded cable between source and ADC is suggested in applications where longer leads are required. Also, care should be taken to reduce the ground-circuit impedances as much as possible since any potential difference in grounds between the signal source and ADC creates an error voltage in series with the input signal.

When interfacing to continuously busy and noisy microprocessor buses, it is possible to get errors at the LSB level. These errors exist because of feedthrough from the bus to the integrated circuit through the package. The problem can be minimized in ceramic side braze (Ceramic SB) packaged chips by grounding the metal lid. Another solution is to isolate the MX7582 from the microprocessor bus with three-state buffers.

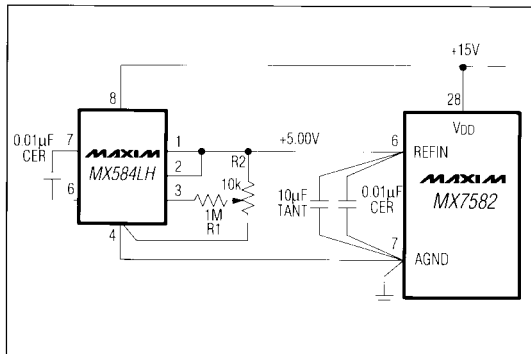
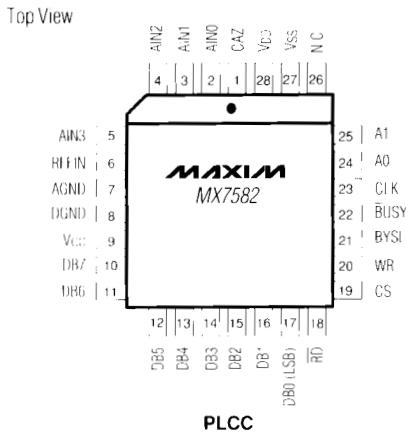


Figure 16. MX584LH as Reference Generator

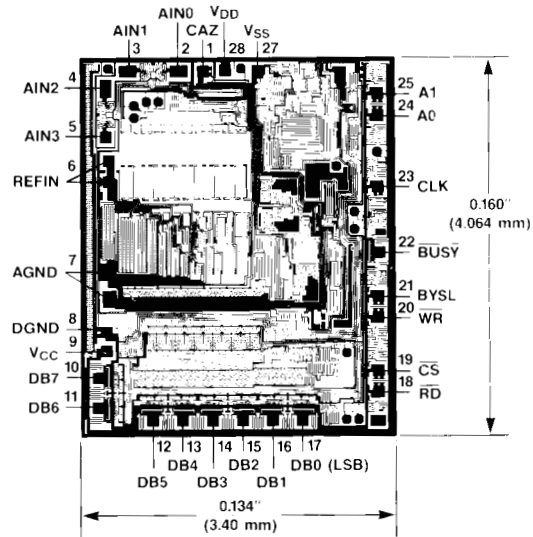
Calibrated 4-Channel 12-Bit ADC

MX7582

Pin Configurations (continued)



Chip Topography



Package Information

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	-	0.200	-	5.08
A1	0.015	-	0.38	-
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.020	0.41	0.51
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.050	0.090	1.27	2.29
E	0.600	0.625	15.24	15.88
E1	0.525	0.575	13.34	14.61
e	0.100	-	2.54	-
eA	0.600	-	15.24	-
eB	-	0.700	-	17.78
L	0.120	0.150	3.05	3.81

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	24	1.230	1.270	31.24	32.26
P	D	28	1.430	1.470	36.32	37.34
P	D	40	2.025	2.075	51.44	52.71

Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.600 in.)

MX7582

Calibrated 4-Channel 12-Bit ADC

Package Information (continued)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
E	0.291	0.299	7.40	7.60
e	0.050		1.27	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.398	0.413	10.10	10.50
D	18	0.447	0.463	11.35	11.75
D	20	0.496	0.512	12.60	13.00
D	24	0.598	0.614	15.20	15.60
D	28	0.697	0.713	17.70	18.10

21-0042A

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.145	0.156	3.68	3.96
A3	0.020	—	0.51	—
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
e	0.050		1.27	

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	20	0.385	0.395	9.78	10.03
D1		0.350	0.356	8.89	9.04
D2		0.290	0.330	7.37	8.38
D3	28	0.200	REF	5.08	REF
D		0.485	0.495	12.32	12.57
D1		0.450	0.456	11.43	11.58
D2		0.390	0.430	9.91	10.92
D3	44	0.300	REF	7.62	REF
D4		0.300	—	7.62	—
D		0.685	0.695	17.40	17.65
D1		0.650	0.656	16.51	16.66
D2	68	0.590	0.630	14.99	16.00
D3		0.500	REF	12.70	REF
D4		0.470	—	11.94	—
D		0.985	0.995	25.02	25.27
D1	0.950	0.958	24.13	24.33	
D2	0.890	0.930	22.61	23.62	
D3	0.800	REF	20.32	REF	
D4	0.625	—	15.87	—	

21-0049B

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