

**MAXIM****Single LVDS Line Receiver in SC70****General Description**

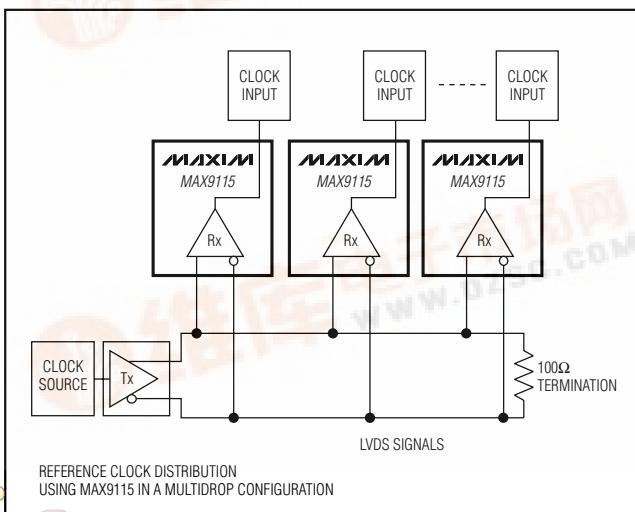
The MAX9115 is a single low-voltage differential signaling (LVDS) line receiver ideal for applications requiring high data rates, low power, and low noise. The device is guaranteed to receive data at speeds up to 200Mbps (100MHz).

The MAX9115 accepts an LVDS differential input and translates it to an LVTTL/LVC MOS output. The fail-safe feature sets the output high when the inputs are undriven and open, terminated, or shorted. The device supports a wide common-mode input range, allowing a ground potential difference and common-mode noise between the driver and the receiver. The MAX9115 conforms to the ANSI TIA/EIA-644 LVDS standard.

The MAX9115 operates from a single +3.3V supply, and is specified for operation from -40°C to +85°C. It is available in a space-saving 5-pin SC70 package. Refer to the MAX9110/MAX9112 data sheet for single/dual LVDS line drivers.

**Applications**

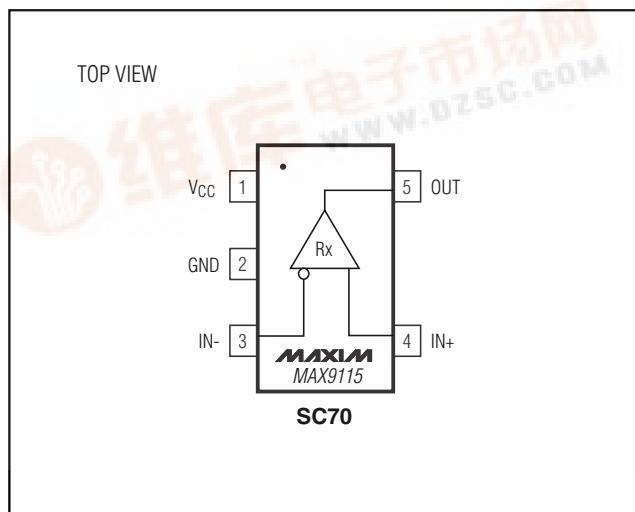
Clock Distribution  
Cellular Phone Base Stations  
Digital Cross-Connects  
Network Switches/Routers  
DSLAMs  
Laser Printers

**Typical Application Circuit****Features**

- ◆ Space-Saving SC70 Package (50% Smaller than SOT23)
- ◆ Guaranteed 200Mbps Data Rate
- ◆ Low 350ps (max) Pulse Skew
- ◆ High-Impedance LVDS Inputs When Powered Off Allow Hot Swapping
- ◆ Conforms to ANSI TIA/EIA-644 LVDS Standard
- ◆ Single +3.3V Supply
- ◆ Fail-Safe Circuit Sets Output High for Undriven Inputs (Open, Terminated, or Shorted)
- ◆ Low 150µA (typ) Supply Current in Fail-Safe Mode

**MAX9115****Ordering Information**

PART	TEMP. RANGE	PIN-PACKAGE	TOP MARK
MAX9115EXK-T	-40°C to +85°C	5 SC70-5	ACI

**Pin Configuration**

# Single LVDS Line Receiver in SC70

## ABSOLUTE MAXIMUM RATINGS

V <sub>CC</sub> to GND	-0.3V to +4.0V
IN+, IN- to GND	-0.3V to +4.0V
OUT to GND	-0.3V to (V <sub>CC</sub> + 0.3V)
Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
5-Pin SC70 (derate 3.1mW/°C above +70°C)	247 mW
Output Short to GND (OUT) (Note 1)	1s
Storage Temperature Range	-65°C to +150°C

Maximum Junction Temperature	+150°C
Operating Temperature Range	-40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
ESD Protection	

    Human Body Model (IN+, IN-) ±6kV

**Note 1:** Package leads soldered to a PC board having copper ground and V<sub>CC</sub> planes. Do not exceed Maximum Junction Temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +3.0V to +3.6V, differential input voltage |V<sub>ID</sub>| = 0.05V to 1.0V, input common voltage V<sub>CM</sub> = |V<sub>ID</sub>|/2 to 2.4V - |V<sub>ID</sub>|/2, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values at V<sub>CC</sub> = +3.3V, T<sub>A</sub> = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
<b>LVDS INPUTS (IN+, IN-)</b>							
Differential Input High Threshold	V <sub>TH</sub>				50		mV
Differential Input Low Threshold	V <sub>TL</sub>			-50			mV
Input Current	I <sub>IN+</sub> , I <sub>IN-</sub>	0.05V ≤  V <sub>ID</sub>   ≤ 0.6V		-20	20		μA
		0.6V <  V <sub>ID</sub>   ≤ 1.0V		-25	25		
Power-Off Input Current	I <sub>INO</sub>	0.05V ≤  V <sub>ID</sub>   ≤ 0.6V, V <sub>CC</sub> = 0		-20	20		μA
		0.6V <  V <sub>ID</sub>   ≤ 1.0V, V <sub>CC</sub> = 0		-25	25		
Input Resistance	R <sub>IN1</sub>	V <sub>CC</sub> = +3.6V or 0, Figure 1		35			kΩ
	R <sub>IN2</sub>	V <sub>CC</sub> = +3.6V or 0, Figure 1		132			
<b>LVTT/LVCMOS OUTPUT (OUT)</b>							
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -8.0mA	Inputs open or undriven short or undriven 100Ω termination	V <sub>CC</sub> - 0.3		V	
			V <sub>ID</sub> = +50mV	V <sub>CC</sub> - 0.3			
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = +8.0mA, V <sub>ID</sub> = -50mV			0.25		V
Output Short-Circuit Current	I <sub>OS</sub>	V <sub>ID</sub> = +50mV, V <sub>OUT</sub> = 0			-125		mA
<b>SUPPLY CURRENT</b>							
Supply Current	I <sub>CC</sub>	No load, inputs undriven (fail-safe)		150	300		μA
		No load, inputs driven			7		mA

# Single LVDS Line Receiver in SC70

## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +3.0V$  to  $+3.6V$ ,  $C_L = 15pF$ , differential input voltage  $|V_{ID}| = 0.15V$  to  $1.0V$ , input common voltage  $V_{CM} = |V_{ID}|/2l$  to  $2.4V - |V_{ID}|/2l$ , input rise and fall time =  $1ns$  (20% to 80%), input frequency =  $100MHz$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values at  $V_{CC} = +3.3V$ ,  $|V_{ID}| = 0.2V$ ,  $V_{CM} = 1.2V$ ,  $T_A = +25^{\circ}C$ .) (Figures 2 and 3) (Notes 4 and 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Propagation Delay High to Low	$t_{PHLD}$		1.2	1.9	3	ns
Differential Propagation Delay Low to High	$t_{PLHD}$		1.2	1.9	3	ns
Differential Pulse Skew $ t_{PHLD} - t_{PLHD} $ (Note 6)	$t_{SKD1}$				350	ps
Differential Part-to-Part Skew (Note 7)	$t_{SKD2}$				1.3	ns
Differential Part-to-Part Skew (Note 8)	$t_{SKD3}$				1.8	ns
Rise-Time	$t_{TLH}$		0.5	0.8		ns
Fall-Time	$t_{THL}$		0.5	0.8		ns
Maximum Operating Frequency (Note 9)	$f_{MAX}$		100			MHz

**Note 2:** Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at  $T_A = +25^{\circ}C$ .

**Note 3:** Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except  $V_{TH}$ ,  $V_{TL}$ , and  $V_{ID}$ .

**Note 4:** AC parameters are guaranteed by design and characterization.

**Note 5:**  $CL$  includes scope probe and test jig capacitance.

**Note 6:**  $t_{SKD1}$  is the magnitude difference of differential propagation delays.  $t_{SKD1} = |t_{PHLD} - t_{PLHD}|$ .

**Note 7:**  $t_{SKD2}$  is the magnitude difference of any differential propagation delays between parts operating over rated conditions at the same  $V_{CC}$  and within  $5^{\circ}C$  of each other.

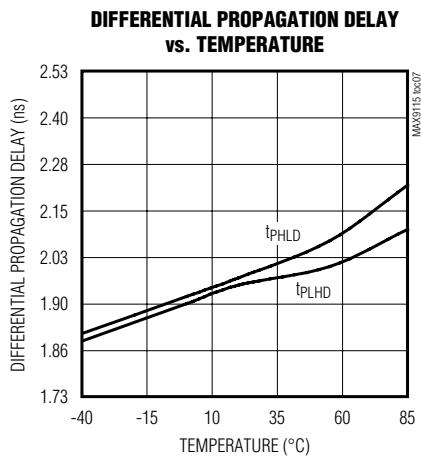
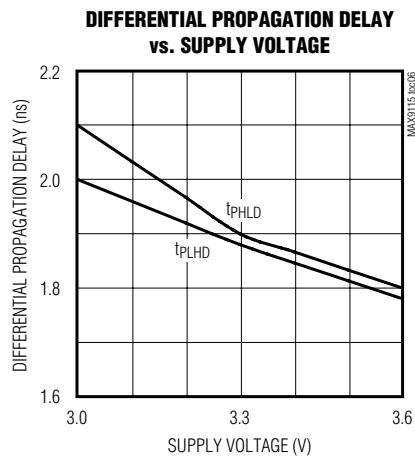
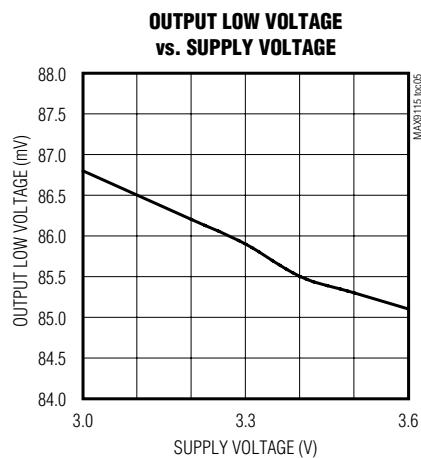
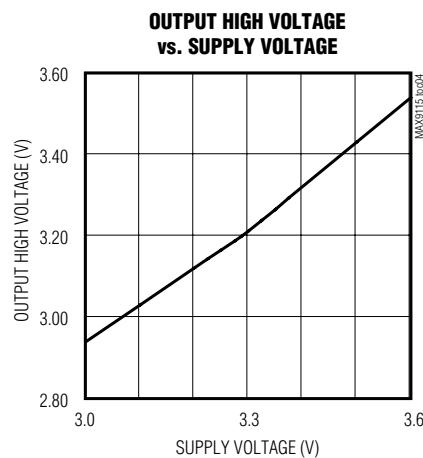
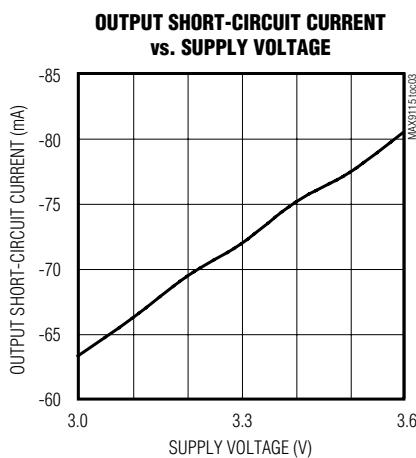
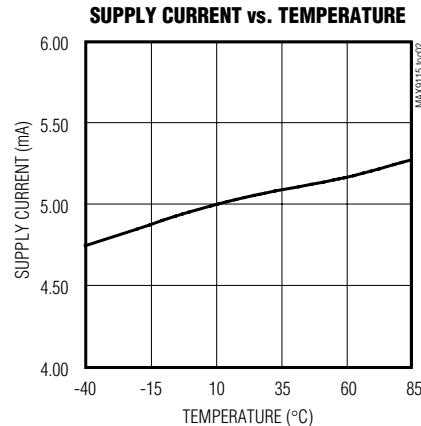
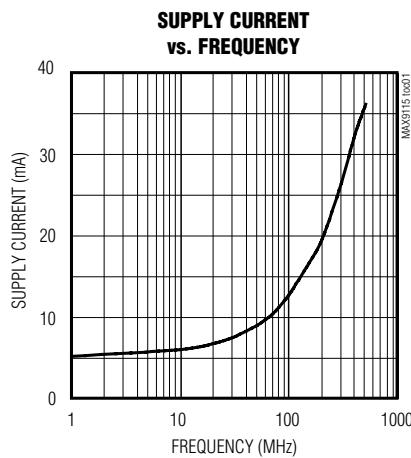
**Note 8:**  $t_{SKD3}$  is the magnitude difference of any differential propagation delays between parts operating over rated conditions.

**Note 9:**  $f_{MAX}$  pulse generator output conditions: rise-time = fall-time =  $1ns$  (0% to 100%), 50% duty cycle,  $V_{OH} = +1.3V$ ,  $V_{OL} = +1.1V$ . MAX9115 output criteria: 60% to 40% duty cycle,  $V_{OL} = 0.25V$  max,  $V_{OH} = 2.7V$  min, load =  $15pF$ .

## Single LVDS Line Receiver in SC70

### Typical Operating Characteristics

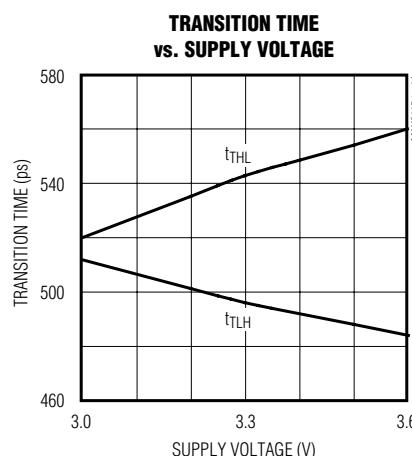
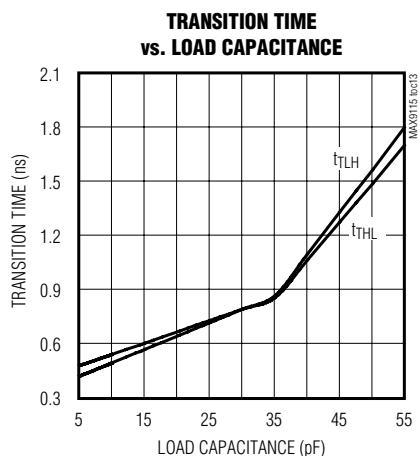
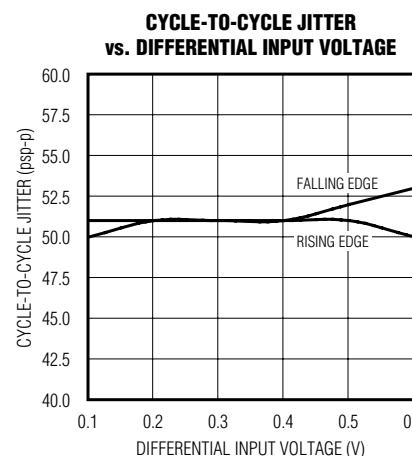
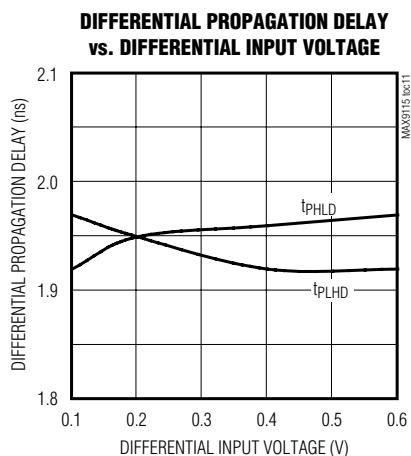
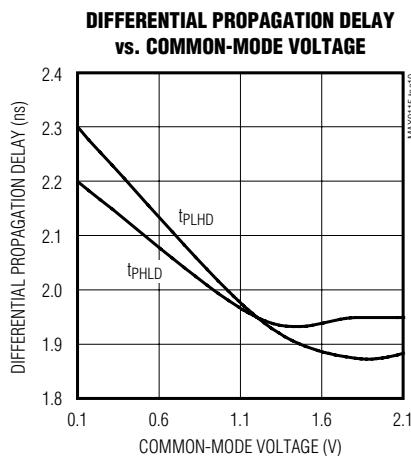
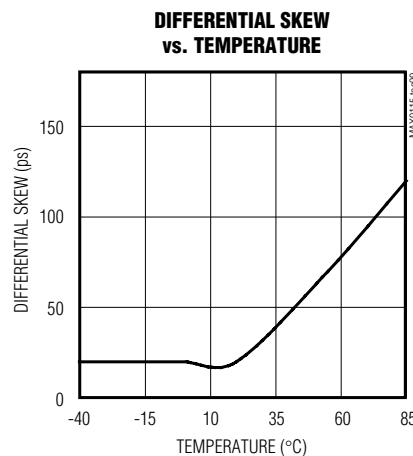
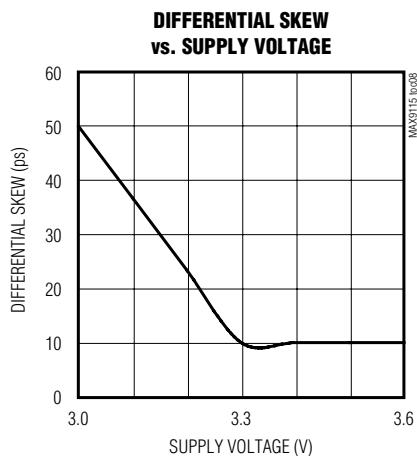
( $V_{CC} = +3.3V$ ,  $C_L = 15pF$ ,  $IV_{DL} = 0.2V$ ,  $V_{CM} = 1.2V$ , input rise and fall time = 1ns (20% to 80%), input frequency = 100MHz, 50% duty cycle,  $T_A = +25^{\circ}C$ , unless otherwise noted.)



# Single LVDS Line Receiver in SC70

## Typical Operating Characteristics (continued)

( $V_{CC} = +3.3V$ ,  $C_L = 15pF$ ,  $IV_{IDL} = 0.2V$ ,  $V_{CM} = 1.2V$ , input rise and fall time = 1ns (20% to 80%), input frequency = 100MHz, 50% duty cycle,  $T_A = +25^\circ C$ , unless otherwise noted.)



# Single LVDS Line Receiver in SC70

## Pin Description

PIN	NAME	FUNCTION
1	Vcc	Power-Supply Input. Bypass Vcc to GND with a $0.01\mu\text{F}$ ceramic capacitor.
2	GND	Ground
3	IN-	Inverting LVDS Differential Input
4	IN+	Noninverting LVDS Differential Input
5	OUT	LVTT/LVC MOS Output

## Detailed Description

LVDS is intended for point-to-point communication over a controlled-impedance medium as defined by the ANSI TIA/EIA-644 and IEEE 1596.3 standards. LVDS uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI emissions and system susceptibility to noise.

The MAX9115 is a single LVDS line receiver ideal for applications requiring high data rates, low power, and low noise. The device accepts an LVDS input and translates it to an LVTT/LVC MOS output. The receiver detects differential signals as low as 50mV and as high as 1V within an input voltage range of 0 to +2.4V.

The 250mV to 450mV differential output of an LVDS driver is nominally centered around a +1.25V offset. This offset, coupled with the receiver's 0 to +2.4V input voltage range, allows an approximate  $\pm 1\text{V}$  shift in the signal (as seen by the receiver). This allows for a difference in ground references of the driver and the receiver, the common-mode effects of coupled noise, or both. The LVDS standards specify an input voltage range of 0 to +2.4V referenced to receiver ground.

### Fail-Safe

The fail-safe feature of the MAX9115 sets the output high and reduces supply current when:

- inputs are open
- inputs are undriven and shorted
- inputs are undriven and terminated

A fail-safe circuit is important because under these conditions, noise at the input may switch the receiver and it may appear to the system that data is being received. Open or undriven terminated input conditions can occur when a cable is disconnected or cut, or when an LVDS driver output is in high impedance. A short condition can occur because of a cable failure.

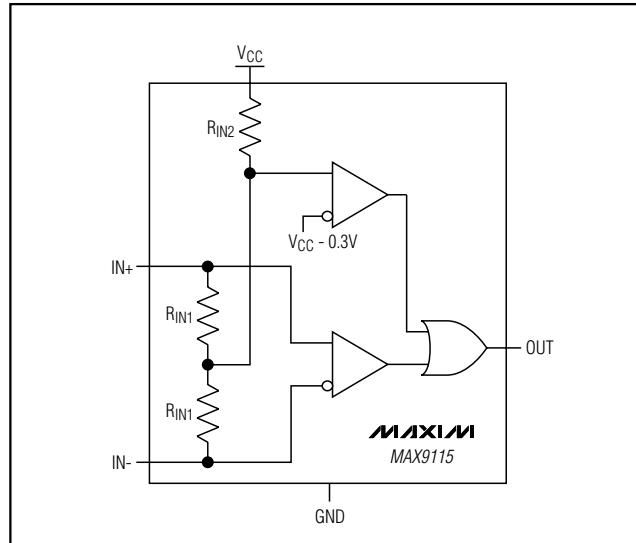


Figure 1. Input Fail-Safe Network

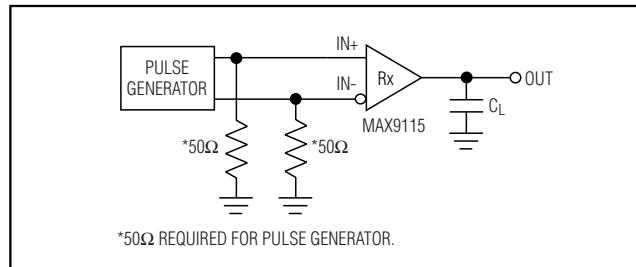


Figure 2. Propagation Delay and Transition Time Test Circuit

The fail-safe input network (Figure 1) samples the input common-mode voltage and compares it to  $\text{VCC} - 0.3\text{V}$  (nominal). When the input is driven to levels specified in the LVDS standards, the input common-mode voltage is less than  $\text{VCC} - 0.3\text{V}$  and the fail-safe circuit is not activated. If the inputs are open or if the inputs are undriven and shorted or undriven and parallel terminated, there is no input current. In this case, a pullup resistor in the fail-safe circuit pulls both inputs above  $\text{VCC} - 0.3\text{V}$ , activating the fail-safe circuit and forcing the output high.

## Applications Information

### Power-Supply Bypassing

Bypass  $\text{VCC}$  with a high-frequency surface-mount ceramic  $0.01\mu\text{F}$  capacitor in parallel as close to the device as possible.

# Single LVDS Line Receiver in SC70

## Differential Traces

Input trace characteristics affect the performance of the MAX9115. Use controlled-impedance PC board traces, typically  $100\Omega$ . Match the termination resistor to this characteristic impedance.

Eliminate reflections and ensure that noise couples as common mode by running the differential traces close together. Reduce skew by matching the electrical length of the traces. Excessive skew can result in a degradation of magnetic field cancellation.

Input differential signals should be routed close to each other to cancel their external magnetic field. Maintain a constant distance between the differential traces to avoid discontinuities in differential impedance. Minimize the number of vias to further prevent impedance discontinuities.

## Cables and Connectors

Transmission media should typically have a controlled differential impedance of  $100\Omega$ . Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Avoid the use of unbalanced cables such as ribbon or simple coaxial cable. Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to canceling effects. Balanced cables tend to pick up noise as common mode, which is rejected by the LVDS receiver.

## Termination

The MAX9115 requires an external termination resistor. The termination resistor should match the differential impedance of the transmission line. Termination resistance is typically  $100\Omega$  but may range between  $90\Omega$  to  $132\Omega$ , depending on the characteristic impedance of the transmission medium.

When using the MAX9115, minimize the distance between the input termination resistor and the MAX9115 receiver inputs. Use 1% surface-mount resistors.

## Board Layout

For LVDS applications, a four-layer PC board that provides separate layers, power, ground, and input/output signals is recommended. Keep the LVDS input signals away from the output LVCMS/LVTTL signal to prevent coupling (Figure 4). To minimize crosstalk, do not run the output in parallel with the inputs. Extend the ground pin trace under the package to the other side between IN+ and OUT to provide isolation between IN+ and OUT.

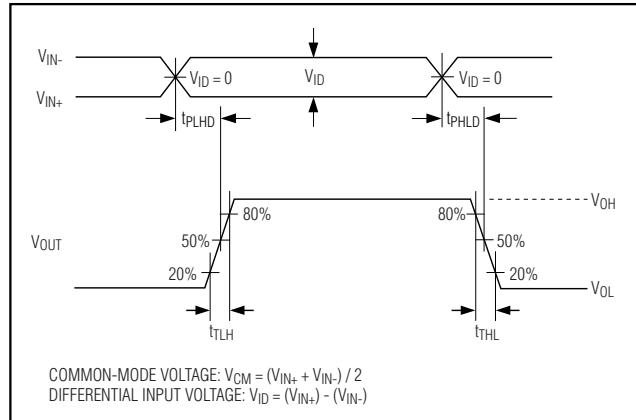


Figure 3. Propagation Delay and Transition-Time Waveforms

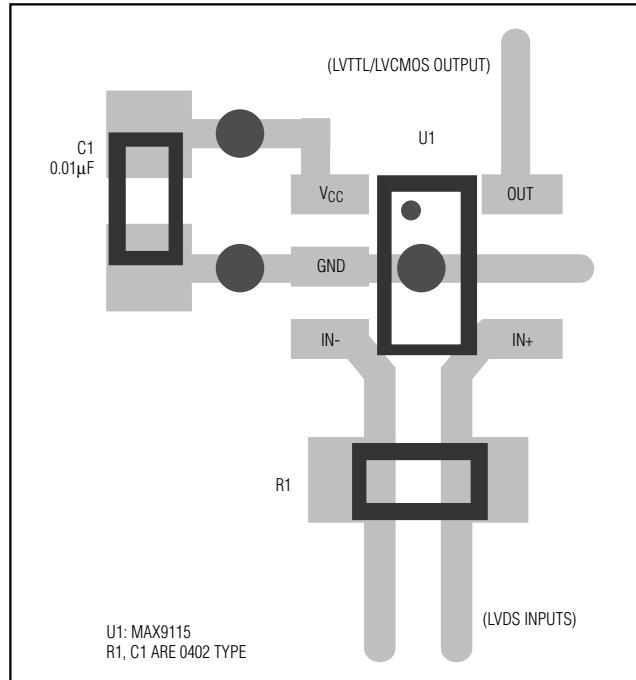


Figure 4. Board Layout

## Chip Information

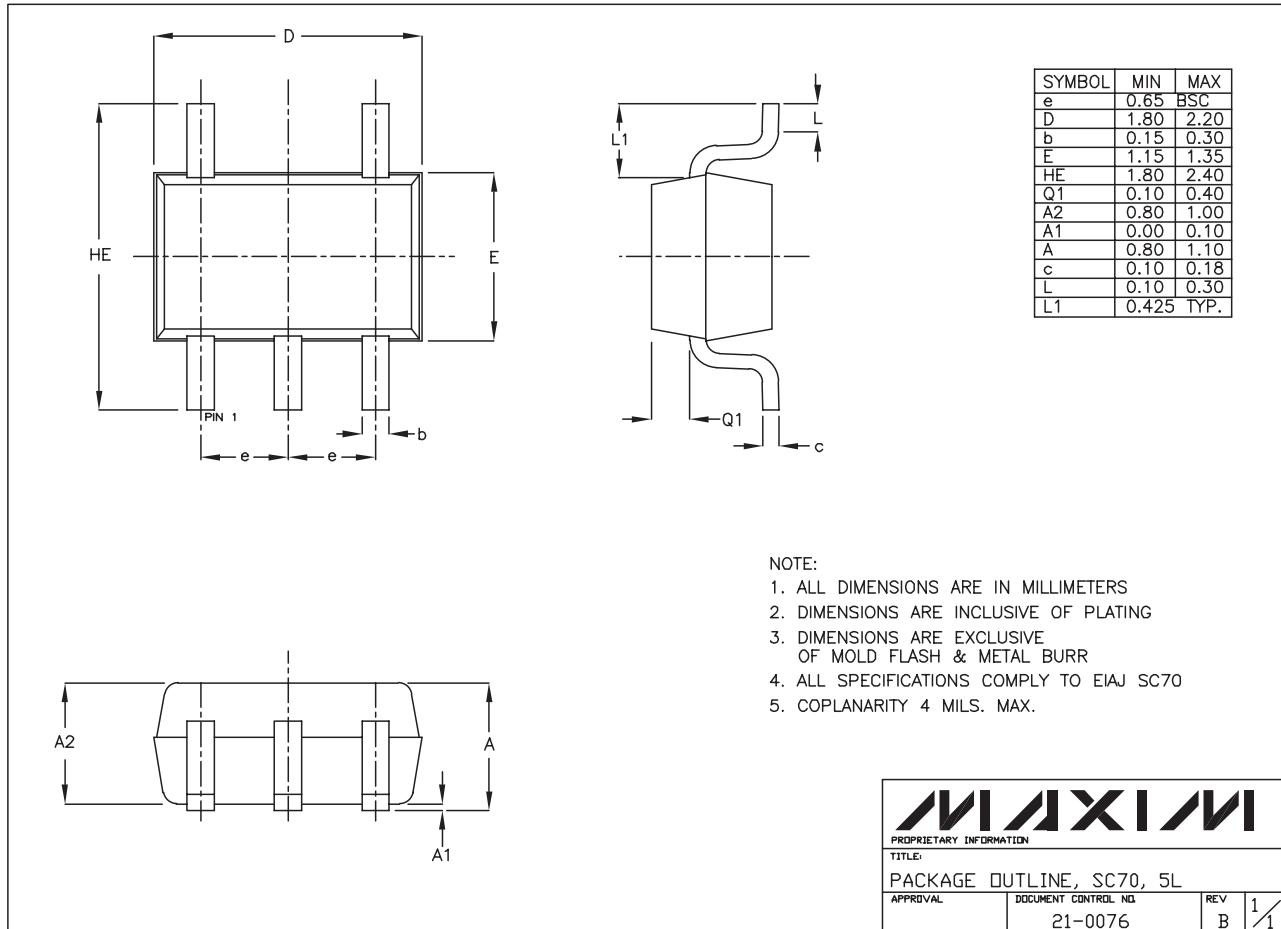
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PROCESS: CMOS

# Single LVDS Line Receiver in SC70

## Package Information

SC70\_5L.EPS



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