August 2005

ASM3P1819N

rev 0.2

Low Power Mobile VGA EMI Reduction IC

Features

- FCC approved method of EMI attenuation
- Provides up to 15dB EMI reduction
- Generates a low EMI spread spectrum clock and a non-spread Reference Clock of the input frequency
- Optimized for frequency range from 20MHz to 40MHz
- Internal loop filter minimizes external components and board space
- Down Spread Deviation: -1.25%
- Low inherent Cycle-to-Cycle jitter
- 3.3V Operating Voltage
- CMOS/TTL compatible inputs and outputs
- Low power CMOS design
- Supports notebook VGA and other LCD timing controller applications
- Power Down function for mobile application
- Products are available for industrial temperature range.
- Available in 8 pin SOIC and TSSOP Packages

Functional Description

The ASM3P1819N is a versatile spread spectrum frequency modulator designed specifically for a wide range of input clock frequencies from 20 to 40MHz. The ASM3P1819N can generate an EMI reduced clock from crystal, ceramic resonator, or system clock.

The ASM3P1819N reduces electromagnetic interference (EMI) at the clock source, allowing a system wide EMI reduction for all the down stream clocks and data dependent signals. The ASM3P1819N allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding, and other passive components that are traditionally required to pass EMI regulations.

The ASM3P1819N modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock, thereby decreasing the peak amplitude of its harmonics. This result in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most clock generators.

Lowering EMI by increasing a signal's bandwidth is called "spread spectrum clock generation". The ASM3P1819N uses the most efficient and optimized modulation profile approved by the FCC and is implemented by using a proprietary all digital method

Applications

The ASM3P1819N is targeted towards EMI management for memory and LVDS interfaces in mobile graphic chipsets and high-speed digital applications such as PC peripheral devices, consumer electronics and embedded controller system.
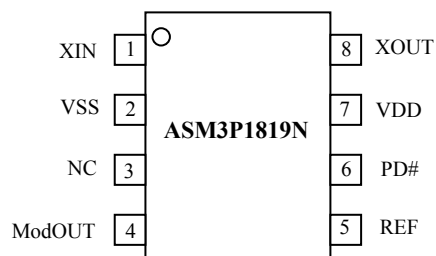
Block Diagram
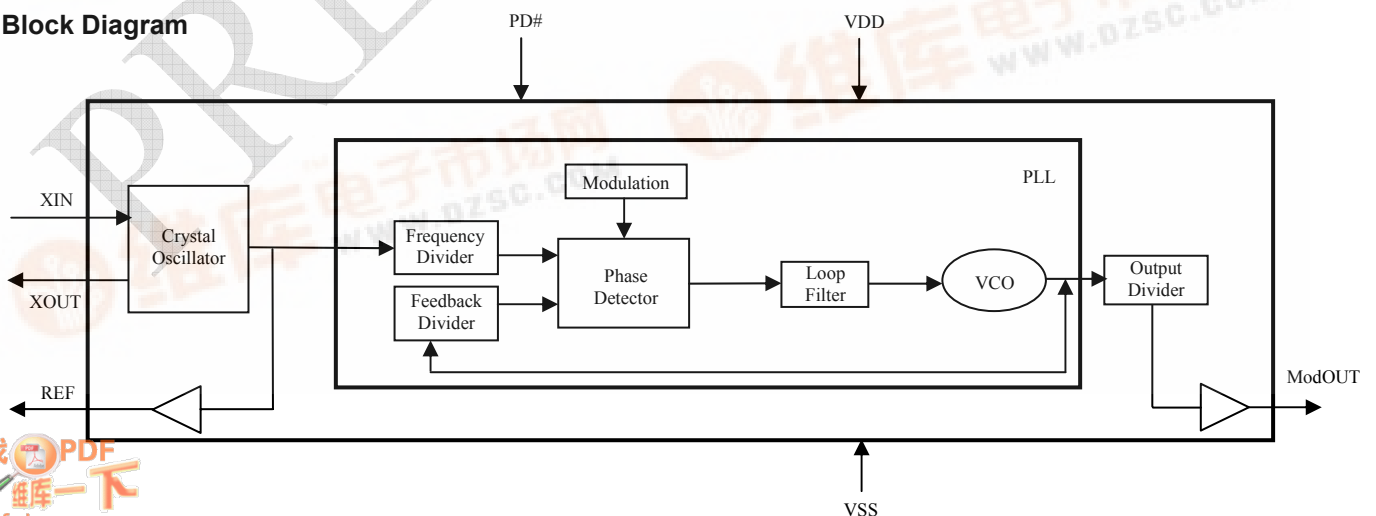
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Pin Configuration

Pin Description

Pin#	Pin Name	Type	Description
1	XIN	I	Connect to externally generated Clock signal or Crystal.
2	VSS	P	Ground Connection. Connect to system ground.
3	NC	-	No Connect.
4	ModOUT	O	Spread spectrum clock output.
5	REF	O	Non-modulated Reference clock output of the input frequency.
6	PD#	I	Power down control pin. Pull LOW to enable Power-Down mode. This pin has an internal pull-up resistor.
7	VDD	P	Connect to +3.3V.
8	XOUT	I	Connect to crystal. No connect if externally generated clock signal is used.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any pin with respect to Ground	-0.5 to +7.0	V
T_{STG}	Storage temperature	-65 to +125	°C
T_A	Operating temperature	0 to 70	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Output Frequency and Modulation Rate

Input Frequency Range (MHz)	Output Frequency Range (MHz)	Modulation Rate	Spread Deviation (%)
20 to 40	20 to 40	Input Frequency / 512	-1.25

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DC Electrical Characteristics

(Test condition: All parameters are measured at room temperature (+25°C) unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low voltage	VSS – 0.3	-	0.8	V
V_{IH}	Input High voltage	2.0	-	VDD + 0.3	V
I_{IL}	Input Low current	-	-	-20.0	µA
I_{IH}	Input High current	-	-	1.0	µA
I_{XOL}	X_{OUT} Output low current @ 0.4V, VDD = 3.3V	-	3	-	mA
I_{XOH}	X_{OUT} Output high current @ 2.5V, VDD = 3.3V	-	3	-	mA
V_{OL}	Output Low voltage VDD = 3.3V, I_{OL} = 20mA	-	-	0.4	V
V_{OH}	Output High voltage VDD = 3.3V, I_{OH} = 20mA	2.5	-	-	V
I_{CC}	Dynamic Supply current 3.3V and 10pF probe loading	7.1 $f_{IN - min}$	-	26.9 $f_{IN - max}$	mA
I_{DD}	Static Supply current	-	4.5	-	mA
VDD	Operating Voltage	-	3.3	-	V
t_{ON}	Power up time (First locked clock cycle after power up)	-	0.18	-	mS
Z_{OUT}	Clock Output impedance	-	50	-	Ω

AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input Frequency	20	-	40	MHz
f_{OUT}	Output Frequency	20	-	40	MHz
t_{LH}[1]	Output Rise time (Measured from 0.8V to 2.0V)	-	0.69	-	nS
t_{HL}[1]	Output Fall time (Measured from 2.0V to 0.8V)	-	0.66	-	nS
t_{JC}	Jitter (Cycle to Cycle)	-200	-	200	pS
t_D	Output Duty cycle	45	50	55	%
Note:1. t_{LH} and t_{HL} are measured into a capacitive load of 15pF					

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Package Information

8-Pin (150-mil) SOIC Package
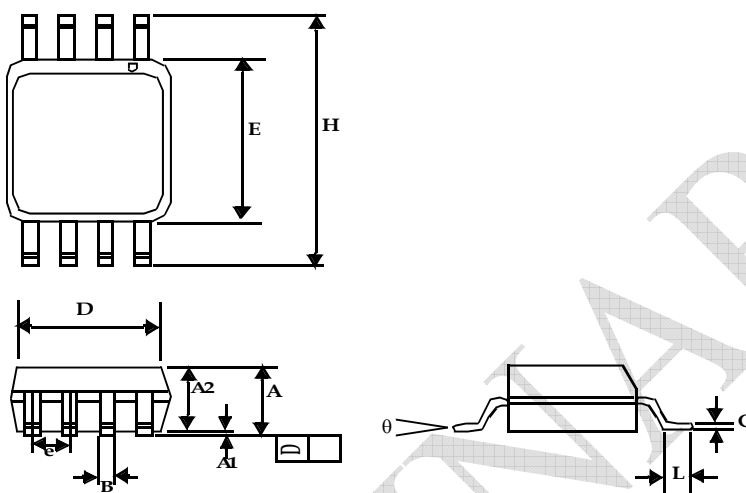
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

Note: Controlling dimensions are millimeters
SOIC – 0.074 grams unit weight

8-lead Thin Shrunk Small Outline Package (4.40-MM Body)
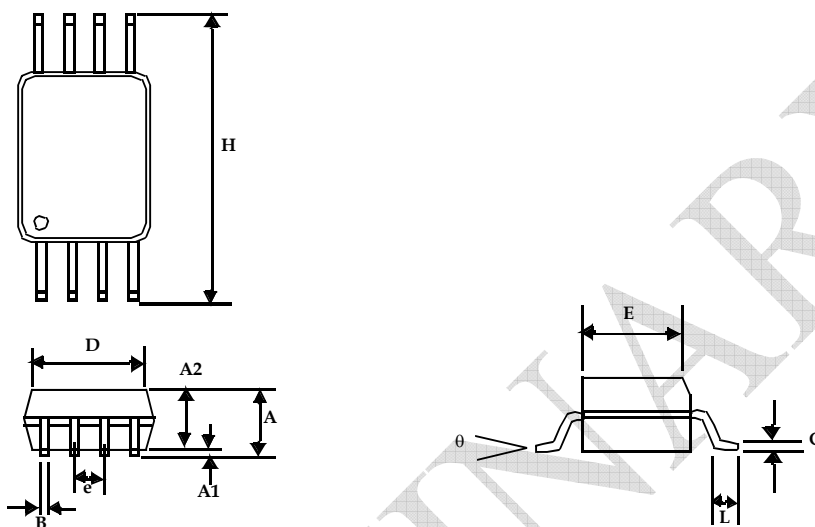
Symbol	Dimensions			
	Inches		Millimeters	
	Min	**Max**	**Min**	**Max**
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°

Note: Controlling dimensions are millimeters
TSSOP – 0.0325 grams unit weight

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Ordering Information

Part number	Marking	Package Configuration	Temperature Range
ASM3P1819N -08-ST	3P1819N	8-Pin SOIC,Tube	Commercial
ASM3P1819N -08-SR	3P1819N	8-Pin SOIC, Tape and Reel	Commercial
ASM3P1819NF-08-ST	3P1819NF	8-Pin SOIC, Tube, Pb Free	Commercial
ASM3P1819NF-08-SR	3P1819NF	8-Pin SOIC, Tape and Reel, Pb Free	Commercial
ASM3P1819NG-08-ST	3P1819NG	8-Pin SOIC, Tube, Green	Commercial
ASM3P1819NG-08-SR	3P1819NG	8-Pin SOIC, Tape and Reel, Green	Commercial
ASM3I1819N -08-ST	3I1819N	8-Pin SOIC, Tube	Industrial
ASM3I1819N -08-SR	3I1819N	8-Pin SOIC, Tape and Reel	Industrial
ASM3I1819NF-08-ST	3I1819NF	8-Pin SOIC, Tube, Pb Free	Industrial
ASM3I1819NF-08-SR	3I1819NF	8-Pin SOIC, Tape and Reel, Pb Free	Industrial
ASM3I1819NG-08-ST	3I1819NG	8-Pin SOIC, Tube, Green	Industrial
ASM3I1819NG-08-SR	3I1819NG	8-Pin SOIC, Tape and Reel, Green	Industrial
ASM3P1819N -08-TT	3P1819N	8-Pin TSSOP, Tube	Commercial
ASM3P1819N -08-TR	3P1819N	8-Pin TSSOP, Tape and Reel	Commercial
ASM3P1819NF-08-TT	3P1819NF	8-Pin TSSOP, Tube, Pb Free	Commercial
ASM3P1819NF-08-TR	3P1819NF	8-Pin TSSOP, Tape and Reel, Pb Free	Commercial
ASM3P1819NG-08-TT	3P1819NG	8-Pin TSSOP, Tube, Green	Commercial
ASM3P1819NG-08-TR	3P1819NG	8-Pin TSSOP, Tape and Reel, Green	Commercial
ASM3I1819N -08-TT	3I1819N	8-Pin TSSOP, Tube	Industrial
ASM3I1819N -08-TR	3I1819N	8-Pin TSSOP, Tape and Reel	Industrial
ASM3I1819NF-08-TT	3I1819NF	8-Pin TSSOP, Tube, Pb Free	Industrial
ASM3I1819NF-08-TR	3I1819NF	8-Pin TSSOP, Tape and Reel, Pb Free	Industrial
ASM3I1819NG-08-TT	3I1819NG	8-Pin TSSOP, Tube, Green	Industrial
ASM3I1819NG-08-TR	3I1819NG	8-Pin TSSOP, Tape and Reel, Green	Industrial

Device Ordering Information

A S M   3 P   1 8 1 9 N F - 0 8 - S R

R = Tape & reel, T = Tube or Tray

O = SOT	U = MSOP
S = SOIC	E = TQFP
T = TSSOP	L = LQFP
A = SSOP	U = MSOP
V = TVSOP	P = PDIP
B = BGA	D = QSOP
Q = QFN	X = SC-70

DEVICE PIN COUNT

F = LEAD FREE AND RoHS COMPLIANT PART
G = GREEN PACKAGE

PART NUMBER

X= Automotive   I= Industrial   P or n/c = Commercial
   (-40C to +125C)   (-40C to +85C)   (0C to +70C)

1 = Reserved	6 = Power Management
2 = Non PLL based	7 = Power Management
3 = EMI Reduction	8 = Power Management
4 = DDR support products	9 = Hi Performance
5 = STD Zero Delay Buffer	0 = Reserved

ALLIANCE SEMICONDUCTOR MIXED SIGNAL PRODUCT

Licensed under US patent #5,488,627, #6,646,463 and #5,631,920

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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to Alliance Semiconductor, dated 11-11-2003