Integrated Circuit Systems, Inc.

ICS9150-08

Frequency Generator & Integrated Buffers for Pentium/Pro™

General Description

The **ICS9150-08** generates all clocks required for high speed RISC or CISC microprocessor systems such as Intel PentiumPro or Cyrix. Eight different reference frequency multiplying factors are selectable.

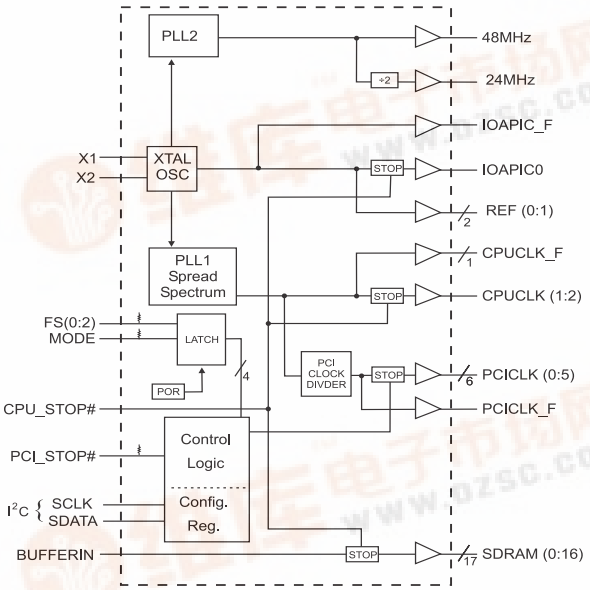
Features include three CPU, seven PCI and seventeen SDRAM clocks. Two reference output is available equal to the crystal frequency, plus two IOAPIC outputs powered by VDDL1. One 48 MHz for USB is provided plus a 24 MHz. Spread Spectrum built in at ±0.5% or ±0.25% modulation to reduce EMI. Serial programming I^2C interface allows changing functions, stop clock programing and Frequency selection. It is not recommended to use dual function I/O pins to clock slots (ISA, PIC, CPU, DIMM). The add on card may have a pull-up or pull-down. Additionally, the device meets the Pentium power-up stabilization, which requires that CPU and PCI clocks be stable within 2ms after power-up.

High drive PCICLK and SDRAM outputs typically provide greater than 1 V/ns slew rate into 30pF loads. CPUCLK outputs typically provide better than 1V/ns slew rate into 20pF loads while maintaining 50±5% duty cycle. The REF, 24 and 48 MHz clock outputs typically provide better than 0.5V/ns slew rates into 20pF.

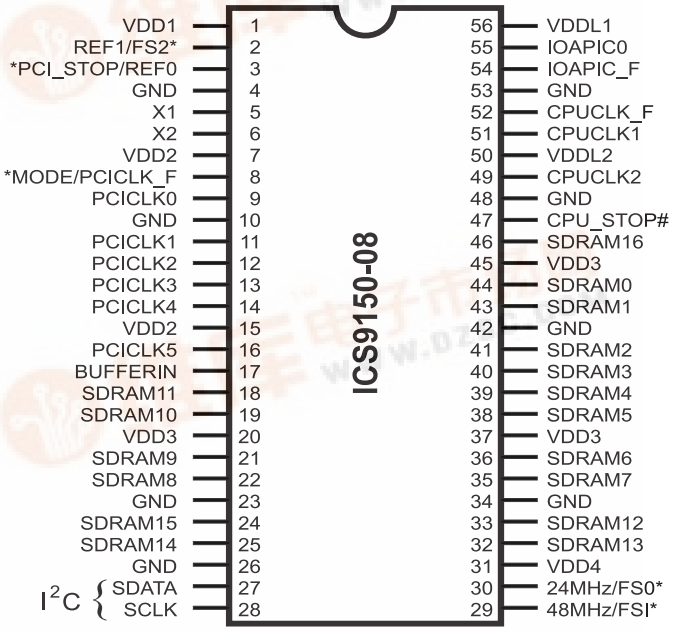
Features

- 3.3V outputs: SDRAM, PCI, REF, 48/24MHz
- 2.5V outputs: CPU, IOAPIC
- 20 ohm CPU clock output impedance
- 20 ohm PCI clock output impedance
- Skew from CPU (earlier) to PCI clock - 1 to 4 ns, center 2.6 ns.
- No external load cap for C_L=18pF crystals
- ±250 ps CPU, PCI clock skew
- 250ps (cycle to cycle) CPU jitter
- Smooth CPU frequency switching from 50 to 133 MHz
- I^2C interface for programming
- 2ms power up clock stable time
- Clock duty cycle 45-55%.
- 56 pin 300 mil SSOP package
- 3.3V operation, 5V tolerant inputs (with series R)
- <5.5ns SDRAM propagation delay from Buffer Input

Block Diagram



Pin Configuration



56-Pin SSOP

* Internal Pull-up Resistor of 240K to 3.3V on indicated inputs

Power Groups

VDD1 = REF (0:1), X1, X2
VDD2 = PCICLK_F, PCICLK(0:5)
VDD3 = SDRAM (0:18), supply for PLL core,
VDD4 = 48MHz, 24MHz
VDDL1 = IOAPIC_F
VDDL2 = CPUCLK_F (1:2)

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2	REF1	OUT	14.318 MHz reference clock output
	FS2[1]	IN	Latched frequency select input. Has pull-up to VDD2.
3	REF0	OUT	14.318MHz reference clock output
	PCI_STOP#	IN	Halts PCICLK (0:5) at logic "0" level when low. (in mobile, MODE=0)
4, 10, 23, 26, 34, 42, 48, 53	GND	PWR	Ground.
5	X1	IN	14.318MHz input. Has internal load cap, (nominal 33pF).
6	X2	OUT	Crystal output. Has internal load cap (33pF) and feedback resistor to X1
8	PCICLK_F	OUT	Free running BUS clock not afected by PCI_STOP#
	MODE[1]	IN	Latched input for MODE select. Converts pin 3 to PCI_STOP# when low for power management.
9, 11, 12, 13, 14, 16	PCICLK (0:5)	OUT	PCI Clock Outputs.
17	BUFFERIN	IN	Input for Buffers
27	SDATA	IN	Serial data in for serial config port. (I^2C)
28	SCLK	IN	Clock input for serial config port. (I^2C)
30	24MHz	OUT	24MHz clock output for Super I/O or FD.
	FS0[1]	IN	Latched frequency select input. Has pull-up to VDD4.
29	48MHz	OUT	48MHz clock output for USB.
	FS1[1]	IN	Latched frequency select input. Has pull-up to VDD2.
1, 7, 15, 20, 31, 37, 45	VDD2, VDD1, VDD3, VDD4	PWR	Nominal 3.3V power supply, see power groups for function.
18, 19, 21, 22, 24, 25, 32, 33, 35, 36, 38, 39, 40 41, 43, 44, 46	SDRAM (1:8) (15:12) (7:0), 16	OUT	SDRAM clocks
47	CPU_STOP#	IN	Halts CPUCLK (1:2), IOAPIC0, SDRAM (0:16) clocks at logic "0" level when low.
50, 56	VDDL2, VDDL1	PWR	CPU and IOAPIC clock buffer power supply, either 2.5 or 3.3V nominal.
55	IOAPIC0	OUT	IOAPIC clock output. (14.318 MHz) Poweredby VDDL1
51, 49	CPUCLK (1:2)	OUT	CPU Output clocks. Powered by VDDL2 (60 or 66.6MHz)
52	CPUCLK_F	OUT	Free running CPU output clock. Not affected ty the CPU_STOP#.
54	IOAPIC_F	OUT	Freerunning IOAPIC clock output. Not affected by the CPU_STOP# (14.31818 MHz) Powered by VDDL1

Notes:

1: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

Mode Pin - Power Management Input Control

MODE, Pin 8 (Latched Input)	Pin 3
0	PCI_STOP# (INPUT)
1	Ref 0 (OUTPUT)

Power Management Functionality

CPU_STOP#	PCI_STOP#	CPUCLK Outputs	PCICLK (0:5)	PCICLK_F, REF, 24/48MHz and SDRAM	Crystal OSC	VCO
0	1	Stopped Low	Running	Running	Running	Running
1	1	Running	Running	Running	Running	Running
1	0	Running	Stopped Low	Running	Running	Running
0	0	Stopped Low	Stopped Low	Running	Running	Running

Functionality

V_{DD}1,2,3 = 3.3V±5%, V_{DDL}1,2 = 2.5V±5% or 3.3±5%, TA=0 to 70°C
Crystal (X1, X2) = 14.31818MHz

FS2	FS1	FS0	CPU (MHz)	PCICLK (MHz)	REF, IOAPIC (MHz)
1	1	1	100.2	33.3 (CPU/3)	14.318
1	1	0	133.3[1]	33.3 (CPU/4)[1]	14.318
1	0	1	112[1]	37.3[1]	14.318
1	0	0	103	34.3 (CPU/3)	14.318
0	1	1	66.8	33.4 (CPU/2)	14.318
0	1	0	83.3	41.65 (CPU/2)	14.318
0	0	1	75	37.5 (CPU/2)	14.318
0	0	0	50	25 (CPU/2)	14.318

Note1. Performance not guaranteed

General I²C serial interface information

A. For the clock generator to be addressed by an I²C controller, the following address must be sent as a start sequence, with an acknoledge bit between each byte.

Clock Generator Address (7 bits)	ACK	+ 8 bits dummy command code	ACK	+ 8 bits dummy Byte count	ACK
A(6:0) & R/W#					
D2(H)					

Then Byte 0, 1, 2, etc in sequence until STOP.

B. The clock generator is a slave/receiver I²C component. It can read back the data stored in the latches for verification. (set R/W# to 1 above) **Read-Back will support Intel PIIX4 "Block-Read" protocol**, with a "Byte count" following the address with R/W#=1, then proceding to Byte 0, 1, 2, ...until STOP.

Clock Generator Address (7 bits)	ACK	Byte Count Readback	ACK
A(6:0) & R/W#			
D3(H)			

Then Byte 0, 1, 2, etc. in sequence until STOP.

C. The data transfer rate supported by this clock generator is 100K bits/sec (standard mode)

D. The input is operating at 3.3V logic levels.

E. The data byte format is 8 bit bytes.

F. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.

G. At power-on, all registers are set to a default condition. Byte 0 defaults to a 0, Bytes 1 through 5 default to a 1 (Enabled output state).

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description			PWD
Bit 7	0 - ±0.25% Spread Spectrum Modulation 1 - ±0.5% Spread Spectrum Modulation			0
	Bit6 Bit5 Bit4	CPU clock	PCI	
Bit 6:4	111	100.2	33.3 (CPU/3)	Note1
	110	133.3[2]	33.3 (CPU/4)[2]	
	101	112.0[2]	37.3 (CPU/3)[2]	
	100	103	34.3 (CPU/3)	
	011	66.8	33.4 (CPU/2)	
	010	83.3	41.65(CPU/2)	
	001	75	37.5 (CPU/2)	
	000	50	25 (CPU/2)	
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 6:4 (above)			0
Bit 2	0 - Spread Spectrum center spread type. 1 - Spread Spectrum down spread type.			0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled			0
Bit 0	0 - Running 1- Tristate all outputs			0

Note1. Default at Power-up will be for latched logic inputs to define frequency. Bits 4, 5, 6 are default to 000, and if bit 3 is written to a 1 to use Bits 6:4, then these should be defined to desired frequency at same write cycle.

Note2. Performance not guaranteed

Note: PWD = Power-Up Default

Byte 1: CPU, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	46	1	SDRAM16 (Act/Inact)
Bit 2	49	1	CPUCLK2 (Act/Inact)
Bit 1	51	1	CPUCLK1 (Act/Inact)
Bit 0	52	1	CPUCLK0 (Act/Inact)

Byte 2: PCI, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	8	1	PCICLKF (Act/Inact)
Bit 5	16	1	PCICLK5 (Act/Inact)
Bit 4	14	1	PCICLK4 (Act/Inact)
Bit 3	13	1	PCICLK3 (Act/Inact)
Bit 2	12	1	PCICLK2 (Act/Inact)
Bit 1	11	1	PCICLK1 (Act/Inact)
Bit 0	9	1	PCICLK0 (Act/Inact)

Byte 3: SDRAM, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	30	1	48MHz (Act/Inact)
Bit 4	29	1	24MHz (Act/Inact)
Bit 3	33, 32, 25, 24	1	SDRAM(12:15) (Act/Inact)
Bit 2	22, 21, 19, 18	1	SDRAM (8:11) (Act/Inact)
Bit 1	39, 38, 36, 35	1	SDRAM (4:7) (Act/Inact)
Bit 0	44, 43, 41, 40	1	SDRAM0 (0:3) (Act/Inact)

Byte 4: Reserved , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	-	Latched FS0#
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	-	Latched FS1#
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

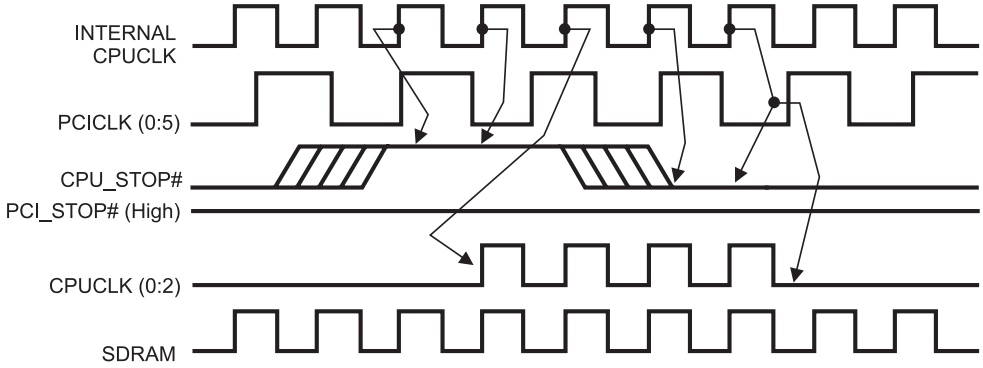
Byte 5: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	-	Latched FS2#
Bit 5	54	1	IOAPIC1 (Act/Inact)
Bit 4	55	1	IOAPIC0 (Act/Inact)
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	2	1	REF1 (Act/Inact)
Bit 0	3	1	REF0 (Act/Inact)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inferted logic load of the input frequency select pin conditions.

CPU_STOP# Timing Diagram

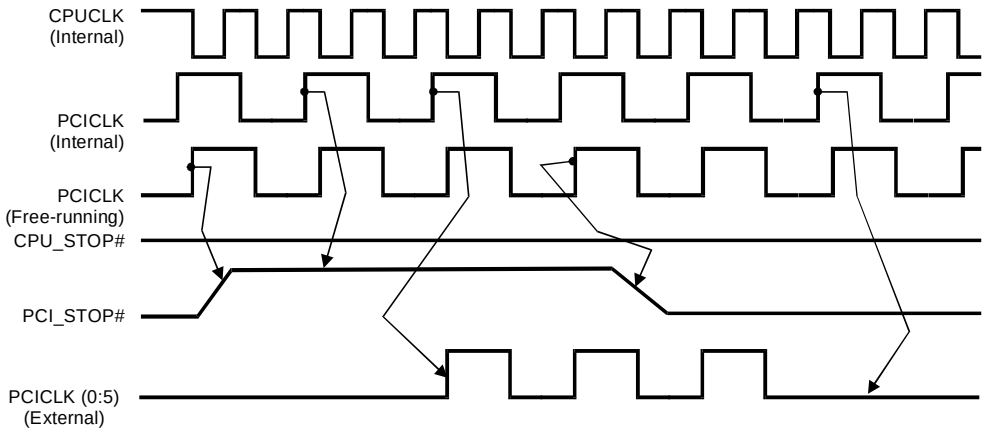
CPUSTOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the **ICS9150-08**. All other clocks will continue to run while the CPUCLKs are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.



Notes:
1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS9150-08.**
3. All other clocks continue to run undisturbed.
4. PCI_STOP# is shown in a high (true) state.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9150-08**. It is used to turn off the PCICLK (0:5) clocks for low power operation. PCI_STOP# is synchronized by the **ICS9150-08** internally. PCICLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:5) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the device.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.

Shared Pin Operation - Input/Output Pins

Pins 8, 29, 30, 54 on the **ICS9150-08** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 4-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm(10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figs. 1 and 2 show the recommended means of implementing this function. In Fig. 1 either one of the resistors is loaded onto the board (selective stuffing) to configure the device's internal logic. Figs. 2a and b provide a single resistor loading option where either solder spot tabs or a physical jumper header may be used.

These figures illustrate the optimal PCB physical layout options. These configuration resistors are of such a large ohmic value that they do not effect the low impedance clock signals. The layouts have been optimized to provide as little impedance transition to the clock signal as possible, as it passes through the programming resistor pad(s).

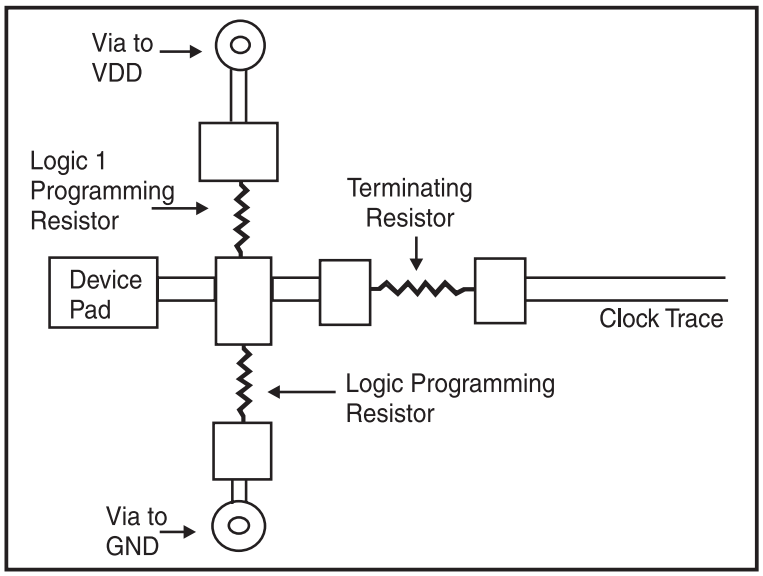


Fig. 1

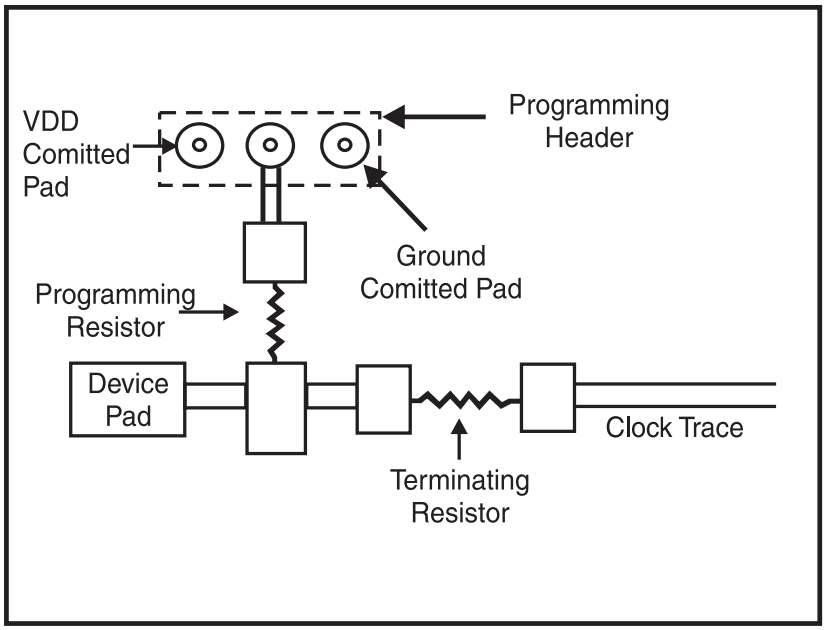

VDD
Comitted
Pad
Programming
Header
Ground
Comitted Pad
Programming
Resistor
Device
Pad
Clock Trace
Terminating
Resistor

Fig. 2a

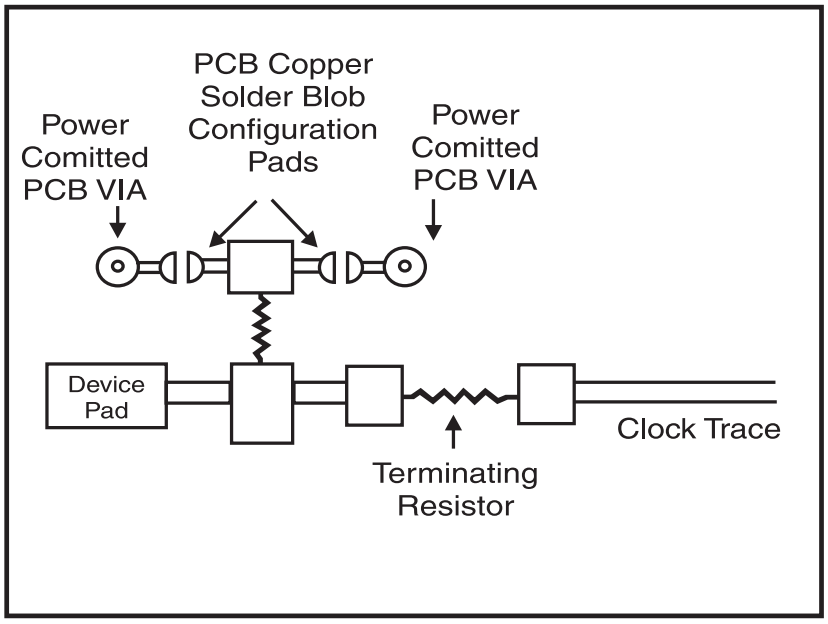

PCB Copper
Solder Blob
Configuration
Pads
Power
Comitted
PCB VIA
Power
Comitted
PCB VIA
Device
Pad
Clock Trace
Terminating
Resistor

Fig. 2b

Absolute Maximum Ratings

Supply Voltage . . . . . 7.0 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Supply Current	I_{DD}	C_L = 0 pF; Select @ 66M		100	180	mA
	I_{DDL}			6.0	30	mA
Input frequency	F_i	V_{DD} = 3.3 V;		14.318		MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	ps
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.		1.5	3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew[1]	$T_{CPU-BUS}$	V_T = 1.5 V;	1.0	2.6	4.0	ns

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2A}[1]	$V_O = V_{DD}*(0.5)$	10		20	Ω
Output Impedance	R_{DSN2A}[1]	$V_O = V_{DD}*(0.5)$	10		20	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2	2.3		V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA		0.2	0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V		-30	-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	25	37		mA
Rise Time	t_{r2A}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V @ 66MHz		1.3	1.6	ns
Fall Time	t_{f2A}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V @ 66MHz		1.1	1.6	ns
Duty Cycle	d_{t2A}[1]	V_T = 1.25 V	45.0	51.0	55.0	%
Skew (Window)	t_{sk2A}[1]	V_T = 1.25 V		40	250	ps
Jitter	period(norm)	V_T = 1.25 V; 100MHz	9.75	10	10.25	ns
	period(spr)	V_T = 1.25 V; 100MHz	9.75	10	10.35	ns
	t_{j1s2A}[1]	V_T = 1.25 V		120	350	ps
	t_{jabs2A}[1]	V_T = 1.25 V	-250	100	+250	ps
	Dev run avg	V_T = 1.25 V		150	250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	23	55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12	20	55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -28 mA	2.4	2.9		V
Output Low Voltage	V_{OL1}	I_{OL} = 23 mA		0.2	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-58	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	25	52		mA
Rise Time	t_{r1}[1]	V_{OL} = 0.8 V, V_{OH} = 2.4 V		1.5	2.0	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.8 V		1.4	2.0	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45.0	50.0	55.0	%
Skew	t_{sk1}[1]	V_T = 1.5 V		80	250	ps
Jitter	t_{j1s1}[1]	V_T = 1.5 V		50	150	ps
	t_{jabs1}[1]	V_T = 1.5 V		200	500	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} =V_{DDL} 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2A}[1]	$V_O = V_{DD}*(0.5)$	10		20	Ω
Output Impedance	R_{DSN2A}[1]	$V_O = V_{DD}*(0.5)$	10		20	Ω
Output High Voltage	V_{OH2A}	I_{OH} = -28 mA	2.4	3		V
Output Low Voltage	V_{OL2A}	I_{OL} = 19 mA		0.3	0.4	V
Output High Current	I_{OH2A}	V_{OH} = 2.0 V		-72	-42	mA
Output Low Current	I_{OL2A}	V_{OL} = 0.8 V	33	55		mA
Rise Time	t_{r2A}[1]	V_{OL} = 0.8 V, V_{OH} = 2.4 V		1.6	2.0	ns
Fall Time	t_{f2A}[1]	V_{OH} = 2.4 V, V_{OL} = 0.8 V		1.2	2.0	ns
Duty Cycle	d_{t2A}[1]	V_T = 1.5 V	41	46	51	%
Skew (output to output)	t_{sk2A}[1]	V_T = 1.5 V		200	600	ps
Skew Propagation Delay (Bufferin to output)	t_{sk2A}[1]	V_T = 1.5 V		4.5	55	ns

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 24M, 48M, REF 1

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP5}[1]	$V_O = V_{DD}*(0.5)$		20	60	W
Output Impedance	R_{DSN5}[1]	$V_O = V_{DD}*(0.5)$		55	100	W
Output High Voltage	V_{OH5}	I_{OH} = -8 mA	2.4	2.9		V
Output Low Voltage	V_{OL5}	I_{OL} = 8 mA		0.18	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-42	-14	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	26		mA
Rise Time	t_{r5}[1]	V_{OL} = 0.8 V, V_{OH} = 2.4 V		1.2	2.0	ns
Fall Time	t_{f5}[1]	V_{OH} = 2.4 V, V_{OL} = 0.8 V		2.0	2.4	ns
Duty Cycle	d_{t5}[1]	V_T = 1.5 V	40.0	54.0	60.0	%
Jitter	t_{j1s5}[1]	V_T = 1.5 V		100	2.1	ns
	t_{jabs5}[1]	V_T = 1.5 V		0.35	3.5	ns

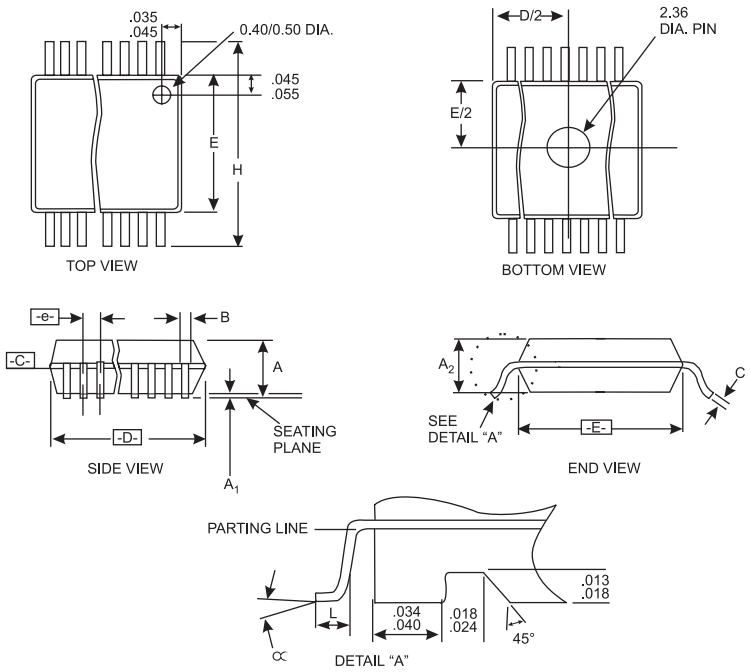
[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP5}[1]	V_O = V_{DD}*(0.5)		20	60	W
Output Impedance	R_{DSN5}[1]	V_O = V_{DD}*(0.5)		55	100	W
Output High Voltage	V_{OH5}	I_{OH} = -8 mA	2.4	2.9		V
Output Low Voltage	V_{OL5}	I_{OL} = 1.2 mA		0.2	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-42	-14	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	10	27		mA
Rise Time	t_{r5}[1]	V_{OL} = 0.8 V, V_{OH} = 2.4 V		2.0	2.6	ns
Fall Time	t_{f5}[1]	V_{OH} = 2.4 V, V_{OL} = 0.8 V		2.8	3.2	ns
Duty Cycle	d_{t5}[1]	V_T = 1.5 V	48.0	54.0	58.0	%
Jitter	t_{j1s5}[1]	V_T = 1.5 V		100	250	ns
	t_{jabs5}[1]	V_T = 1.5 V		550	800	ps

[1]Guarenteed by design, not 100% tested in production.



SSOP Package

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016	AD	.720	.725	.730	56
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	-	.010					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∝	0°	5°	8°					
X	.085	.093	.100					

Ordering Information

ICS9150F-08

Example:

ICS XXXX F - PPP

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device