



Integrated
Circuit
Systems, Inc.

ICS9148-10

Pentium/Pro™ System Clock Chip

General Description

The **ICS9148-10** is a Clock Synthesizer chip for Pentium and PentiumPro CPU based Desktop/Notebook systems that will provide all necessary clock timing.

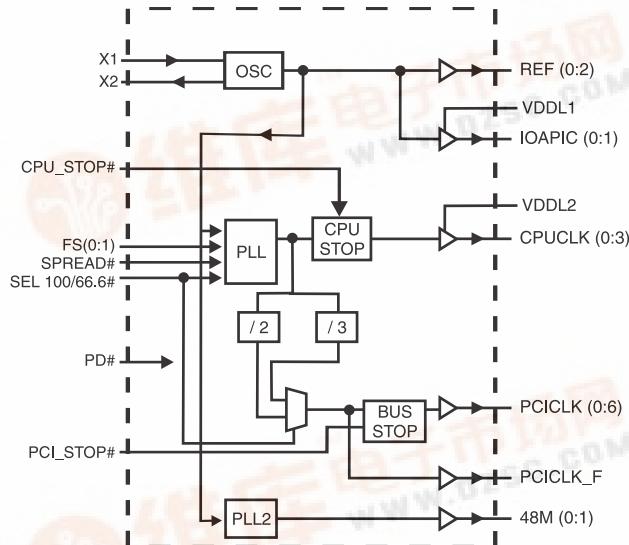
Features include four CPU and eight PCI clocks. Three reference outputs are available equal to the crystal frequency. Additionally, the device meets the Pentium power-up stabilization requirement, assuring that CPU and PCI clocks are stable within 2ms after power-up.

PD# pin enables low power mode by stopping crystal OSC and PLL stages. Other power management features include CPU_STOP#, which stops CPU (0:3) clocks, and PCI_STOP#, which stops PCICLK (0:6) clocks.

High drive CPUCLK outputs typically provide greater than 1 V/ns slew rate into 20pF loads. PCICLK outputs typically provide better than 1V/ns slew rate into 30pF loads while maintaining 50±5% duty cycle. The REF clock outputs typically provide better than 0.5V/ns slew rates.

The **ICS9148-10** accepts a 14.318MHz reference crystal or clock as its input and runs on a 3.3V core supply.

Block Diagram



Power Groups

VDD = Supply for PLL core
 VDD1 = REF (0:2), X1, X2
 VDD2 = PCICLK_F, PCICLK (0:6)
 VDD3 = 48MHz0, 48MHz1
 VDDL1 = IOAPIC (0:1)
 VDDL2 = CPUCLK (0:3)

Ground Groups

GND = Ground for PLL core
 GND1 = REF (0:2), X1, X2
 GND2 = PCICLK_F, PCICLK (0:6)
 GND3 = 48MHz0, 48MHz1
 GNDL1 = IOAPIC (0:1)
 GNDL2 = CPUCLK (0:3)

Features

- Generates system clocks for CPU, IOAPIC, PCI, plus 14.314 MHz REF (0:2), USB, and Super I/O
- Supports single or dual processor systems
- Supports Spread Spectrum modulation for CPU & PCI clocks, down spread -1%
- Skew from CPU (earlier) to PCI clock (rising edges for 100/33.3MHz) 1.5 to 4ns
- Two fixed outputs at 48MHz.
- Separate 2.5V and 3.3V supply pins
- 2.5V or 3.3V output: CPU, IOAPIC
- 3.3V outputs: PCI, REF, 48MHz
- No power supply sequence requirements
- Uses external 14.318MHz crystal, no external load cap required for $C_L=18\text{pF}$ crystal
- 48 pin 300 mil SSOP

Pin Configuration

REF0	1	VDD1
REF1	2	REF2
GND1	3	VDDL1
X1	4	IOAPIC0
X2	5	IOAPIC1
GND2	6	GNDL1
PCICLK_F	7	N/C
PCICLK0	8	VDDL2
VDD2	9	CPUCLK0
PCICLK1	10	CPUCLK1
PCICLK2	11	GNDL2
PCICLK3	12	VDDL2
PCICLK4	13	CPUCLK2
VDD2	14	CPUCLK3
PCICLK5	15	GNDL2
PCICLK6	16	VDD
GND2	17	GND
VDD	18	PCI_STOP#
GND	19	CPU_STOP#
VDD3	20	PD#
48MHz0	21	SPREAD#
48MHz1	22	FS0
GND3	23	FS1
	24	SEL 100/66.6#

48-Pin SSOP



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 2, 47	REF (0:2)	OUT	14.318MHz clock output
3	GND1	PWR	Ground for REF outputs
4	X1	IN	XTAL_IN 14.318MHz Crystal input, has internal 33pF load cap and feed back resistor from X2
5	X2	OUT	XTAL_OUT Crystal output, has internal load cap 33pF
6, 12, 18	GND2	PWR	Ground for PCI outputs
7	PCICLK_F	OUT	Free Running PCI output
8, 10, 11, 13, 14, 16, 17	PCICLK (0:6)	OUT	PCI clock outputs. TTL compatible 3.3V
9, 15	VDD2	PWR	Power for PCICLK outputs, nominally 3.3V
19, 33	VDD	PWR	Isolated power for core, nominally 3.3V
20, 32	GND	PWR	Isolated ground for core
21	VDD3	PWR	Power for 48MHz outputs, nominally 3.3V
22, 23	48MHz (0:1)	OUT	48MHz outputs
24	GND3	PWR	Ground for 48MHz outputs
25	SEL100/66.6#	IN	Select pin for enabling 100MHz or 66.6MHz H=100MHz, L=66.6MHz (PCI always synchronous 33.3MHz)
26, 27	FS (0:1)	IN	Frequency Select pins
28	SPREAD#	IN	Enables Spread Spectrum feature when LOW
29	PD#	IN	Powers down chip, active low
30	CPU_STOP#	IN	Halts CPU clocks at logic "0" level when low
31	PCL_STOP#	IN	Halts PCI Bus at logic "0" level when low
37, 41	VDDL2	PWR	Power for CPU outputs, nominally 2.5V
34, 38	GNDL2	PWR	Ground for CPU outputs.
35, 36, 39, 40	CPUCLK (3:0)	OUT	CPU and Host clock outputs @ 2.5V
42	N/C	-	Not internally connected
43	GNDL1	PWR	Ground for IOAPIC outputs
44, 45	IOAPIC (0:1)	OUT	IOAPIC outputs (14.318MHz) @ 2.5V
46	VDDL1	PWR	Power for IOAPIC outputs, nominally 2.5V
48	VDD1	PWR	Supply for REF (0:2), X1, X2, nominal 3.3V

Select Functions

Functionality	CPU	PCI, PCI_F	REF	IOAPIC	48 MHz Selection
Tristate	HI - Z	HI - Z	HI - Z	HI - Z	HI - Z
Testmode	TCLK/2 ¹	TCLK/6 ¹	TCLK ¹	TCLK ¹	TCLK/2 ¹
Spread Spectrum	Modulated ²	Modulated ²	14.318MHz	14.318MHz	48.0MHz

SEL 100/66#	FS1	FS0	Function
0	0	0	Tri-State
0	0	1	59.7 ³
0	1	0	74.6 ³
0	1	1	Active 66.6MHz CPU, 33.3 PCI
1	0	0	Test Mode
1	0	1	133.3 ³
1	1	0	82.9 ³
1	1	1	Active 100MHz CPU, 33.3 PCI

Notes:

1. TCLK is a test clock driven on the X1 (crystal in pin) input during test mode.
2. -1% modulation down spread from the selected frequency.
3. Performance not guaranteed



Technical Pin Function Descriptions

VDD(1,2,3)

This is the power supply to the internal core logic of the device as well as the clock output buffers for REF(0:2), PCICLK_F, PCICLK(0:6), 48MHz0, 48MHz1.

This pin operates at 3.3V volts. Clocks from the listed buffers that it supplies will have a voltage swing from Ground to this level. For the actual guaranteed high and low voltage levels for the Clocks, please consult the DC parameter table in this data sheet.

VDDL1,2

This is the power supply for the CPUCLK (0:3) and IOAPIC output buffers. The voltage level for these outputs may be 2.5 or 3.3volts. Clocks from the buffers that each supplies will have a voltage swing from Ground to this level. For the actual Guaranteed high and low voltage levels of these Clocks, please consult the DC parameter table in this Data Sheet.

GND(1,2,3)

This is the ground to the internal core logic of the device as well as the clock output buffers for REF(0:2), PCICLK_F, PCICLK(0:6), 48MHz0, 48MHz1.

GNDL(1,2)

This is the ground for the CPUCLK (0:3) and IOAPIC output buffers.

X1

This input pin serves one of two functions. When the device is used with a Crystal, X1 acts as the input pin for the reference signal that comes from the discrete crystal. When the device is driven by an external clock signal, X1 is the device input pin for that reference clock. This pin also implements an internal Crystal loading capacitor that is connected to ground. With a nominal value of 33pF no external load cap is needed for a $C_L=17$ to 18pF crystal.

X2

This Output pin is used only when the device uses a Crystal as the reference frequency source. In this mode of operation, X2 is an output signal that drives (or excites) the discrete Crystal. The X2 pin will also implement an internal Crystal loading capacitor nominally 33pF.

CPUCLK(0:3)

These Output pins are the Clock Outputs that drive processor and other CPU related circuitry that requires clocks which are in tight skew tolerance with the CPU clock. The voltage swing of these Clocks is controlled by the Voltage level applied to the VDDL2 pin of the device. See the Functionality Table for a list of the specific frequencies that are available for these Clocks and the selection codes to produce them.

48MHz(0:1)

This is a fixed frequency Clock output that is typically used to drive Super I/O devices. Outputs 0 and 1 are defined as 48MHz.

IOAPIC(0:1)

This Output is a fixed frequency Output Clock that runs at the Reference Input (typically 14.31818MHz). Its voltage level swing is controlled by VDDL1 and may operate at 2.5 or 3.3volts.

REF(0:2)

The REF Outputs are fixed frequency Clocks that run at the same frequency as the Input Reference Clock X1 or the Crystal (typically 14.31818MHz) attached across X1 and X2.

PCICLK_F

This Output is equal to PCICLK(0:6) and is FREE RUNNING, and will not be stopped by PCI_STOP#.

PCICLK(0:6)

These Output Clocks generate all the PCI timing requirements for a Pentium/Pro based system. They conform to the current PCI specification. They run at 33.3 MHz.

SELECT 100/66.6MHz#

This Input pin controls the frequency of the Clocks at the CPUCLK, PCICLK and SDRAM output pins. If a logic "1" value is present on this pin, the 100MHz Clock will be selected. If a logic "0" is used, the 66.6MHz frequency will be selected. The PCI clock is multiplexed to be 33.3MHz for both select cases. PCI is synchronous at the rising edge of PCI to the CPU rising edge (with the skew making CPU early).

PWR_DWN#

This is an asynchronous active Low Input pin used to Power Down the device into a Low Power state by not removing the power supply. The internal Clocks are disabled and the VCO and Crystal are stopped. Powered Down will also place all the Outputs in a low state at the end of their current cycle. The latency of Power Down will not be greater than 3ms.

CPU_STOP#

This is a synchronous active Low Input pin used to stop the CPUCLK clocks in an active low state. All other Clocks including SDRAM clocks will continue to run while this function is enabled. The CPUCLK's will have a turn ON latency of at least 3 CPU clocks.

PCI_STOP#

This is a synchronous active Low Input pin used to stop the PCICLK clocks in an active low state. It will not affect PCICLK_F nor any other outputs.



Power Management

Clock Enable Configuration

CPU_STO-P#	PCI_STOP#	PWR_DWN-#	CPUCLK	PCICLK	Other Clocks, REF, IOAPICs, 48 MHz 0 48 MHz 1	Crystal	VCOs
X	X	0	Low	Low	Stopped	Off	Off
0	0	1	Low	Low	Running	Running	Running
0	1	1	Low	33.3 MHz	Running	Running	Running
1	0	1	100/66.6MHz-z	Low	Running	Running	Running
1	1	1	100/66.6MHz-z	33.3 MHz	Running	Running	Running

Full clock cycle timing is guaranteed at all times after the system has initially powered up except where noted. During power up and power down operations using the PD# select pin will not cause clocks of a shorter or longer pulse than that of the running clock. The first clock pulse coming out of a stopped clock condition may be slightly distorted due to clock network charging circuitry. Board routing and signal loading may have a large impact on the initial clock distortion also.

ICS9148-10 Power Management Requirements

SIGNAL	SIGNAL STATE	Latency
		No. of rising edges of free running PCICLK
CPU_STOP#	0 (Disabled) ²	1
	1 (Enabled) ¹	1
PCI_STOP#	0 (Disabled) ²	1
	1 (Enabled) ¹	1
PD#	1 (Normal Operation) ³	3ms
	0 (Power Down) ⁴	2max

Notes.

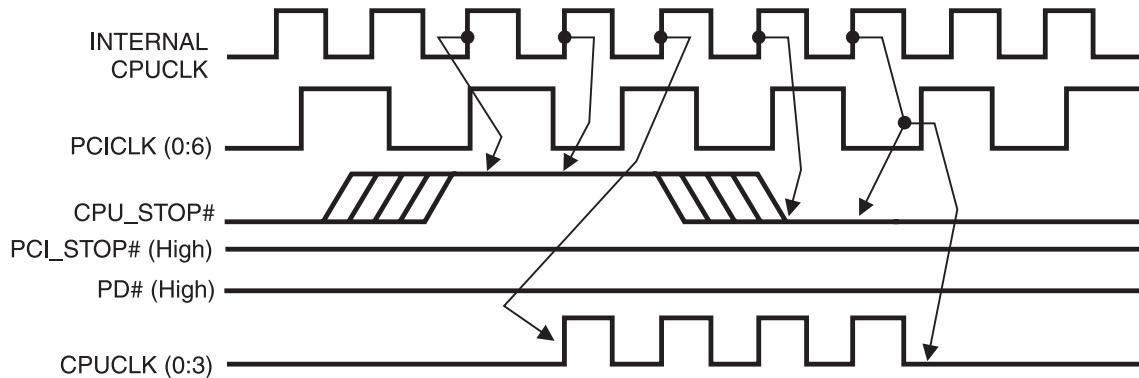
1. Clock on latency is defined from when the clock enable goes active to when the first valid clock comes out of the device.
2. Clock off latency is defined from when the clock enable goes inactive to when the last clock is driven low out of the device.
3. Power up latency is when PD# goes inactive (high) to when the first valid clocks are output by the device.
4. Power down has controlled clock counts applicable to CPUCLK, PCICLK only.

The REF and IOAPIC will be stopped independent of these.



CPU_STOP# Timing Diagram

CPUSTOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the **ICS9148-10**. The minimum that the CPUCLK is enabled (CPU_STOP# high pulse) is 100 CPUCLKs. All other clocks will continue to run while the CPUCLKs are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.

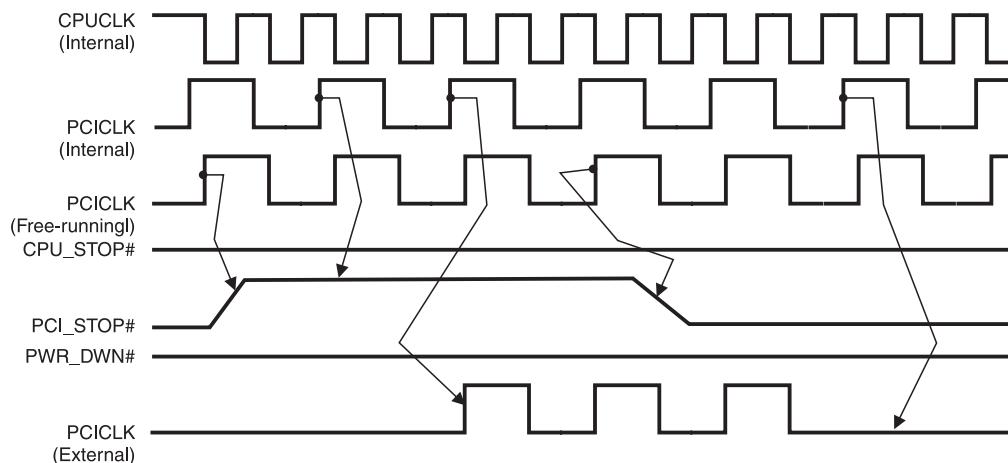


Notes:

1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist.
This signal is synchronized to the CPUCLKs inside the **ICS9148-10**.
3. All other clocks continue to run undisturbed.
4. PD# and PCI_STOP# are shown in a high (true) state.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9148-10**. It is used to turn off the PCICLK (0:6) clocks for low power operation. PCI_STOP# is synchronized by the **ICS9148-10** internally. The minimum that the PCICLK (0:6) clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK (0:6) clocks. PCICLK (0:6) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:6) clock on latency cycles are only one rising PCICLK. Clock off latency is one PCICLK clock.



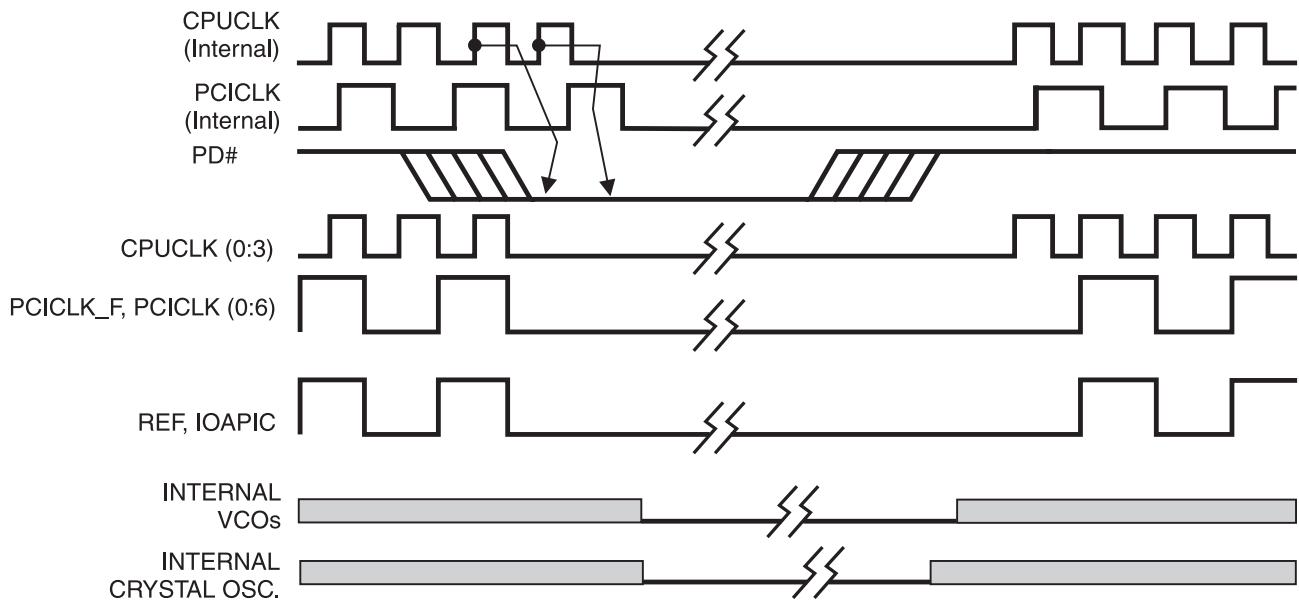
Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9148 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9148-10.
3. All other clocks continue to run undisturbed.
4. PD# and CPU_STOP# are shown in a high (true) state.



PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal is synchronized internally by the **ICS9148-10** prior to its control action of powering down the clock synthesizer. Internal clocks will not be running after the device is put in power down state. When PD# is active (low) all clocks are driven to a low state and held prior to turning off the VCOs and the Crystal oscillator. The power on latency is guaranteed to be less than 3ms. The power down latency is less than three CPUCLK cycles. PCI_STOP# and CPU_STOP# are don't care signals during the power down operations.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9148 device).
2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside the ICS9148.
3. The shaded sections on the VCO and the Crystal signals indicate an active clock is being generated.



Absolute Maximum Ratings

Supply Voltage	7.0 V
Logic Inputs	GND -0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature.....	0°C to +70°C
Storage Temperature	-65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ C$; Supply Voltage $V_{DD} = V_{DDL} = 3.3 V \pm 5\%$ (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		$V_{DD} + 0.3$	V
Input Low Voltage	V_{IL}		$V_{SS} - 0.3$		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$		0.1	5	μA
Input Low Current	I_{IL1}	$V_{IN} = 0 V$; Inputs with no pull-up resistors	-5	2.0		μA
Input Low Current	I_{IL2}	$V_{IN} = 0 V$; Inputs with pull-up resistors	-200	-100		μA
Operating Supply Current	$I_{DD3.3OP66}$	C_L = Loaded at Cmax pF; Select @ 66MHz		74	170	mA
	$I_{DD3.3OP100}$	C_L = Loaded at Cmax pF; Select @ 100MHz		79	170	mA
Power Down Supply Current	$I_{DD3.3PD}$	C_L = Loaded at Cmax pF; With input address to Vdd c	3	500		μA
Input frequency	F_i	$V_{DD} = 3.3 V$;		14.318		MHz
Input Capacitance ¹	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time ¹	T_{trans}	To 1st crossing of target Freq.			3	ms
Settling Time ¹	T_s	From 1st crossing to 1% target Freq.		5		ms
Clk Stabilization ¹	T_{STAB}	From $V_{DD} = 3.3 V$ to 1% target Freq.			3	ms
Skew ¹	$T_{CPU-PCI1}$	$V_T = 1.5 V$;	1.5	3	4	ns

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ C$; Supply Voltage $V_{DD} = 3.3 V \pm 5\%$, $V_{DDL} = 2.5 V \pm 5\%$ (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5OP66}$	$C_L = 20 pF$; Select @ 66.8 MHz		28	70	mA
	$I_{DD2.5OP100}$	$C_L = pF$; Select @ 100 MHz		43	100	mA
Skew ¹	$t_{CPU-PCI2}$	$V_T = 1.5 V$; $V_{IL} = 1.25 V$	1.5	3	4	ns

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

TA = 0 - 70C; VDD = 3.3 V +/- 5%; VDDL = 2.5 V +/- 5%; CL = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R _{DSP2B} ¹	V _O = V _{DD} *(0.5)	13.5		45	Ω
Output Impedance	R _{DSN2B} ¹	V _O = V _{DD} *(0.5)	13.5		45	Ω
Output High Voltage	V _{OH2B}	I _{OH} = -12.0 mA	2	2.3		V
Output Low Voltage	V _{OL2B}	I _{OL} = 12 mA		0.2	0.4	V
Output High Current	I _{OH2B}	V _{OH} = 1.7 V		-41	-19	mA
Output Low Current	I _{OL2B}	V _{OL} = 0.7 V	19	37		mA
Rise Time	t _{r2B} ¹	V _{OL} = 0.4 V, V _{OH} = 2.0 V		1.25	1.6	ns
Fall Time	t _{f2B} ¹	V _{OH} = 2.0 V, V _{OL} = 0.4 V		1	1.6	ns
Duty Cycle	d _{t2B} ¹	V _T = 1.25 V	45	48	55	%
Skew	t _{sk2B} ¹	V _T = 1.25 V		30	175	ps
Jitter, Cycle-to-cycle	t _{jcyc-cyc2B} ¹	V _T = 1.25 V		150	250	ps
Jitter, One Sigma	t _{j1s2B} ¹	V _T = 1.25 V		40	150	ps
Jitter, Absolute	t _{jabs2B} ¹	V _T = 1.25 V	-250	140	+250	ps

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

TA = 0 - 70C; VDD = 3.3 V +/- 5%; VDDL = 2.5 V +/- 5%; CL = 20 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance ¹	R _{DSP4B}	V _O = V _{DD} *(0.5)	13.5		45	Ohm
Output Impedance ¹	R _{DSN4B}	V _O = V _{DD} *(0.5)	13.5		45	Ohm
Output High Voltage	V _{OH4B}	I _{OH} = -18 mA	2	2.2		V
Output Low Voltage	V _{OL4B}	I _{OL} = 18 mA		0.33	0.4	V
Output High Current	I _{OH4B}	V _{OH} = 1.7 V		-41	-28	mA
Output Low Current	I _{OL4B}	V _{OL} = 0.7 V	29	37		mA
Rise Time ¹	T _{r4B}	V _{OL} = 0.4 V, V _{OH} = 2.0 V		1.3	1.6	ns
Fall Time ¹	T _{f4B}	V _{OH} = 2.0 V, V _{OL} = 0.4 V		1.1	1.6	ns
Duty Cycle ¹	D _{t4B}	V _T = 1.25 V	45	54	55	%
Skew ¹	t _{sk4B} ¹	V _T = 1.25 V		60	250	ps
Jitter, One Sigma ¹	T _{j1s4B}	V _T = 1.25 V		1	3	%
Jitter, Absolute ¹	T _{jabs4B}	V _T = 1.25 V	-5		5	%

¹Guaranteed by design, not 100% tested in production.

**ICS9148-10**

Electrical Characteristics - PCICLK

TA = 0 - 70C; VDD = VDDL = 3.3 V +/- 5%; CL = 30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance ¹	RDSP1	VO = VDD*(0.5)	12		55	Ohm
Output Impedance ¹	RDSN1	VO = VDD*(0.5)	12		55	Ohm
Output High Voltage	VOH1	IOH = -11 mA	2.4	3.1		V
Output Low Voltage	VOL1	IOL = 9.4 mA		0.1	0.4	V
Output High Current	IOH1	VOH = 2.0 V		-62	-22	mA
Output Low Current	IOL1	VOL = 0.8 V	16	57		mA
Rise Time ¹	tr1	VOL = 0.4 V, VOH = 2.4 V		1.5	2	ns
Fall Time ¹	tfl	VOH = 2.4 V, VOL = 0.4 V		1.1	2	ns
Duty Cycle ¹	dt1	VT = 1.5 V	45	50	55	%
Skew ¹	tsk1	VT = 1.5 V		140	500	ps
Jitter, One Sigma ¹	tj1s1	VT = 1.5 V		17	150	ps
Jitter, Absolute ¹	tjabs1	VT = 1.5 V	-500	70	500	ps

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

TA = 0 - 70C; VDD = VDDL = 3.3 V +/- 5%; CL = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance ¹	RDSP5	VO = VDD*(0.5)	13.5		45	Ohm
Output Impedance ¹	RDSN5	VO = VDD*(0.5)	13.5		45	Ohm
Output High Voltage	VOH5	IOH = -16 mA	2.4	3.1		V
Output Low Voltage	VOL5	IOL = 9 mA		0.17	0.4	V
Output High Current	IOH5	VOH = 2.0 V		-44	-22	mA
Output Low Current	IOL5	VOL = 0.8 V	29	42		mA
Rise Time ¹	tr5	VOL = 0.4 V, VOH = 2.4 V		1.4	2	ns
Fall Time ¹	tfl5	VOH = 2.4 V, VOL = 0.4 V		1.1	2	ns
Duty Cycle ¹	dt5	VT = 1.5 V	45	53	55	%
Jitter, One Sigma ¹	tj1s5	VT = 1.5 V		1	3	%
Jitter, Absolute ¹	tjabs5	VT = 1.5 V		3	5	%

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - 48 MHz

$T_A = 0 - 70^\circ C$; $V_{DD} = V_{DDL} = 3.3 V \pm 5\%$; $C_L = 10 - 20 \text{ pF}$ (unless otherwise stated)

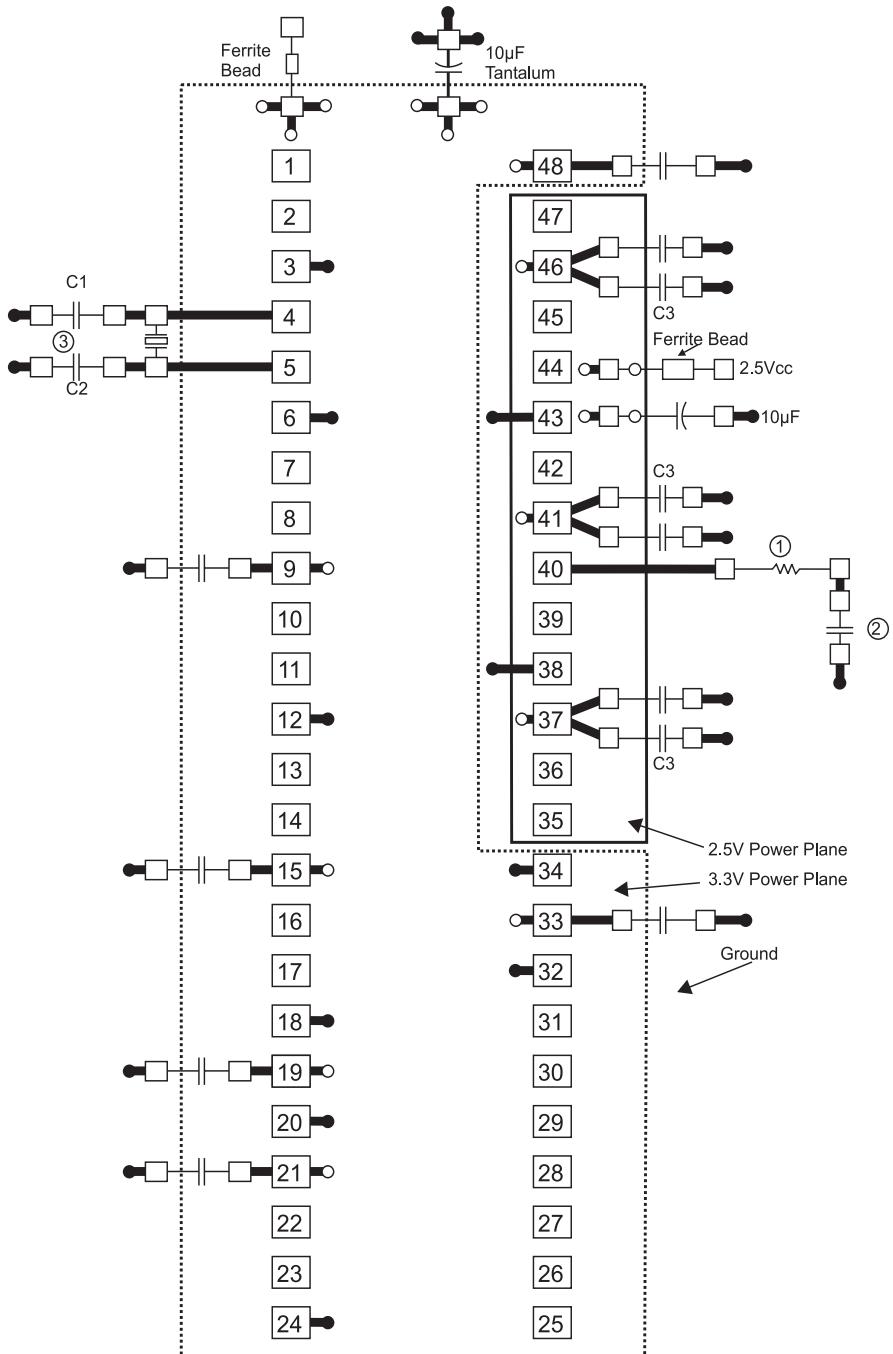
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Accuracy ¹	FACC48m				167	ppm
Output Impedance ¹	R_{DSP5}	$V_O = V_{DD} * (0.5)$	20		60	Ohm
Output Impedance ¹	R_{DSN5}	$V_O = V_{DD} * (0.5)$	20		60	Ohm
Output High Voltage	V_{OH5}	$I_{OH} = -16 \text{ mA}$	2.4	3		V
Output Low Voltage	V_{OL5}	$I_{OL} = 9 \text{ mA}$		0.14	0.4	V
Output High Current	I_{OH5}	$V_{OH} = 2.0 \text{ V}$		-44	-22	mA
Output Low Current	I_{OL5}	$V_{OL} = 0.8 \text{ V}$	16	42		mA
Rise Time ¹	t_{r5}	$V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.4 \text{ V}$		1.2	4	ns
Fall Time ¹	t_{f5}	$V_{OH} = 2.4 \text{ V}$, $V_{OL} = 0.4 \text{ V}$		1.2	4	ns
Duty Cycle ¹	d_{t5}	$V_T = 1.5 \text{ V}$	45	52	55	%
Jitter, One Sigma ¹	t_{j1s5}	$V_T = 1.5 \text{ V}$		1	3	%
Jitter, Absolute ¹	t_{jabs5}	$V_T = 1.5 \text{ V}$		3	5	%

¹Guaranteed by design, not 100% tested in production.



General Layout Precautions:

- 1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
- 2) Make all power traces and vias as wide as possible to lower inductance.



Notes:

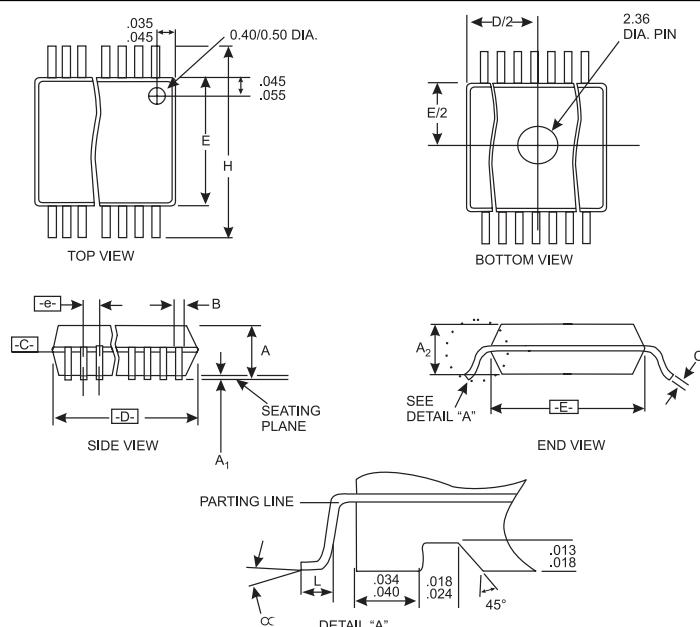
- 1 All clock outputs should have series terminating resistor. Not shown in all places to improve readability of diagram
- 2 Optional EMI capacitor should be used on all CPU, SDRAM, and PCI outputs.
- 3 Optional crystal load capacitors are recommended.

Capacitor Values:

C1, C2 : Crystal load values determined by user
C3 : 100pF ceramic
All unmarked capacitors are 0.01μF ceramic

- = Ground Plane Connection
- = Power Plane Connection
- = Solder Pads

ICS9148-10



SSOP Package

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016	AD	.720	.725	.730	56
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	.006	.0085					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∞	0°	5°	8°					
X	.085	.093	.100					

This table in inches

Ordering Information

ICS9148yF-10

Example:

ICS XXXX y F - PPP

— Pattern Number (2 or 3 digit number for parts with ROM code patterns)

— Package Type

– **Revision Designator** (will not correlate with datasheet revision)

—Device Type (consists of 3 or 4 digit numbers)

— Prefix

ICS, AV = Standard Device