



Integrated  
Circuit  
Systems, Inc.

ICS9148-93

Advance Information

## Frequency Generator & Integrated Buffers for PENTIUM/Pro™

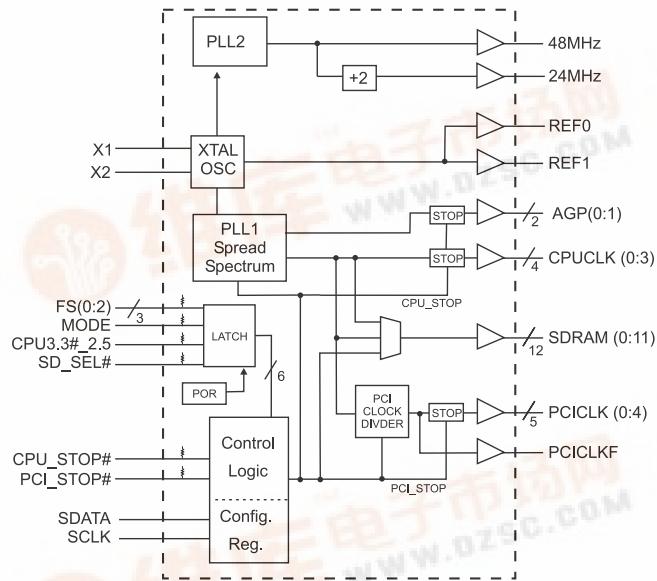
### General Description

The **ICS9148-93** is the single chip clock solution for Desktop/Notebook designs using the VIA MVP3 style chipset. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I<sup>2</sup>C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS9148-93** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I<sup>2</sup>C interface allows changing functions, stop clock programming and frequency selection. The SD\_SEL latched input allows the SDRAM frequency to follow the CPUCLK frequency (SD\_SEL=1) or the AGP clock frequency (SD\_SEL=0).

### Block Diagram



### Power Groups

VDD1 = REF (0:1), X1, X2

VDD2 = PCICLK\_F, PCICLK(0:5)

VDD3 = SDRAM (0:11), supply for PLL core,

24 MHz, 48MHz

VDD4 = AGP (0:1)

VDDL = CPUCLK(0:3)

### Features

- Generates the following system clocks:
  - 4 CPU(2.5V/3.3V) upto 100MHz.
  - 6 PCI(3.3V) @ 33.3MHz
  - 2 AGP(3.3V) @ 2x PCI
  - 12 SDRAMs(3.3V) @ either CPU or AGP
  - 2 REF (3.3V) @ 14.318MHz
- Skew characteristics:
  - CPU - CPU  $\leq$  250ps
  - SDRAM - SDRAM  $\leq$  250ps
  - CPU - SDRAM  $\leq$  250ps
  - CPU(early) - PCI : 1-4ns
- Supports Spread Spectrum modulation  $\pm 0.25, \pm 0.6\%$
- Serial I<sup>2</sup>C interface for Power Management, Frequency Select, Spread Spectrum.
- Efficient Power management scheme through PCI and CPU STOPCLOCKS.
- Uses external 14.318MHz crystal
- 48 pin 300mil SSOP.

### Pin Configuration

VDD1	1	VDD4
*REF0/CPU3.3#_2.5	2	47 AGP1
GND	3	46 REF1/SD_SEL*
X1	4	45 GND
X2	5	44 CPUCLK0
VDD2	6	43 CPUCLK1
*PCICLK_F/FS1	7	42 VDDL
*PCICLK0/FS2	8	41 CPUCLK2
GND	9	40 CPUCLK3
PCICLK1	10	39 GND
PCICLK2	11	38 SDRAM0
PCICLK3	12	37 SDRAM1
PCICLK4	13	36 VDD3
VDD2	14	35 SDRAM2
AGP0	15	34 SDRAM3
GND	16	33 GND
*CPU_STOP#/SDRAM11	17	32 SDRAM4
*PCI_STOP#/SDRAM10	18	31 SDRAM5
VDD3	19	30 VDD3
SDRAM9	20	29 SDRAM6
SDRAM8	21	28 SDRAM7
GND	22	27 GND
I <sup>2</sup> C { SDATA	23	26 48MHz/FS0*
SCLK	24	25 24 MHz/MODE*

### 48-Pin SSOP

\* Internal Pull-up Resistor of 240K to 3.3V on indicated inputs

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### Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VDD1	PWR	Ref (0:2), XTAL power supply, nominal 3.3V
2	REF0	OUT	14.318 MHz reference clock.
	CPU3.3#_2.5 <sup>1,2</sup>	IN	Indicates whether VDDL2 is 3.3V or 2.5V. High=2.5V CPU, LOW=3.3V CPU <sup>1</sup> . Latched input <sup>2</sup>
3,9,16,22,27, 33,39,45	GND	PWR	Ground
4	X1	IN	Crystal input, has internal load cap (33pF) and feedback resistor from X2
5	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (33pF)
6,14	VDD2	PWR	Supply for PCICLK_F and PCICLK (0:5), nominal 3.3V
7	PCICLK_F	OUT	Free running PCI clock output. Synchronous with CPUCLKs with 1-4ns skew (CPU early) This is not affected by PCI_STOP#
	FS1 <sup>1,2</sup>	IN	Frequency select pin. Latched Input. Along with other FS pins determines the CPU, SDRAM, PCI & AGP frequencies.
8	PCICLK0	OUT	PCI clock output. Synchronous CPUCLKs with 1-4ns skew (CPU early)
	FS2 <sup>1,2</sup>	IN	Frequency select pin. Latched Input. Along with other FS pins determines the CPU, SDRAM, PCI & AGP frequencies.
10, 11, 12, 13	PCICLK(1:4)	OUT	PCI clock outputs. Synchronous CPUCLKs with 1-4ns skew (CPU early)
15, 47	AGP (0:1)	OUT	Advanced Graphic Port outputs, powered by VDD4.
17	CPU_STOP# <sup>1</sup>	IN	This asynchronous input halts CPUCLK (0:3) and AGP (0:1) clocks at logic 0 level, when input low (in Mobile Mode, MODE=0)
	SDRAM 11	OUT	SDRAM clock output. Frequency is selected by the SD_SEL latched input. SD_SEL = 1 at power on causes SDRAM frequency = CPU frequency SD_SEL = 0 at power on causes SDRAM frequency = AGP frequency
18	PCI_STOP# <sup>1</sup>	IN	This asynchronous input halts PCICLK(0:5) clocks at logic 0 level, when input low (in mobile mode, MODE=0)
	SDRAM 10	OUT	SDRAM clock output. Frequency is selected by the SD_SEL latched input. SD_SEL = 1 at power on causes SDRAM frequency = CPU frequency SD_SEL = 0 at power on causes SDRAM frequency = AGP frequency
20, 21, 28, 29, 31, 32, 34, 35, 37, 38	SDRAM (0:9)	OUT	SDRAM clock outputs. Frequency is selected by the SD_SEL latched input. SD_SEL = 1 at power on causes SDRAM frequency = CPU frequency SD_SEL = 0 at power on causes SDRAM frequencies = AGP frequency
19,30,36	VDD3	PWR	Supply for SDRAM (0:11), CPU Core and 24, 48MHz clocks, nominal 3.3V.
23	SDATA	IN	Data input for I <sup>2</sup> C serial input.
24	SCLK	IN	Clock input of I <sup>2</sup> C input
25	24MHz	OUT	24MHz output clock, for Super I/O timing.
	MODE <sup>1,2</sup>	IN	Pin 17, pin 18 function select pin, 1=Desktop Mode, 0=Mobile Mode. Latched Input.
26	48MHz	OUT	48MHz output clock, for USB timing.
	FS0 <sup>1,2</sup>	IN	Frequency select pin. Latched Input. Along with other FS pins determines the CPU, SDRAM, PCI & AGP frequencies.
40, 41, 43, 44	CPUCLK(0:3)	OUT	CPU clock outputs, powered by VDDL2. Low if CPU_STOP#=Low
42	VDDL	PWR	Supply for CPU (0:3), either 2.5V or 3.3V nominal
46	REF1	OUT	14.318MHz reference clock.
	SD_SEL	IN	Latched input at Power On selects either CPU (SDSEL=1) or AGP (SD_SEL=0) frequencies for the SDRAM clock outputs.
48	VDD4	PWR	Supply for AGP (0:1)

#### Notes:

- 1: Internal Pull-up Resistor of 240K to 3.3V on indicated inputs
- 2: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.



## Mode Pin - Power Management Input Control

MODE, Pin 25 (Latched Input)	Pin 17	Pin 18
0	CPU_STOP# (INPUT)	PCI_STOP# (INPUT)
1	SDRAM 11 (OUTPUT)	SDRAM 10 (OUTPUT)

## Power Management Functionality

CPU_STOP#	PCI_STOP#	AGP, CPUCLK Outputs	PCICLK (0:5)	PCICLK_F, REF, 24/48MHz and SDRAM	Crystal OSC	VCO
0	1	Stopped Low	Running	Running	Running	Running
1	1	Running	Running	Running	Running	Running
1	0	Running	Stopped Low	Running	Running	Running

## CPU 3.3#\_2.5V Buffer selector for CPUCLK drivers.

CPU3.3#_2.5 Input level (Latched Data)	Buffer Selected for operation at:
1	2.5V VDD
0	3.3V VDD

## Functionality

$V_{DD1,2,3,4} = 3.3V \pm 5\%$ ,  $V_{DDL} = 2.5V \pm 5\%$  or  $3.3 \pm 5\%$ ,  $TA = 0$  to  $70^\circ C$   
Crystal (X1, X2) = 14.31818MHz

FS2	FS1	FS0	CPU (MHz) SDRAM (MHz)	PCI (MHz)	AGP (MHz)
0	0	0	90.00	30.00	60.00
0	0	1	66.82	33.41	66.82
0	1	0	68.49	34.25	68.49
0	1	1	75.00	37.5	75.00
1	0	0	75.00	30.00	60.00
1	0	1	83.31	33.32	66.64
1	1	0	95.25	31.75	63.50
1	1	1	100.00	33.33	66.66

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### General I<sup>2</sup>C serial interface information

The information in this section assumes familiarity with I<sup>2</sup>C programming. For more information, contact ICS for an I<sup>2</sup>C programming application note.

#### How to Write:

- Send the address D2<sub>(H)</sub>.
- Send two additional dummy bytes, a command code and byte count.
- Send the desired number of data bytes.

See the diagram below:

Clock Generator Address (7 bits)	ACK	+ 8 bits dummy command code	ACK	+ 8 bits dummy Byte count	ACK	Data Byte 1	ACK	Data Byte N	ACK
A(6:0) & R/W#									
D2(H)									

Note that the acknowledge bit is sent by the clock chip, and pulls the data line low. There is no minimum of data bytes that must be sent.

#### How to Read:

- Send the address D3<sub>(H)</sub>.
- Send the byte count in binary coded decimal
- Read back the desired number of data bytes

See the diagram below:

Clock Generator Address (7 bits)	ACK	Byte Count	ACK	Data Byte 1	ACK	Data Byte N
A(6:0) & R/W#						
D3(H)						

The following specifications should be observed:

- Operating voltage for I<sup>2</sup>C pins is 3.3V
- Maximum data transfer rate (SCLK) is 100K bits/sec.

**Note 1.** Default at Power-up will be for latched logic inputs, as defined by Bit 3.

### Serial Configuration Command Bitmap

**Byte0: Functionality and Frequency Select Register (default = 0)**

Bit	Description				PWD
Bit 7	0 - ±0.25% Spread Spectrum Modulation 1 - ±0.6% Spread Spectrum Modulation				0
Bit 6:4	Bit (6:4)	CPU SDRAM (MHz)	PCI (MHz)	AGP (MHz)	XXX Note 1
	000	90.00	30.00	60.00	
	001	66.82	33.41	66.82	
	010	68.49	34.25	68.49	
	011	75.00	37.50	75.00	
	100	75.00	30.00	60.00	
	101	83.31	33.32	66.64	
	110	95.25	31.75	63.50	
	111	100.00	33.33	66.66	
Bit 3	0 - Frequency is selected by hardware select, FS(0:2) pins only 1 - Select frequencies by I <sup>2</sup> C				0
	0 - Center Spread 1 - Down Spread				0
Bit 1	0 - Normal operation 1 - Spread Spectrum Enabled				0
Bit 0	0 - Running 1 - Tristate all outputs				0

**Byte 1: CPU Active/Inactive Register  
(1 = enable, 0 = disable)**

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	40	1	CPUCLK3 (Act/Inact)
Bit 2	41	1	CPUCLK2 (Act/Inact)
Bit 1	43	1	CPUCLK1 (Act/Inact)
Bit 0	44	1	CPUCLK0 (Act/Inact)

**Notes:**

1. Inactive means outputs are held LOW and are disabled from switching.

**Byte 3: SDRAM Active/Inactive Register  
(1 = enable, 0 = disable)**

Bit	Pin #	PWD	Description
Bit 7	28	1	SDRAM7 (Act/Inact)
Bit 6	29	1	SDRAM6 (Act/Inact)
Bit 5	31	1	SDRAM5 (Act/Inact)
Bit 4	32	1	SDRAM4 (Act/Inact)
Bit 3	34	1	SDRAM3 (Act/Inact)
Bit 2	35	1	SDRAM2 (Act/Inact)
Bit 1	37	1	SDRAM1 (Act/Inact)
Bit 0	38	1	SDRAM0 (Act/Inact)

**Notes:**

1. Inactive means outputs are held LOW and are disabled from switching.

**Byte 5: Peripheral Active/Inactive Register  
(1 = enable, 0 = disable)**

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	47	1	AGP1(Act/Inact)
Bit 3	-	1	(Reserved)
Bit 2	-	1	(Reserved)
Bit 1	46	1	REF1 (Act/Inact)
Bit 0	2	1	REF0 (Act/Inact)

**Notes:**

1. Inactive means outputs are held LOW and are disabled from switching.

**Byte 2: PCI Active/Inactive Register  
(1 = enable, 0 = disable)**

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	7	1	PCICLK_F (Act/Inact)
Bit 5	15	1	AGP0 (Act/Inact)
Bit 4	13	1	PCICLK4 (Act/Inact)
Bit 3	12	1	PCICLK3 (Act/Inact)
Bit 2	11	1	PCICLK2 (Act/Inact)
Bit 1	10	1	PCICLK1 (Act/Inact)
Bit 0	8	1	PCICLK0(Act/Inact)

**Notes:**

1. Inactive means outputs are held LOW and are disabled from switching.

**Byte 4: SDRAM Active/Inactive Register  
(1 = enable, 0 = disable)**

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	17	1	SDRAM11 (Act/Inact) (Desktop Mode Only)
Bit 2	18	1	SDRAM10 (Act/Inact) (Desktop Mode Only)
Bit 1	20	1	SDRAM9 (Act/Inact)
Bit 0	21	1	SDRAM8 (Act/Inact)

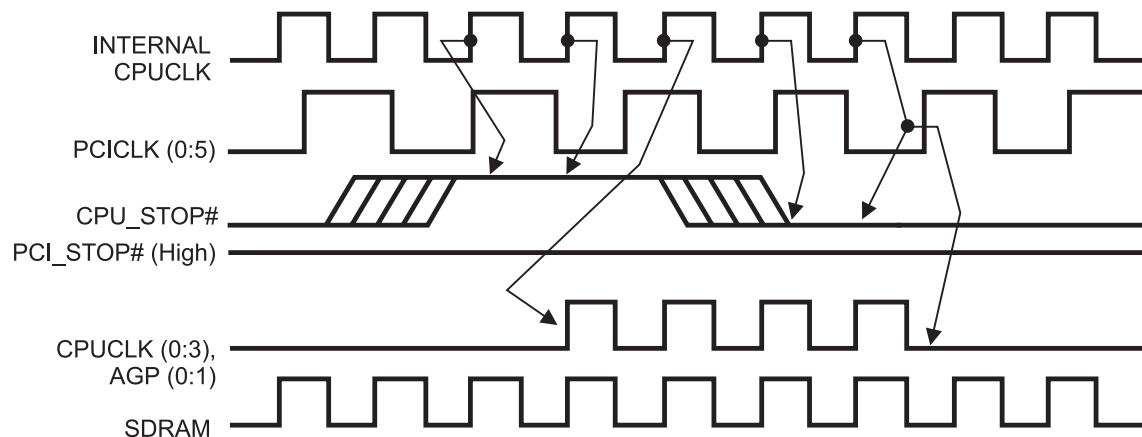
**Notes:**

1. Inactive means outputs are held LOW and are disabled from switching.



### CPU\_STOP# Timing Diagram

CPU\_STOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU\_STOP# is synchronized by the **ICS9148-93**. The minimum that the CPU clock is enabled (CPU\_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.



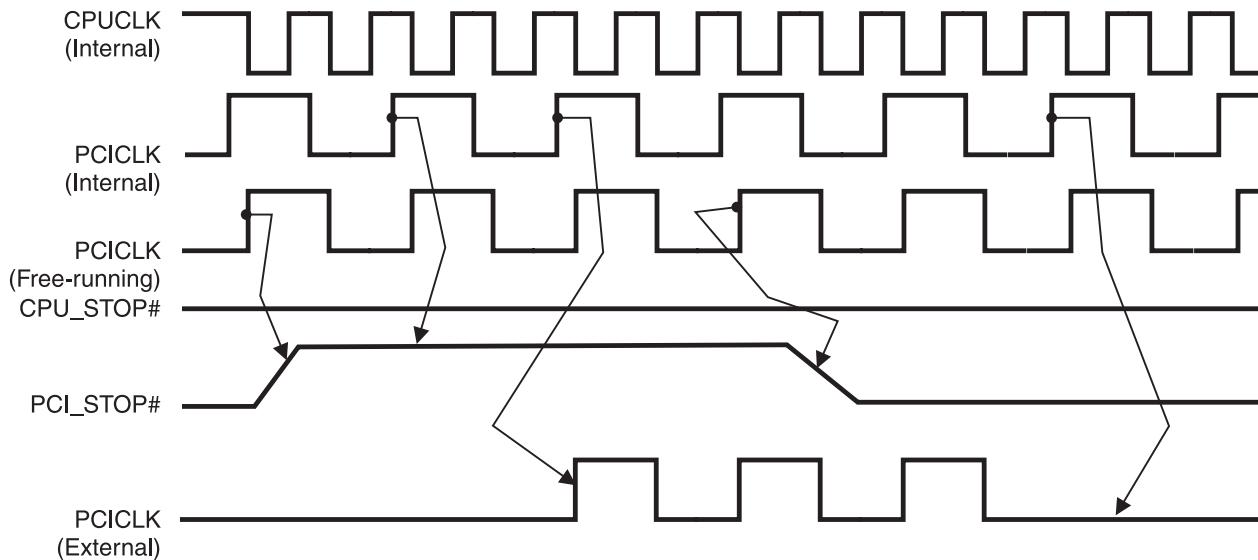
#### Notes:

1. All timing is referenced to the internal CPU clock.
2. CPU\_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9148-93.
3. All other clocks continue to run undisturbed. (including SDRAM outputs).



## PCI\_STOP# Timing Diagram

PCI\_STOP# is an asynchronous input to the **ICS9148-93**. It is used to turn off the PCICLK (0:5) clocks for low power operation. PCI\_STOP# is synchronized by the **ICS9148-93** internally. The minimum that the PCICLK (0:5) clocks are enabled (PCI\_STOP# high pulse) is at least 10 PCICLK (0:5) clocks. PCICLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:5) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



### Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9148 device.)
2. PCI\_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9148.
3. All other clocks continue to run undisturbed.
4. CPU\_STOP# is shown in a high (true) state.



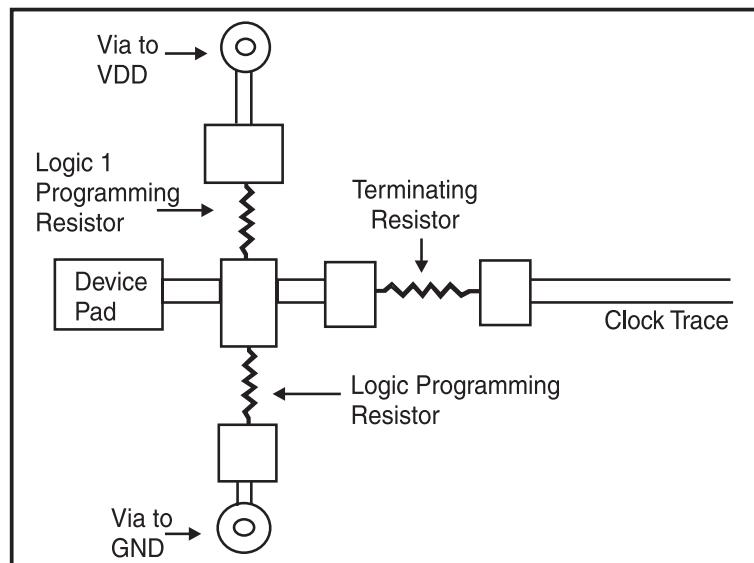
### Shared Pin Operation - Input/Output Pins

Pins 2, 7, 8, 25, 26 and 46 on the **ICS9148-93** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 4-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

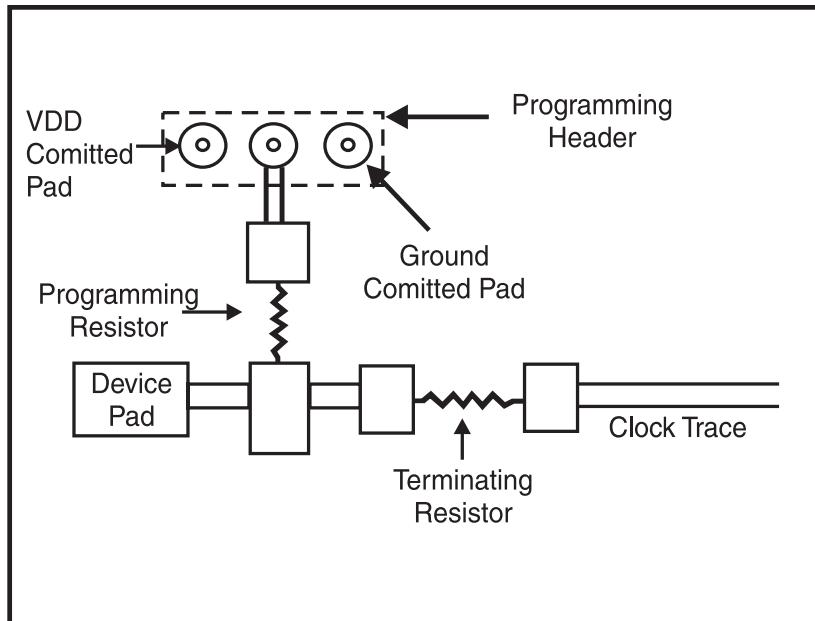
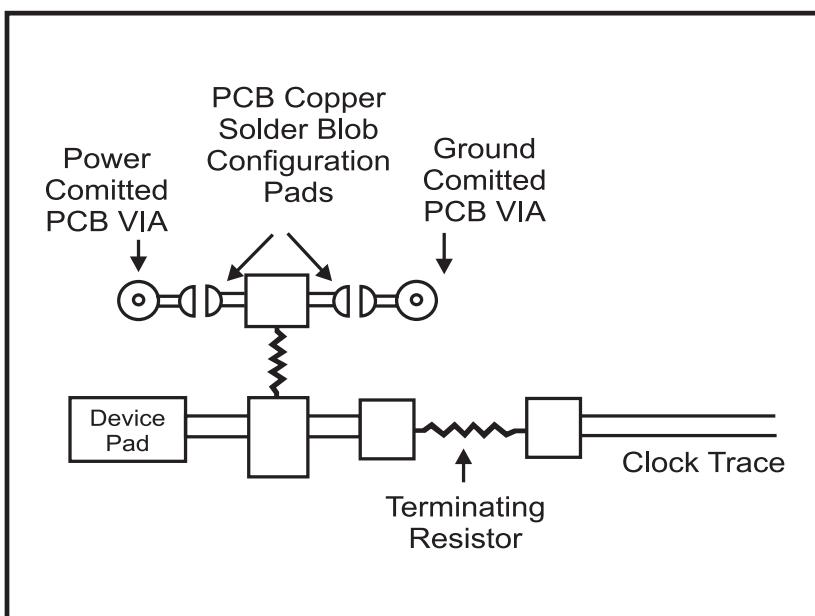
To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm(10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figs. 1 and 2 show the recommended means of implementing this function. In Fig. 1 either one of the resistors is loaded onto the board (selective stuffing) to configure the device's internal logic. Figs. 2a and b provide a single resistor loading option where either solder spot tabs or a physical jumper header may be used.

These figures illustrate the optimal PCB physical layout options. These configuration resistors are of such a large ohmic value that they do not effect the low impedance clock signals. The layouts have been optimized to provide as little impedance transition to the clock signal as possible, as it passes through the programming resistor pad(s).



**Fig. 1**

**Fig. 2a****Fig. 2b**

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### Absolute Maximum Ratings

Supply Voltage .....	7.0 V
Logic Inputs .....	GND -0.5 V to $V_{DD} + 0.5$ V
Ambient Operating Temperature .....	0°C to +70°C
Storage Temperature .....	-65°C to +150°C
Case Temperature .....	115°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ\text{C}$ ; Supply Voltage  $V_{DD} = V_{DDL} = 3.3$  V +/- 5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	$V_{IH}$		2		$V_{DD} + 0.3$	V
Input Low Voltage	$V_{IL}$		$V_{SS} - 0.3$		0.8	V
Input High Current	$I_{IH}$	$V_{IN} = V_{DD}$		0.1	5	mA
Input Low Current	$I_{IL1}$	$V_{IN} = 0$ V; Inputs with no pull-up resistors	-5	2.0		mA
Input Low Current	$I_{IL2}$	$V_{IN} = 0$ V; Inputs with pull-up resistors	-200	-100		mA
Operating Supply Current	$I_{DD3.3OP}$	$C_L = 0$ pF; 66.8 MHz		100	160	mA
Input frequency	$F_i$	$V_{DD} = 3.3$ V;		14.318		MHz
Input Capacitance <sup>1</sup>	$C_{IN}$	Logic Inputs			5	pF
	$C_{INX}$	X1 & X2 pins	27	36	45	pF
Transition Time <sup>1</sup>	$T_{trans}$	To 1st crossing of target Freq.			2	ms
Settling Time <sup>1</sup>	$T_s$	From 1st crossing to 1% target Freq.				ms
Clk Stabilization <sup>1</sup>	$T_{STAB}$	From $V_{DD} = 3.3$ V to 1% target Freq.			2	ms
Skew <sup>1</sup>	$T_{CPU-SDRAM1}$	$V_T = 1.5$ V; SDRAM Leads	-500	200	500	ps
	$T_{CPU-PCI1}$	$V_T = 1.5$ V; CPU Leads	1	2.8	4	ns

<sup>1</sup>Guaranteed by design, not 100% tested in production.

### Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ\text{C}$ ; Supply Voltage  $V_{DD} = 3.3$  V +/- 5%,  $V_{DDL} = 2.5$  V +/- 5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5OP}$	$C_L = 0$ pF; 66.8 MHz		10	20	mA
Skew <sup>1</sup>	$T_{CPU-SDRAM2}$	$V_T = 1.5$ V; $V_{TL} = 1.25$ V; SDRAM Leads	-500	200	500	ps
	$T_{CPU-PCI2}$	$V_T = 1.5$ V; $V_{TL} = 1.25$ V; CPU Leads	1	2.7	4	ns

<sup>1</sup>Guaranteed by design, not 100% tested in production.



## Electrical Characteristics - CPU

$T_A = 0 - 70^\circ C$ ;  $V_{DD} = 3.3 V \pm 5\%$ ;  $V_{DDL} = 2.5 V \pm 5\%$ ;  $C_L = 10 - 20 \text{ pF}$  (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	$V_{OH2B}$	$I_{OH} = -8 \text{ mA}$	2	2.2		V
Output Low Voltage	$V_{OL2B}$	$I_{OL} = 12 \text{ mA}$		0.3	0.4	V
Output High Current	$I_{OH2B}$	$V_{OH} = 1.7 V$		-20	-16	mA
Output Low Current	$I_{OL2B}$	$V_{OL} = 0.7 V$	19	26		mA
Rise Time	$t_{r2B}^1$	$V_{OL} = 0.4 V, V_{OH} = 2.0 V$		1.5	1.8	ns
Fall Time	$t_{f2B}^1$	$V_{OH} = 2.0 V, V_{OL} = 0.4 V$		1.6	1.8	ns
Duty Cycle	$d_{t2B}^1$	$V_T = 1.25 V$	40	47	55	%
Skew	$t_{sk2B}^1$	$V_T = 1.25 V$		60	250	ps
Jitter, Single Edge Displacement <sup>2</sup>	$t_{jsed2B}^1$	$V_T = 1.25 V$		200	250	ps
Jitter, One Sigma	$t_{j1s2B}^1$	$V_T = 1.25 V$		65	150	ps
Jitter, Absolute	$t_{jabs2B}^1$	$V_T = 1.25 V$	-300	160	300	ps

<sup>1</sup> Guaranteed by design, not 100% tested in production.

<sup>2</sup> Edge displacement of a period relative to a 10-clock-cycle rolling average period.

## Electrical Characteristics - CPU

$T_A = 0 - 70^\circ C$ ;  $V_{DD} = V_{DDL} = 3.3 V \pm 5\%$ ;  $C_L = 10 - 20 \text{ pF}$  (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	$V_{OH2A}$	$I_{OH} = -28 \text{ mA}$	2.5	2.6		V
Output Low Voltage	$V_{OL2A}$	$I_{OL} = 27 \text{ mA}$		0.35	0.4	V
Output High Current	$I_{OH2A}$	$V_{OH} = 2.0 V$		-29	-23	mA
Output Low Current	$I_{OL2A}$	$V_{OL} = 0.8 V$	33	37		mA
Rise Time	$t_{r2A}^1$	$V_{OL} = 0.4 V, V_{OH} = 2.4 V$		1.75	2	ns
Fall Time	$t_{f2A}^1$	$V_{OH} = 2.4 V, V_{OL} = 0.4 V$		1.1	2	ns
Duty Cycle	$d_{t2A}^1$	$V_T = 1.5 V$	45	50	55	%
Skew	$t_{sk2A}^1$	$V_T = 1.5 V$		50	250	ps
Jitter, One Sigma	$t_{j1s2A}^1$	$V_T = 1.5 V$		65	150	ps
Jitter, Absolute	$t_{jabs2A}^1$	$V_T = 1.5 V$	-250	165	250	ps

<sup>1</sup> Guaranteed by design, not 100% tested in production.

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### Electrical Characteristics - SDRAM

$T_A = 0 - 70^\circ C$ ;  $V_{DD} = V_{DDL} = 3.3 V \pm 5\%$ ;  $C_L = 30 pF$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	$V_{OHI}$	$I_{OH} = -28 mA$	2.4	3		V
Output Low Voltage	$V_{OLI}$	$I_{OL} = 23 mA$		0.2	0.4	V
Output High Current	$I_{OHI}$	$V_{OH} = 2.0 V$		-60	-40	mA
Output Low Current	$I_{OLI}$	$V_{OL} = 0.8 V$	41	50		mA
Rise Time <sup>1</sup>	$t_{r1}$	$V_{OL} = 0.4 V, V_{OH} = 2.4 V$		1.75	2	ns
Fall Time <sup>1</sup>	$t_{f1}$	$V_{OH} = 2.4 V, V_{OL} = 0.4 V$		1.5	2	ns
Duty Cycle <sup>1</sup>	$D_{t1}$	$V_T = 1.5 V$	45	50	55	%
Skew <sup>1</sup>	$t_{sk1}$	$V_T = 1.5 V$		200	500	ps
Jitter, One Sigma <sup>1</sup>	$t_{j1s1}$	$V_T = 1.5 V$		50	150	ps
Jitter, Absolute <sup>1</sup>	$t_{jabs1}$	$V_T = 1.5 V$ (with synchronous PCI)	-250		+250	ps
Jitter, Absolute <sup>1</sup>	$t_{jabs1}$	$V_T = 1.5 V$ (with asynchronous PCI)	-400		400	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.

### Electrical Characteristics - PCI

$T_A = 0 - 70^\circ C$ ;  $V_{DD} = V_{DDL} = 3.3 V \pm 5\%$ ;  $C_L = 30 pF$  (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	$V_{OHI}$	$I_{OH} = -28 mA$	2.4	3		V
Output Low Voltage	$V_{OLI}$	$I_{OL} = 23 mA$		0.2	0.4	V
Output High Current	$I_{OHI}$	$V_{OH} = 2.0 V$		-60	-40	mA
Output Low Current	$I_{OLI}$	$V_{OL} = 0.8 V$	41	50		mA
Rise Time	$t_{r1}^1$	$V_{OL} = 0.4 V, V_{OH} = 2.4 V$		1.8	2	ns
Fall Time	$t_{f1}^1$	$V_{OH} = 2.4 V, V_{OL} = 0.4 V$		1.6	2	ns
Duty Cycle	$d_{t1}^1$	$V_T = 1.5 V$	45	51	55	%
Skew	$t_{sk1}^1$	$V_T = 1.5 V$		130	250	ps
Jitter, One Sigma <sup>1</sup>	$t_{j1s1a}$	$V_T = 1.5 V$ , synchronous		40	150	ps
	$t_{j1s1b}$	$V_T = 1.5 V$ , asynchronous		200	250	ps
Jitter, Absolute <sup>1</sup>	$t_{abs1a}$	$V_T = 1.5 V$ , synchronous	-250	135	250	ps
	$t_{abs1b}$	$V_T = 1.5 V$ , asynchronous	-650	500	650	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.



## Electrical Characteristics - AGP

$T_A = 0 - 70^\circ C$ ;  $V_{DD} = V_{DDL} = 3.3 V \pm 5\%$ ;  $C_L = 30 pF$  (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	$V_{OH1}$	$I_{OH} = -28 mA$	2.4	3		V
Output Low Voltage	$V_{OL1}$	$I_{OL} = 23 mA$		0.2	0.4	V
Output High Current	$I_{OH1}$	$V_{OH} = 2.0 V$		-60	-40	mA
Output Low Current	$I_{OL1}$	$V_{OL} = 0.8 V$	41	50		mA
Rise Time	$t_{rl}^1$	$V_{OL} = 0.4 V, V_{OH} = 2.4 V$		1.1	2	ns
Fall Time	$t_{fl}^1$	$V_{OH} = 2.4 V, V_{OL} = 0.4 V$		1	2	ns
Duty Cycle	$d_{tl}^1$	$V_T = 1.4 V$	45	49	55	%
Skew	$t_{sk1}^1$	$V_T = 1.5 V$		130	250	ps
Jitter, One Sigma <sup>1</sup>	$t_{j1s1}$	$V_T = 1.5 V$		2	3	%
Jitter, Absolute <sup>1</sup>	$t_{abs1a}$	$V_T = 1.5 V$ , synchronous	-5	2.5	5	%
	$t_{abs1b}$	$V_T = 1.5 V$ , asynchronous	-6	4.5	6	%

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - 24MHz, 48MHz, REF0

$T_A = 0 - 70^\circ C$ ;  $V_{DD} = V_{DDL} = 3.3 V \pm 5\%$ ;  $C_L = 10 - 20 pF$  (unless otherwise stated)

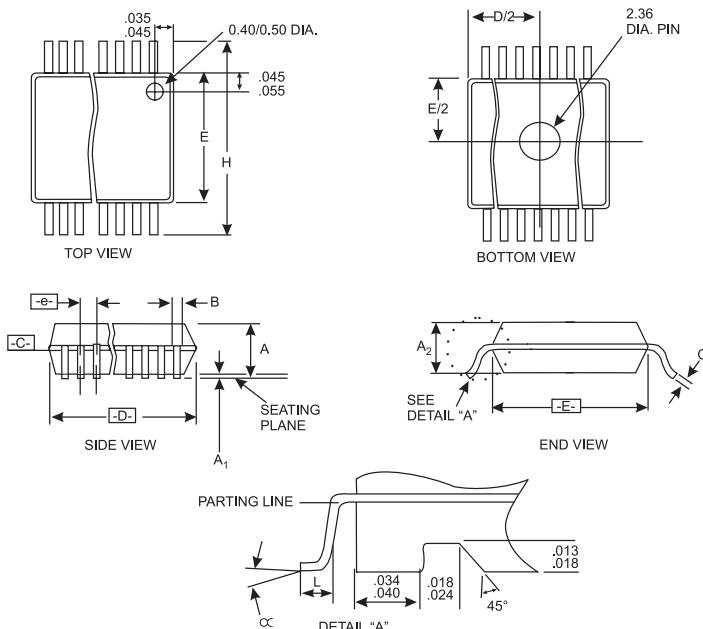
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	$V_{OH5}$	$I_{OH} = -16 mA$	2.4	2.6		V
Output Low Voltage	$V_{OL5}$	$I_{OL} = 9 mA$		0.3	0.4	V
Output High Current	$I_{OH5}$	$V_{OH} = 2.0 V$		-32	-22	mA
Output Low Current	$I_{OL5}$	$V_{OL} = 0.8 V$	16	25		mA
Rise Time	$t_{rl}^1$	$V_{OL} = 0.4 V, V_{OH} = 2.4 V$		2	4	ns
Fall Time	$t_{fl}^1$	$V_{OH} = 2.4 V, V_{OL} = 0.4 V$		1.9	4	ns
Duty Cycle	$d_{tl}^1$	$V_T = 1.5 V$	45	54	57	%
Jitter, One Sigma	$t_{j1s5}^1$	$V_T = 1.5 V$		1	3	%
Jitter, Absolute	$t_{abs5}^1$	$V_T = 1.5 V$	-5	-	5	%

<sup>1</sup>Guaranteed by design, not 100% tested in production.

# ICS9148-93



## Advance Information



## SSOP Package

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016					
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	-	.010					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
$\infty$	$0^\circ$	$5^\circ$	$8^\circ$					
X	.085	.093	.100					

## Ordering Information

### ICS9148F-37

Example:

**ICS XXXX F - PPP**

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type  
F=SSOP

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS, AV = Standard Device