HIGH SPEED 32K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  - — t_{ACC} = 35 ns
  - — t_{CE} = 35 ns
- **Low Power Consumption**
  - — 200 µA Standby I_{CC}
- **Immune to Latch-UP**
  - — Up to 200 mA
- **ESD Protection Exceeds 2000 Volts**
- **Available in 300 Mil DIP and PLDCC**
- **DESC SMD No. 5962-86063**

GENERAL DESCRIPTION

The WS57C256F is a High Performance 32K x 8 UV Erasable EPROM. It is manufactured using an advanced CMOS process technology enabling it to operate at speeds as fast as 35 ns Address Access Time (t_{ACC}) and 35 ns Chip Enable Time (t_{CE}). It was designed utilizing WSI's patented self-aligned split gate EPROM cell, resulting in a low power device with a very cost effective die size. The low standby power capability of this 256 K product (200 µA in a CMOS interface environment) is especially attractive.

This product, with its high speed capability, is particularly appropriate for use with today's fast DSP processors and high-clock-rate Microprocessors. The WS57C256F's 35 ns speed enables these advanced processors to operate without introducing any undesirable wait states. The WS57C256F is also ideal for use in modem applications, and is recommended for use in these applications by the leading modem chip set manufacturer.

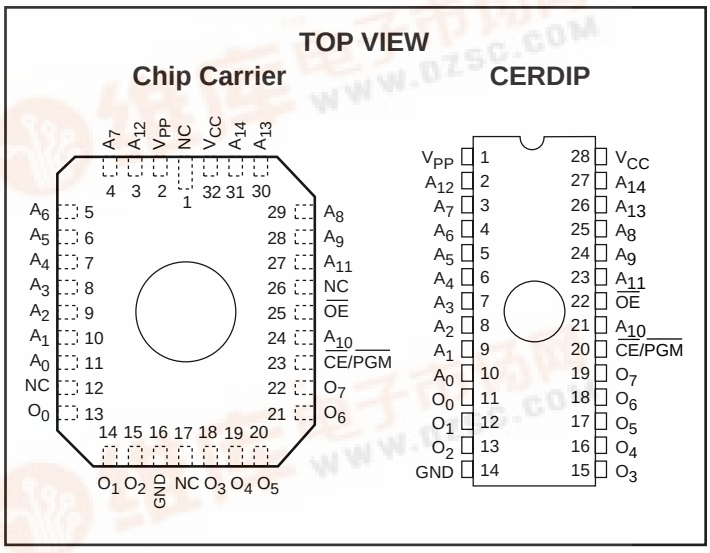
The WS57C256F is available in a variety of package types including the space saving 300 Mil DIP, the surface mount PLDCC, and other windowed and non-windowed options. And its standard JEDEC EPROM pinouts provide for automatic upgrade density paths for current 64K and 128K EPROM users.

MODE SELECTION

PINS / MODE	$\overline{CE}$/$\overline{PGM}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	X	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	X	X	V_{PP}[2]	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	X	X	V_{PP}[2]	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	X	X	V_{PP}[2]	V_{CC}	High Z
Signature[3]	V_{IL}	V_{IL}	V_H[2]	V_{IL}	V_{CC}	V_{CC}	23 H[4]
	V_{IL}	V_{IL}	V_H[2]	V_{IH}	V_{CC}	V_{CC}	EO H[5]

NOTES:
1. X can be V_{IL} or V_{IH}.
2. V_{IH} = V_{PP} = 12.75 ± 0.25 V.
3. A1 – A8, A10 – A14 = V_{IL}.
4. Manufacturer Signature.
5. Device Signature.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C256F-35	WS57C256F-45	WS57C256F-55	WS57C256F-70
Address Access Time (Max)	35 ns	45 ns	55 ns	70 ns
Output Enable Time (Max)	15 ns	20 ns	25 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature.....–65° to + 150°C

Voltage on any Pin with
Respect to Ground .....–0.6V to +7V

V_{PP} and A_9 with Respect to Ground .....–0.6V to + 14V

ESD Protection.....>2000V

***NOTICE:**
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 10%
Industrial	–40°C to +85°C	+5V ± 10%
Military	–55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

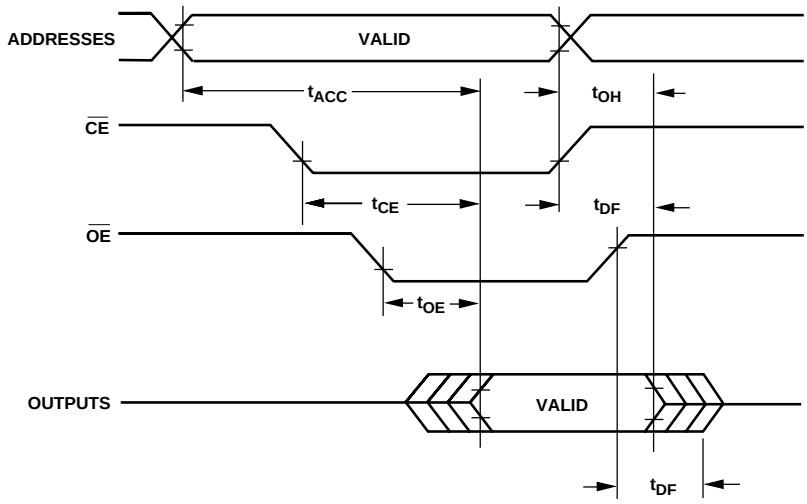
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 4)		–0.1	0.8	V
V_{IH}	Input High Voltage	(Note 4)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4 mA		2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3$ V (Note 1)	Comm'l		200	µA
			Ind/Mil		500	µA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE} = V_{IH}$ (Note 2)	Comm'l		3	mA
			Ind/Mil		5	mA
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3) Outputs Not Loaded	Comm'l		25	mA
			Ind/Mil		30	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3) Outputs Not Loaded	Comm'l		50	mA
			Ind/Mil		60	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} –0.4	V_{CC}	V
I_{LI}	Input Leakage Current	V_{IN} = 5.5V or Gnd		–10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		–10	10	µA

NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \le 0.8V$, $V_{IH} \ge 2.0V$.
3. Add 3 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range. with $V_{PP} = V_{CC}$

PARAMETER	SYMBOL	57C256F-35		57C256F-45		57C256F-55		57C256F-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55		70	ns
$\overline{CE}$ to Output Delay	t_{CE}		35		45		55		70	
$\overline{OE}$ to Output Delay	t_{OE}		15		20		25		30	
Output Disable to Output Float	t_{DF}		20		20		25		30	
Address to Output Hold	t_{OH}	0		0		0		0		

AC READ TIMING DIAGRAM

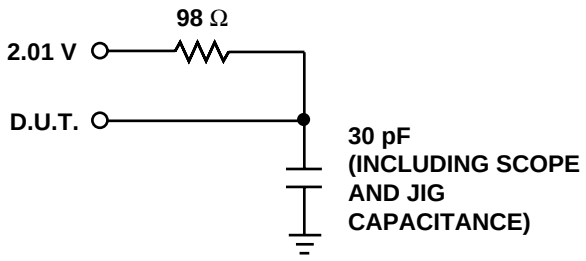


CAPACITANCE(5) T_A = 25°C, f = 1 MHz

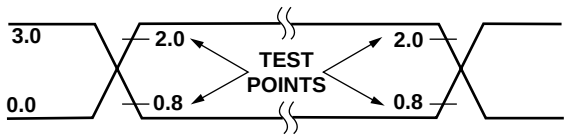
SYMBOL	PARAMETER	CONDITIONS	TYP(6)	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0 V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0." Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 0.1 microfarad capacitor in parallel with a 0.01 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 ± 0.25 V)

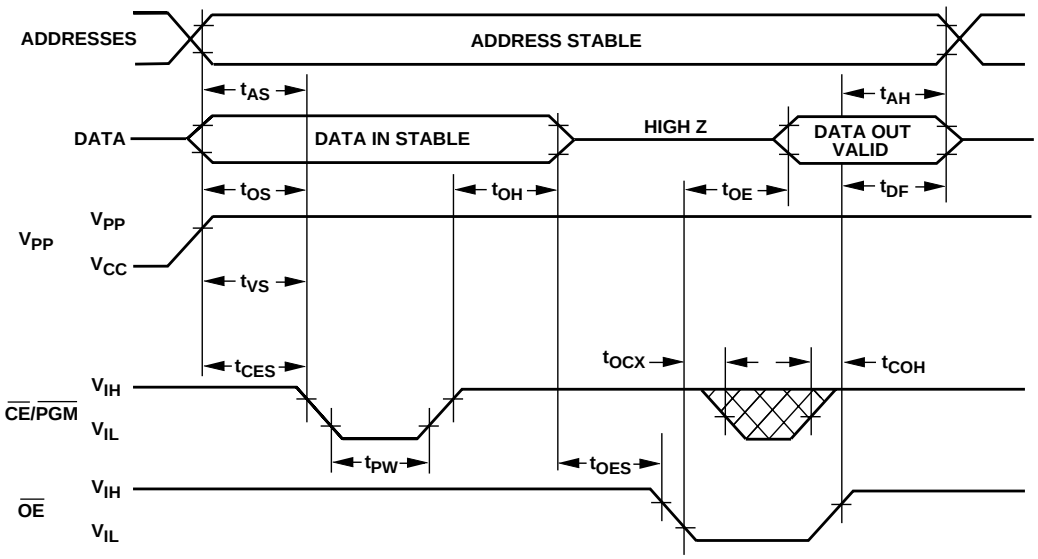
SYMBOLS	PARAMETER	MIN	MAX	UNITS
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse ($\overline{CE}/\overline{PGM}$ = V_{IL})		60	mA
I_{CC}	V_{CC} Supply Current (Note 8)		35	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.4	V
V_{OH}	Output High Voltage During Verify (I_{OH} = –4 mA)	2.4		V

NOTE:
8. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
9. V_{PP} must not be greater than 13 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
10. During power up the $\overline{PGM}$ pin must be brought high (≥ V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 ± 0.25 V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{COH}	CE High to OE High	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{OS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{OH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		130	ns
t_{OE}	Data Valid From Output Enable			130	ns
t_{VS}/t_{CES}	V_{PP} Setup Time/CE Setup Time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	100		200	µs
t_{OCX}	$\overline{OE}$ Low to $\overline{CE}$ "Don't Care"	2			µs

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C256F-35C	35	32 Pad CLLCC	C2	Comm'l	Standard
WS57C256F-35D	35	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C256F-35J	35	32 Pin PLDCC	J4	Comm'l	Standard
WS57C256F-35L	35	32 Pin CLDCC	L3	Comm'l	Standard
WS57C256F-35P	35	28 Pin Plastic DIP, 0.6"	P3	Comm'l	Standard
WS57C256F-35T	35	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C256F-45C	45	32 Pad CLLCC	C2	Comm'l	Standard
WS57C256F-45D	45	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C256F-45P	45	28 Pin Plastic DIP, 0.6"	P3	Comm'l	Standard
WS57C256F-45T	45	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C256F-55C	55	32 Pad CLLCC	C2	Comm'l	Standard
WS57C256F-55CMB	55	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C256F-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C256F-55DM	55	28 Pin CERDIP, 0.6"	D2	Military	Standard
WS57C256F-55DMB	55	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C256F-55J	55	32 Pin PLDCC	J4	Comm'l	Standard
WS57C256F-55L	55	32 Pin CLDCC	L3	Comm'l	Standard
WS57C256F-55P	55	28 Pin Plastic DIP, 0.6"	P3	Comm'l	Standard
WS57C256F-55T	55	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C256F-55TMB	55	28 Pin CERDIP, 0.3"	T2	Military	MIL-STD-883C
WS57C256F-70CMB*	70	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C256F-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C256F-70DMB*	70	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C256F-70J	70	32 Pin PLDCC	J4	Comm'l	Standard
WS57C256F-70JI	70	32 Pin PLDCC	J4	Industrial	Standard
WS57C256F-70T	70	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard

NOTE: 11. The actual part marking will not include the initials "WS."

*SMD product. See section 4 for DESC SMD number.

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS57C256F is programmed using Algorithm D shown on page 5-9.
When using Data I/O programmers, algorithm 57C256FB is recommended for use with the WS57C256F for best programming results.