



MOS INTEGRATED CIRCUIT
μPD4443362

4M-BIT CMOS SYNCHRONOUS FAST STATIC RAM
128K-WORD BY 36-BIT
HSTL INTERFACE / REGISTER-REGISTER / LATE WRITE

Description

The μPD4443362 is a 131,072 words by 36 bits synchronous static RAM fabricated with advanced CMOS technology using Full-CMOS six-transistor memory cell.

The μPD4443362 is suitable for applications which require synchronous operation, high-speed, low voltage, high-density memory and wide bit configuration, such as cache and buffer memory.

The μPD4443362 is packaged in 100-pin plastic LQFP with a 1.4 mm package thickness for high density and low capacitive loading.

Features

- Fully synchronous operation
- HSTL Input / Output levels
- ★ • Fast clock access time : 3.8 ns (133 MHz)
- Asynchronous output enable control : /G
- Byte write control : /SBa (DQa1-9), /SBb (DQb1-9), /SBc (DQc1-9), /SBd (DQd1-9)
- Common I/O using three-state outputs
- Internally self-timed write cycle
- Late write with 1 dead cycle between Read-Write
- 3.3 V (Chip) / 1.5 V (I/O) supply
- 100-pin plastic LQFP package, 14 mm x 20 mm
- Sleep Mode : ZZ (Enables sleep mode, active high)

★ **Ordering Information**

| Part number | Access time | Clock frequency | Package |
|------------------|-------------|-----------------|--------------------------------|
| μPD4443362GF-A75 | 3.8 ns | 133 MHz | 100-PIN PLASTIC LQFP (14 x 20) |

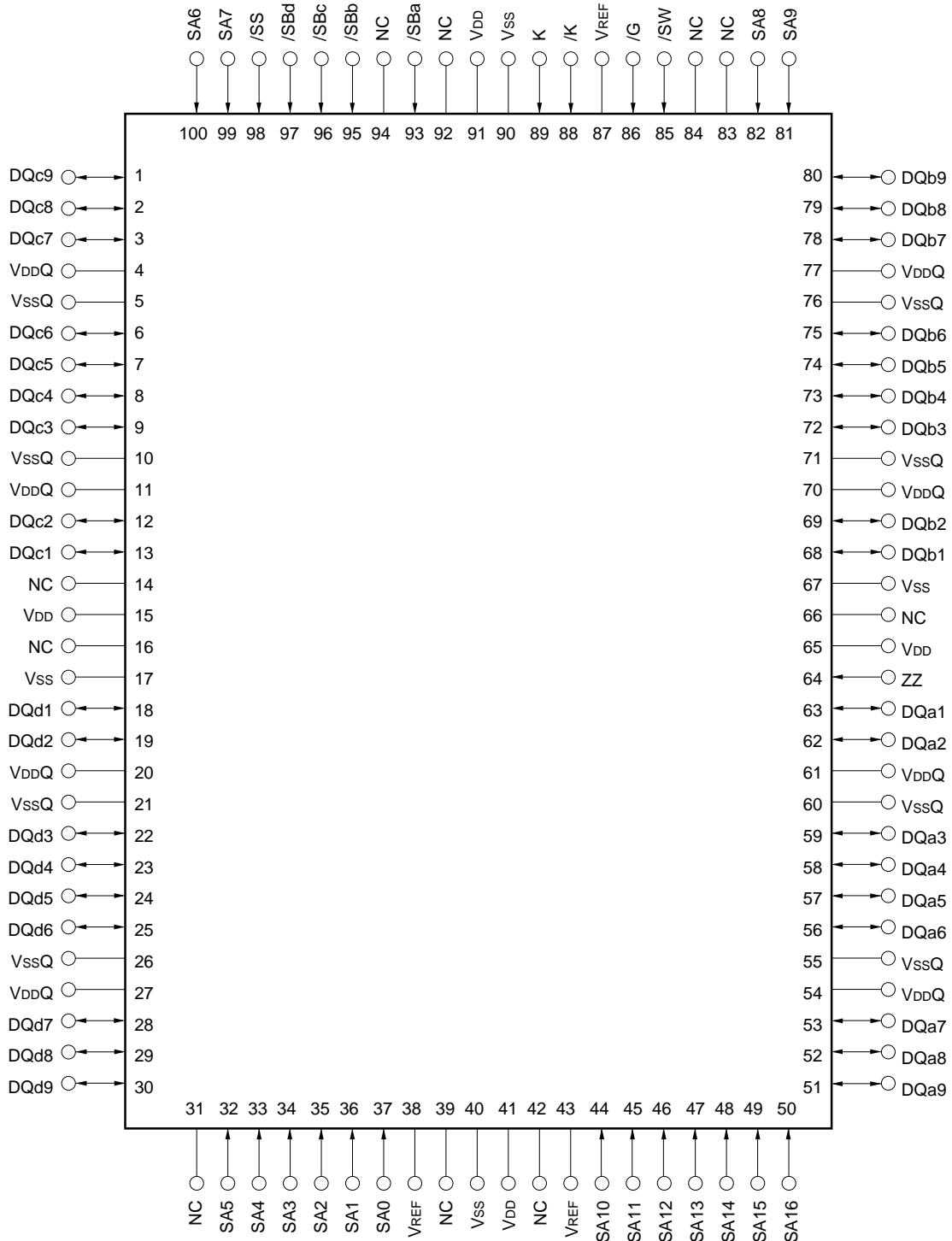
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Pin Configuration (Marking Side)

/xxx indicates active low signal.

100-PIN PLASTIC LQFP (14 x 20)

[μPD4443362GF]



Remark Refer to Package Drawing for 1-pin index mark.

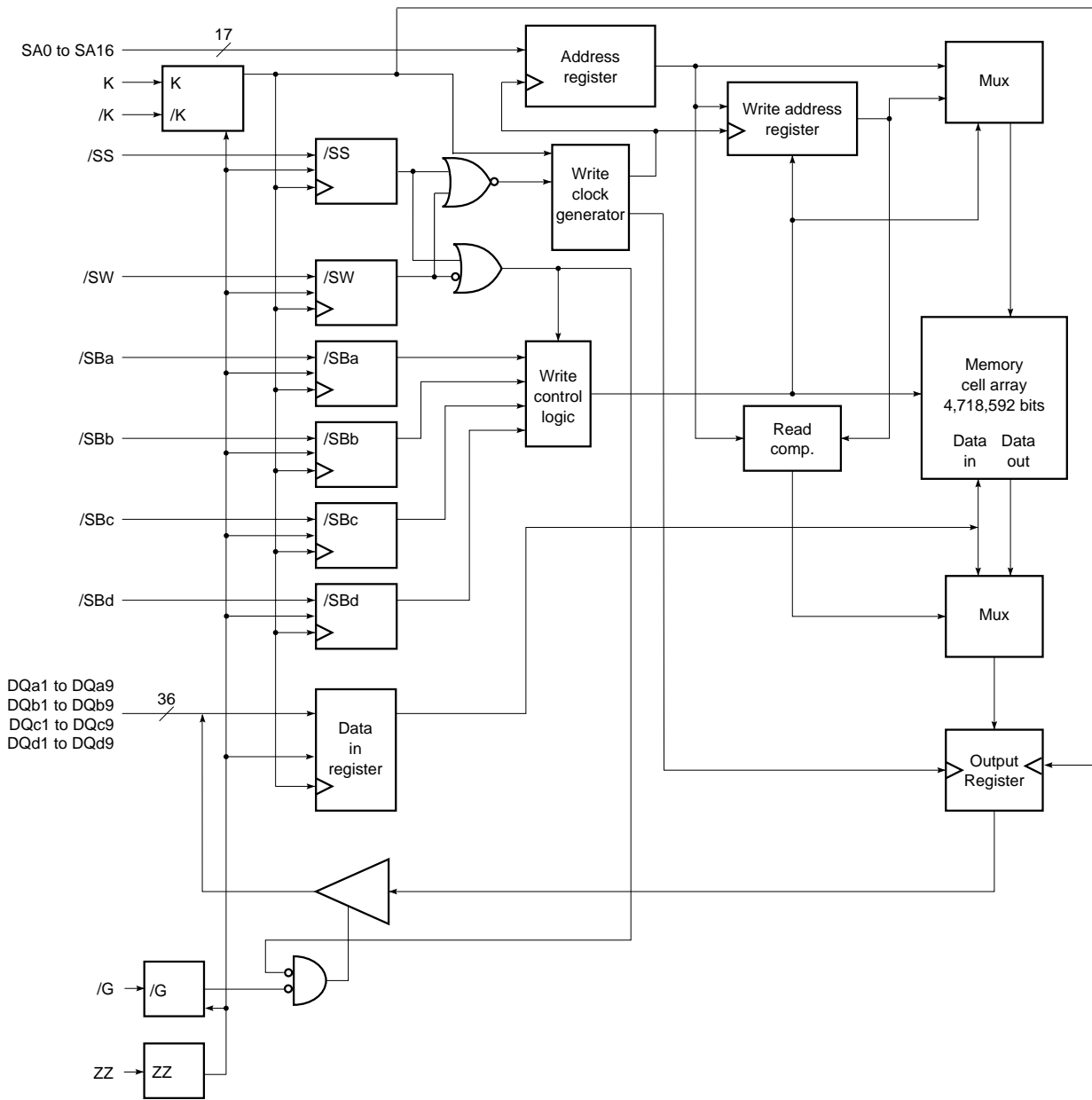
Pin Name and Functions

| Pin name | Pin No. | Description |
|-----------------------|---|-----------------------------------|
| SA0 to SA16 | 37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50 | Synchronous Address Input |
| DQa1 to DQa9 | 63, 62, 59, 58, 57, 56, 53, 52, 51 | Synchronous Data Input / Output |
| DQb1 to DQb9 | 68, 69, 72, 73, 74, 75, 78, 79, 80 | |
| DQc1 to DQc9 | 13, 12, 9, 8, 7, 6, 3, 2, 1 | |
| DQd1 to DQd9 | 18, 19, 22, 23, 24, 25, 28, 29, 30 | |
| /SS | 98 | Synchronous Chip Select |
| /SW | 85 | Synchronous Byte Write Enable |
| /SBa ^{Note1} | 93 | Synchronous Byte "a" Write Enable |
| /SBb ^{Note1} | 95 | Synchronous Byte "b" Write Enable |
| /SBc ^{Note1} | 96 | Synchronous Byte "c" Write Enable |
| /SBd ^{Note1} | 97 | Synchronous Byte "d" Write Enable |
| /G | 86 | Asynchronous Output Enable |
| ZZ ^{Note2} | 64 | Asynchronous Sleep Mode |
| K, /K | 89, 88 | Main Clock Input |
| VDD | 15, 41, 65, 91 | Core Power Supply |
| VSS | 17, 40, 67, 90 | Ground |
| VDDQ | 4, 11, 20, 27, 54, 61, 70, 77 | Output Buffer Power Supply |
| VSSQ | 5, 10, 21, 26, 55, 60, 71, 76 | Output Buffer Ground |
| VREF | 38, 43, 87 | Input Reference |
| NC | 14, 16, 31, 39, 42, 66, 83, 84, 92, 94 | No Connection |

- Notes**
1. If Byte Write Operation is not used, Byte Write Pins (/SBa, /SBb, /SBc, /SBd) are to be tied to Vss.
 2. If Sleep Mode is not used, ZZ Pin is to be tied to Vss.

Remark This device only supports Single Differential Clock, R / R Mode.
 (R / R stands for Registered Input / Registered Output.)

Late Write Block Diagram



Synchronous Truth Table

| ZZ | /SS | /SW | /SBa | /SBb | /SBc | /SBd | Mode | DQa1-9 | DQb1-9 | DQc1-9 | DQd1-9 | Power |
|----|-----|-----|------|------|------|------|--------------|--------|--------|--------|--------|---------|
| L | H | × | × | × | × | × | Not selected | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Active |
| L | L | H | × | × | × | × | Read | Dout | Dout | Dout | Dout | Active |
| L | L | L | L | L | L | L | Write | Din | Din | Din | Din | Active |
| L | L | L | L | H | H | H | Write | Din | Hi-Z | Hi-Z | Hi-Z | Active |
| L | L | L | H | L | L | L | Write | Hi-Z | Din | Din | Din | Active |
| L | L | L | H | H | H | H | Abort Write | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Active |
| H | × | × | × | × | × | × | Sleep Mode | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Standby |

Remark × : Don't care

Output Enable Truth Table

| Mode | /G | DQ |
|------------------|----|-----------|
| Read | L | Dout |
| Read | H | Hi-Z |
| Sleep (ZZ=H) | × | Hi-Z |
| Write (/SW=L) | × | Hi-Z, Din |
| Deselect (/SS=H) | × | Hi-Z |

★

Remark × : Don't care

Electrical Specifications

Absolute Maximum Ratings

| | Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit | Note |
|---|------------------------|------------------|-----------|------|------|-----------------------|------|------|
| ★ | Supply voltage | V _{DD} | | -0.5 | | +4.0 | V | 1 |
| ★ | Output supply voltage | V _{DDQ} | | -0.5 | | +4.0 | V | 1 |
| | Input voltage | V _{IN} | | -0.5 | | V _{DD} +0.3 | V | 1 |
| | Input / Output voltage | V _{I/O} | | -0.5 | | V _{DDQ} +0.3 | V | 1 |
| ★ | Operating temperature | T _A | | 0 | | 50 | °C | |
| | Storage temperature | T _{stg} | | -55 | | +125 | °C | |

Note 1. -2.0 V MIN. (Pulse width : 2 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

★ **Recommended DC Operating Conditions (T_A = 0 to 50 °C)**

| | Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|------------------------------|------------------|------------|-----------------------|------|-----------------------|------|
| | Core supply voltage | V _{DD} | | 3.135 | 3.3 | 3.465 | V |
| | Output buffer supply voltage | V _{DDQ} | | 1.4 | 1.5 | 1.6 | V |
| | Input reference voltage | V _{REF} | | 0.7 | 0.75 | 0.8 | V |
| | Low level input voltage | V _{IL} | | -0.3 ^{Note} | | V _{REF} -0.1 | V |
| | High level input voltage | V _{IH} | | V _{REF} +0.1 | | V _{DDQ} +0.3 | V |

Note -0.8 V MIN. (Pulse width : 2 ns)

★ **Recommended AC Operating Conditions (T_A = 0 to 50 °C)**

| | Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|--------------------------|------------------------|------------|-----------------------|------|-----------------------|------|
| | Input reference voltage | V _{REF (RMS)} | | -5% | | +5% | V |
| | Low level input voltage | V _{IL} | | -0.3 | | V _{REF} -0.2 | V |
| | High level input voltage | V _{IH} | | V _{REF} +0.2 | | V _{DDQ} +0.3 | V |

Capacitance (T_A = 25 °C, f = 1 MHz)

| | Parameter ^{Note} | Symbol | Test conditions | MAX. | Unit |
|---|----------------------------|------------------|------------------------|------|------|
| ★ | Input capacitance | C _{IN} | V _{IN} = 0 V | 5.5 | pF |
| | Input / Output capacitance | C _{I/O} | V _{I/O} = 0 V | 7.0 | pF |
| | Clock Input Capacitance | C _{clk} | V _{clk} = 0 V | 6.0 | pF |

Note These parameters are not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------------|-------------------|---|------|------|------|------|
| Input leakage current | I _{LI} | V _{IN} = 0 to V _{DD} | -5 | | +5 | μA |
| DQ leakage current | I _{LO} | V _{I/O} = 0 to V _{DDQ} | -5 | | +5 | μA |
| ★ Operating supply current | I _{DD} | V _{IN} = V _{IH} or V _{IL} , /SS = V _{IL} , ZZ = V _{IL} , Cycle = MAX., I _{DQ} = 0 mA | | | 350 | mA |
| ★ Sleep mode power supply current | I _{SBZZ} | ZZ = V _{IH} , All other inputs = V _{IH} or V _{IL} , Cycle = DC, I _{DQ} = 0 mA | | | 20 | mA |

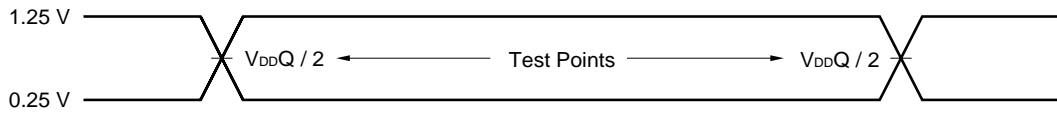
Output Voltage on Push-Pull Output Buffer Mode

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------------------|-----------------|-------------------------|-----------------------|------|------|------|
| Low level output voltage | V _{OL} | I _{OL} = +2 mA | - | | 0.3 | V |
| High level output voltage | V _{OH} | I _{OH} = -2 mA | V _{DDQ} -0.3 | | - | V |

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

AC Characteristics Test Conditions

- ★ Input waveform (rise and fall time = 0.5 ns (20 to 80%))



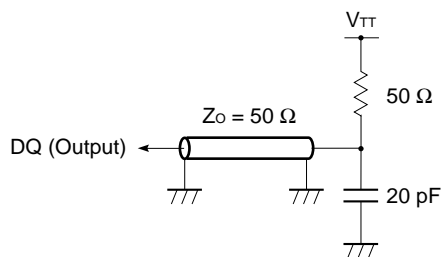
Output waveform



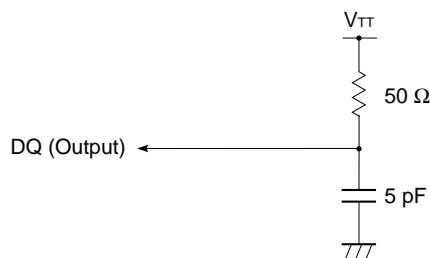
★ Single Differential Clock, Registered Input / Registered Output Mode

| Parameter | | Symbol | -A75 (133 MHz) | | Unit | Notes |
|------------------------|--------------|--|----------------|------|------|-------|
| | | | MIN. | MAX. | | |
| Clock cycle time | | t _{KHKH} | 7.5 | – | ns | |
| Clock phase time | | t _{KHKL} / t _{KLKH} | 2.0 | – | ns | |
| Setup times | Address | t _{AVKH} | 1.5 | – | ns | |
| | Write data | t _{DVKH} | | | | |
| | Write enable | t _{WVKH} | | | | |
| | Chip select | t _{SVKH} | | | | |
| Hold times | Address | t _{KHAX} | 0.5 | – | ns | |
| | Write data | t _{KHDX} | | | | |
| | Write enable | t _{KHWX} | | | | |
| | Chip select | t _{KHSX} | | | | |
| Clock access time | | t _{KHQV} | – | 3.8 | ns | 1 |
| K high to Q change | | t _{KHQX} | 1.5 | – | ns | 2 |
| /G low to Q valid | | t _{GLQV} | – | 3.8 | ns | 1 |
| /G low to Q change | | t _{GLQX} | 0 | – | ns | 2 |
| /G high to Q Hi-Z | | t _{GHQZ} | 0 | 3.8 | ns | 2 |
| K high to Q Hi-Z (/SW) | | t _{KHQZ} | 1.5 | 3.8 | ns | 2 |
| K high to Q Hi-Z (/SS) | | t _{KHQZ2} | 1.5 | 3.8 | ns | 2 |
| K high to Q Lo-Z | | t _{KHQX2} | 1.5 | – | ns | 2 |
| Sleep Mode Recovery | | t _{ZZR} | – | 7.5 | ns | |
| Sleep Mode Enable | | t _{ZZE} | – | 7.5 | ns | |

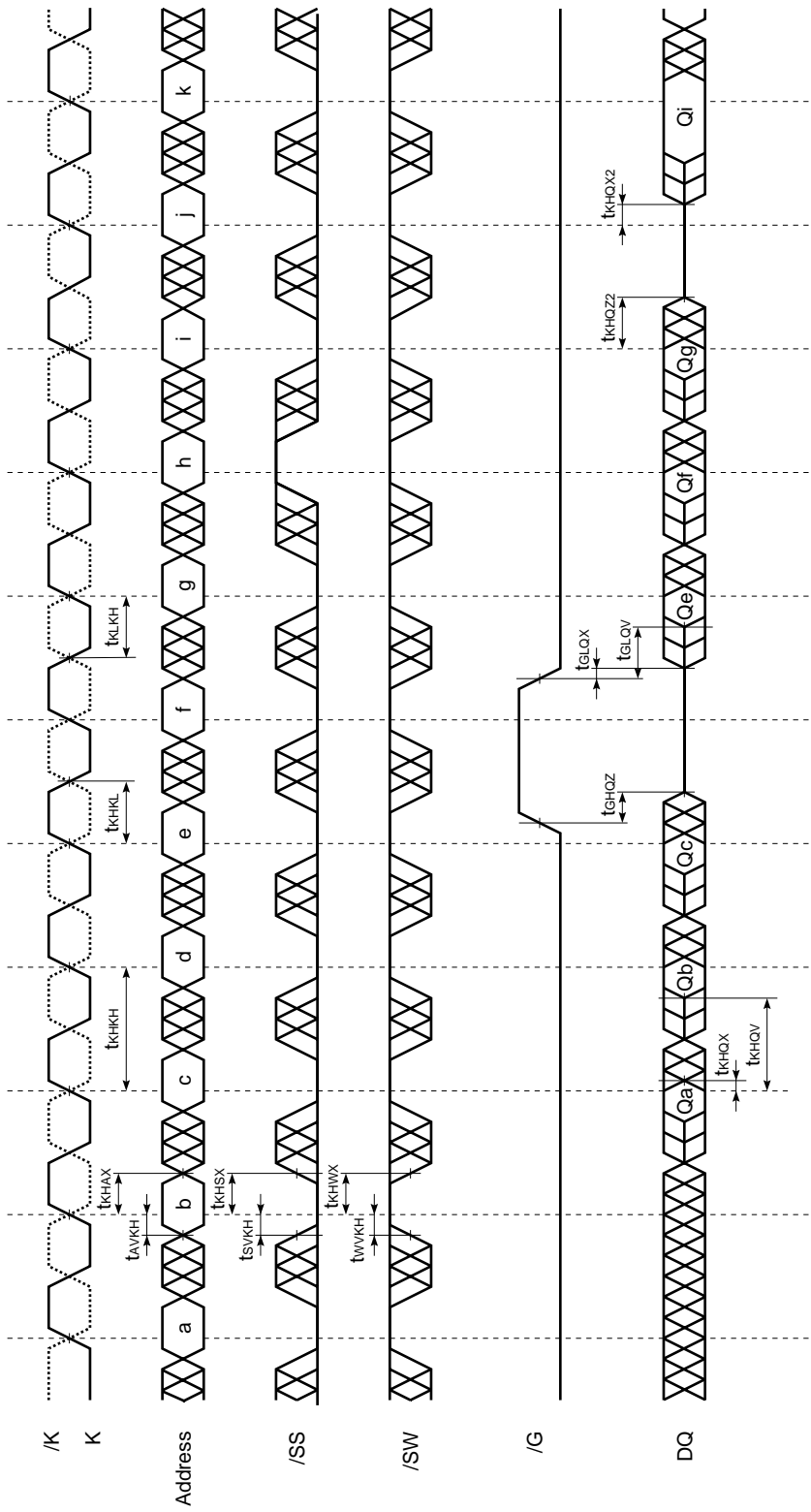
Notes 1. See figure. (V_{TT} = 0.75 V)



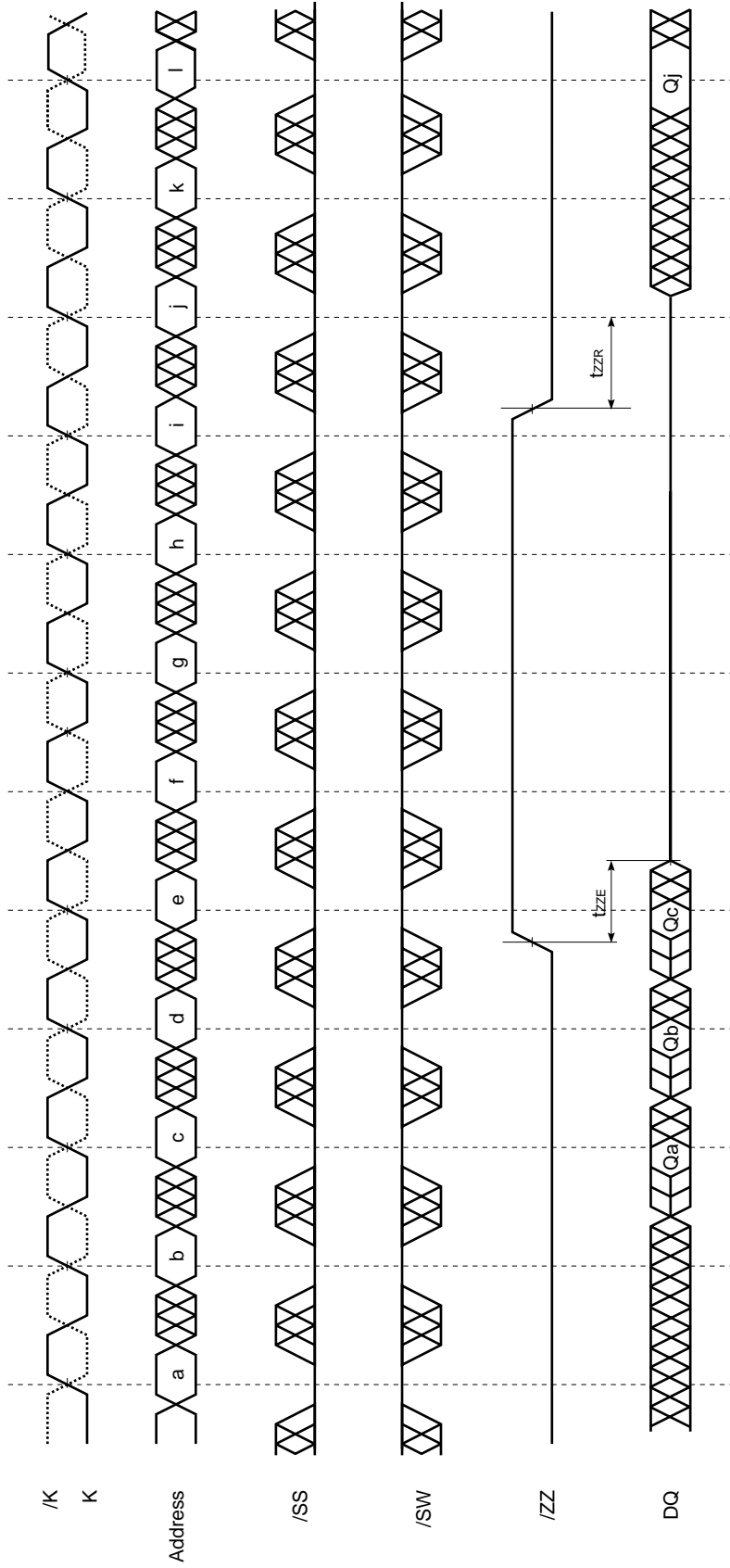
2. See figure. (V_{TT} = 0.75 V)



Read Operation

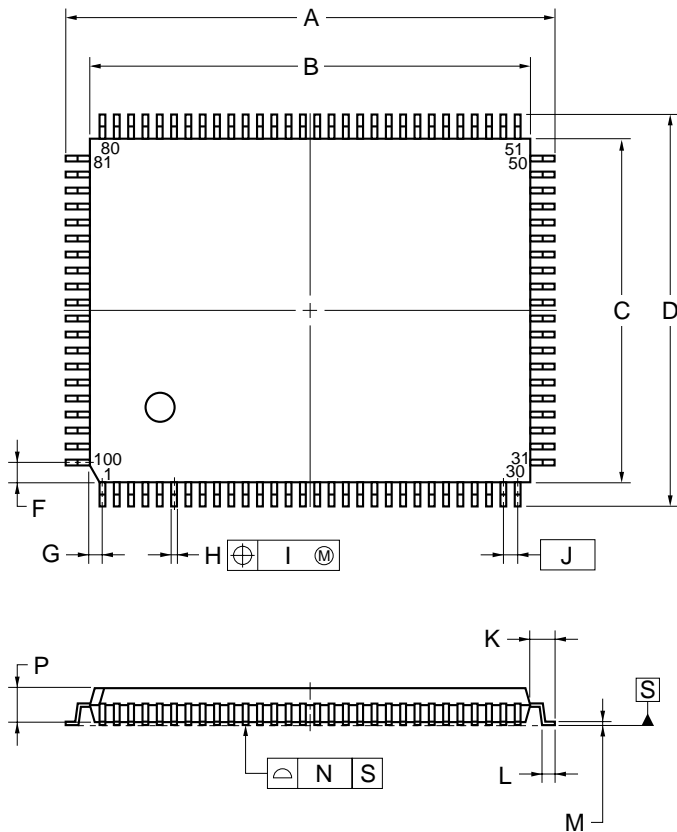


Sleep Mode

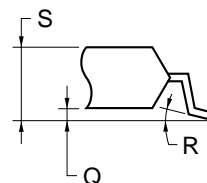


Package Drawing

100-PIN PLASTIC LQFP (14x20)



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|------|--|
| A | 22.0±0.2 |
| B | 20.0±0.2 |
| C | 14.0±0.2 |
| D | 16.0±0.2 |
| F | 0.825 |
| G | 0.575 |
| H | 0.32 ^{+0.08} _{-0.07} |
| I | 0.13 |
| J | 0.65 (T.P.) |
| K | 1.0±0.2 |
| L | 0.5±0.2 |
| M | 0.17 ^{+0.06} _{-0.05} |
| N | 0.10 |
| P | 1.4 |
| Q | 0.125±0.075 |
| R | 3° ^{+7°} _{-3°} |
| S | 1.7 MAX. |

S100GF-65-8ET-1

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μ PD4443362.

Type of Surface Mount Device

μ PD4443362GF: 100-PIN PLASTIC LQFP (14 x 20)

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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