

DDR SDRAM 128Mb F-die (x4, x8)

DDR SDRAM

128Mb F-die DDR SDRAM Specification

66 TSOP-II with Pb-Free
(RoHS compliant)

Revision 1.0

May 2004

Rev. 1.1 May. 2004

128Mb F-die Revision History

Revision 1.0 (April, 2004)

- Revision 1.0 spec. release.

Revision 1.1 (May, 2004)

- Corrected typo.

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DDR SDRAM

Key Features

- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Four banks operation
- Differential clock inputs(CK and $\overline{\text{CK}}$)
- DLL aligns DQ and DQS transition with CK transition
- MRS cycle with address key programs
 - . Read latency 2, 2.5 (clock)
 - . Burst length (2, 4, 8)
 - . Burst type (sequential & interleave)
- All inputs except data & DM are sampled at the positive going edge of the system clock(CK)
- Data I/O transactions on both edges of data strobe
- Edge aligned data output, center aligned data input
- DM for write masking only (x4, x8)
- Auto & Self refresh
- 15.6us refresh interval(4K/64ms refresh)
- Maximum burst refresh cycle : 8
- 66pin TSOP II **Pb-Free** package
- **RoHS compliant**

Ordering Information

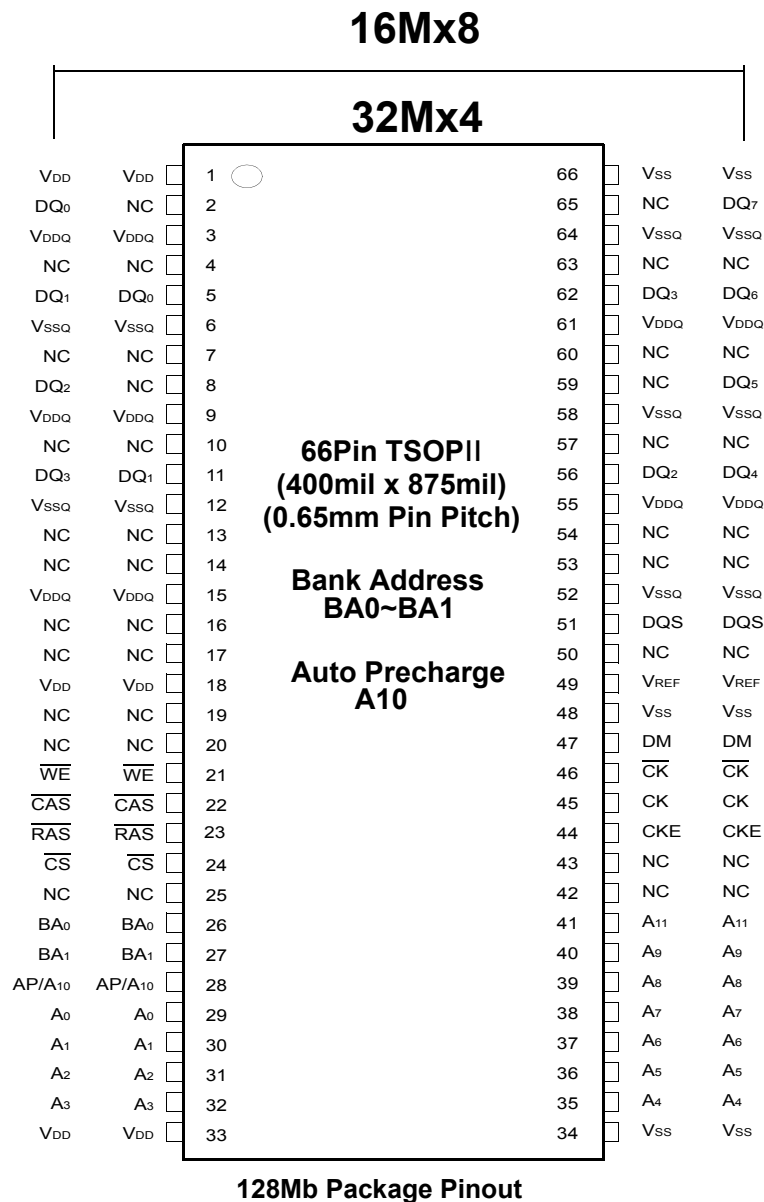
Part No.	Org.	Max Freq.	Interface	Package
K4H280438F-UC/LA2	32M x 4	A2(DDR266@CL=2)	SSTL2	66pin TSOP II
K4H280438F-UC/LB0		B0(DDR266@CL=2.5)		
K4H280438F-UC/LA0		A0(DDR200@CL=2)		
K4H280838F-UC/LB3	16M x 8	B3(DDR333@CL=2.5)	SSTL2	66pin TSOP II
K4H280838F-UC/LA2		A2(DDR266@CL=2)		
K4H280838F-UC/LB0		B0(DDR266@CL=2.5)		

Operating Frequencies

	B3(DDR333@CL=2.5)	A2(DDR266@CL=2.0)	B0(DDR266@CL=2.5)	A0(DDR200@CL=2.0)
Speed @CL2	133MHz	133MHz	100MHz	100MHz
Speed @CL2.5	166MHz	133MHz	133MHz	-

*CL : CAS Latency

Pin Description



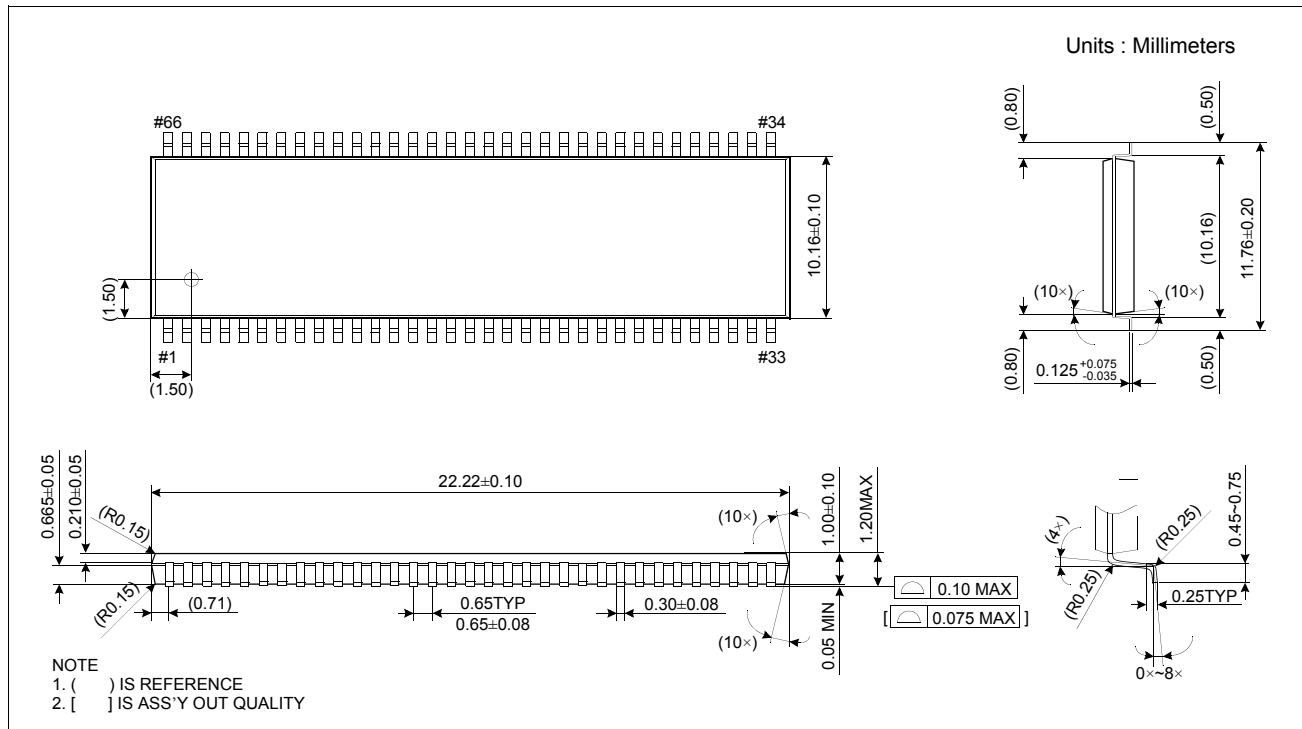
Organization	Row Address	Column Address
32Mx4	A0~A11	A0-A9, A11
16Mx8	A0~A11	A0-A9

DM is internally loaded to match DQ and DQS identically.

Row & Column address configuration

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Package Physical Dimension

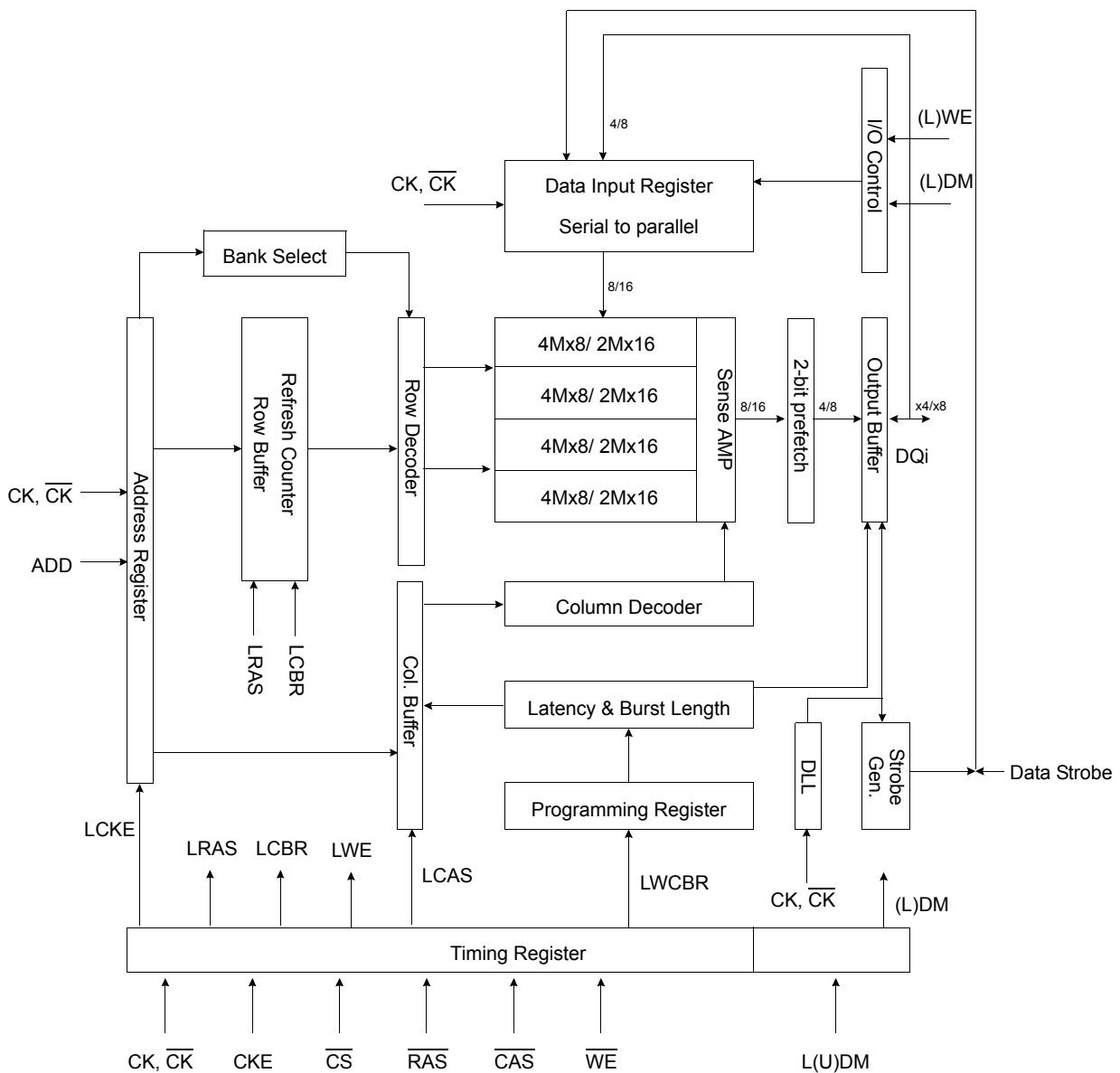


66pin TSOPII / Package dimension

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Block Diagram (8Mbit x 4 / 4Mbit x 8 I/O x 4 Banks)



Input/Output Function Description

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{\text{CK}}$	Input	Clock : CK and $\overline{\text{CK}}$ are differential clock inputs. All address and control input signals are sampled on the positive edge of CK and negative edge of $\overline{\text{CK}}$. Output (read) data is referenced to both edges of CK. Internal clock signals are derived from CK/ $\overline{\text{CK}}$.
CKE	Input	Clock Enable : CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for disabling outputs, which is achieved asynchronously. Input buffers, excluding CK, $\overline{\text{CK}}$ and CKE are disabled during power-down and self refresh modes, providing low standby power. CKE will recognize an LVCMOS LOW level prior to VREF being stable on power-up.
$\overline{\text{CS}}$	Input	Chip Select : $\overline{\text{CS}}$ enables(registered LOW) and disables(registered HIGH) the command decoder. All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external bank selection on systems with multiple banks. $\overline{\text{CS}}$ is considered part of the command code.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Input	Command Inputs : $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$) define the command being entered.
LDM,(UDM)	Input	Input Data Mask : DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0~D7 ; UDM corresponds to the data on DQ8~DQ15. DM may be driven high, low, or floating during READs.
BA0, BA1	Input	Bank Address Inputs : BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A [0 : 11]	Input	Address Inputs : Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS). A12 & A13 are used on device densities of 256Mb and greater, and A13 is used only on 1Gb devices.
DQ	I/O	Data Input/Output : Data bus
LDQS,(U)DQS	I/O	Data Strobe : Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0~D7 ; UDQS corresponds to the data on DQ8~DQ15
NC	-	No Connect : No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply : +2.5V $\pm$ 0.2V.
VSSQ	Supply	DQ Ground.
VDD	Supply	Power Supply : +2.5V $\pm$ 0.2V (device specific).
VSS	Supply	Ground.
VREF	Input	SSTL_2 reference voltage.

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Command Truth Table

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND			CKEn-1	CKEn	CS	RAS	CAS	WE	BA0,1	A10/AP	A0 ~ A9, A11	Note	
Register	Extended MRS		H	X	L	L	L	L	OP CODE			1, 2	
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1, 2	
Refresh	Auto Refresh		H	H	L	L	L	H	X			3	
	Self Refresh	Entry		L								3	
		Exit	L	H	L	H	H	H	X			3	
												H	X
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address			
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address	4	
	Auto Precharge Enable									H		4	
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address	4	
	Auto Precharge Enable									H		4, 6	
Burst Stop			H	X	L	H	H	L	X			7	
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X		
	All Banks								X	H		5	
Active Power Down		Entry	H	L	H	X	X	X	X				
					L	V	V	V					
		Exit	L	H	X	X	X	X					
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X				
					L	H	H	H					
		Exit	L	H	H	X	X	X					
					L	V	V	V					
DM(UDM/LDM for x16 only)			H	X					X			8	
No operation (NOP) : Not defined			H	X	H	X	X	X	X			9	
					L	H	H	H				9	

Note : 1. OP Code : Operand Code. A0 ~ A11 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)

2. EMRS/MRS can be issued only at all banks precharge state.

A new command can be issued 2 clock cycles after EMRS or MRS.

3. Auto refresh functions are same as the CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.

If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.

6. During burst write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

7. Burst stop command is valid at every burst length.

8. DM(x4/8) sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).

UDM/LDM(x16 only) sampled at the rising and falling edges of the UDQS/LDQS and Data-in are masked at the both edges

(Write UDM/LDM latency is 0).

9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

DDR SDRAM 128Mb F-die (x4, x8)

DDR SDRAM

8M x 4Bit x 4 Banks / 4M x 8Bit x 4 Banks Double Data Rate SDRAM

General Description

The K4H280438F / K4H280838F is 134,217,728 bits of double data rate synchronous DRAM organized as 4x 8,388,608 / 4x 4,194,304 words by 4/ 8bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 333Mb/s per pin. I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} & V_{DDQ} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.5	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommend operation condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operating Conditions

Recommended operating conditions(Voltage referenced to $V_{SS}=0V$, $T_A=0$ to $70^{\circ}C$)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V_{DD} of 2.5V)	V_{DD}	2.3	2.7		
I/O Supply voltage	V_{DDQ}	2.3	2.7	V	
I/O Reference voltage	V_{REF}	0.49* V_{DDQ}	0.51* V_{DDQ}	V	1
I/O Termination voltage(system)	V_{TT}	$V_{REF}-0.04$	$V_{REF}+0.04$	V	2
Input logic high voltage	$V_{IH}(DC)$	$V_{REF}+0.15$	$V_{DDQ}+0.3$	V	
Input logic low voltage	$V_{IL}(DC)$	-0.3	$V_{REF}-0.15$	V	
Input Voltage Level, CK and $\overline{CK}$ inputs	$V_{IN}(DC)$	-0.3	$V_{DDQ}+0.3$	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	$V_{ID}(DC)$	0.36	$V_{DDQ}+0.6$	V	3
V-I Matching: Pullup to Pulldown Current Ratio	$V_I(Ratio)$	0.71	1.4	-	4
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current(Normal strength driver) ; $V_{OUT} = V_{TT} + 0.84V$	I_{OH}	-16.8		mA	
Output High Current(Normal strength driver) ; $V_{OUT} = V_{TT} - 0.84V$	I_{OL}	16.8		mA	
Output High Current(Half strength driver) ; $V_{OUT} = V_{TT} + 0.45V$	I_{OH}	-9		mA	
Output High Current(Half strength driver) ; $V_{OUT} = V_{TT} - 0.45V$	I_{OL}	9		mA	

Note : 1. V_{REF} is expected to be equal to 0.5* V_{DDQ} of the transmitting device, and to track variations in the dc level of same.
Peak-to-peak noise on V_{REF} may not exceed +/-2% of the dc value.
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} , and must track variations in the DC level of V_{REF} .
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
4. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25V to 1.0V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1/7 for device drain to source voltages from 0.1 to 1.0.

DDR SDRAM Spec Items & Test Conditions

Conditions	Symbol
Operating current - One bank Active-Precharge; tRC=tRCmin; tCK=7.5ns for DDR266, 6ns for DDR333; DQ,DM and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	IDD0
Operating current - One bank operation ; One bank open, BL=4, Reads - Refer to the following page for detailed test condition	IDD1
Percharge power-down standby current; All banks idle; power - down mode; CKE = <VIL(max); tCK=7.5ns for DDR266, 6ns for DDR333; Vin = Vref for DQ,DQS and DM.	IDD2P
Precharge Floating standby current; CS# >= VIH(min);All banks idle; CKE >= VIH(min); tCK=7.5ns for DDR266, 6ns for DDR333; Address and other control inputs changing once per clock cycle; Vin = Vref for DQ,DQS and DM	IDD2F
Precharge Quiet standby current; CS# >= VIH(min); All banks idle; CKE >= VIH(min); tCK=7.5ns for DDR266, 6ns for DDR333; Address and other control inputs stable at >= VIH(min) or <=VIL(max); Vin = Vref for DQ ,DQS and DM	IDD2Q
Active power - down standby current ; one bank active; power-down mode; CKE=< VIL (max); tCK=7.5ns for DDR266, 6ns for DDR333; Vin = Vref for DQ,DQS and DM	IDD3P
Active standby current; CS# >= VIH(min); CKE>=VIH(min); one bank active; active - precharge; tRC=tRASmax; tCK=7.5ns for DDR266, 6ns for DDR333; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	IDD3N
Operating current - burst read; Burst length = 2; reads; contiguous burst; One bank active; address and control inputs changing once per clock cycle; CL=2 at 7.5ns for DDR266(A2), CL=2.5 at 7.5ns for DDR266(B0), 6ns for DDR333; 50% of data changing on every transfer; Iout = 0 m A	IDD4R
Operating current - burst write; Burst length = 2; writes; continuous burst; One bank active address and control inputs changing once per clock cycle; CL=2 at tCK=7.5ns for DDR266(A2), CL=2.5 at tCK=7.5ns for DDR266(B0), 6ns for DDR333; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every burst	IDD4W
Auto refresh current; tRC = tRFC(min) - 10*tCK for DDR266 at tCK=7.5ns; 12*tCK for DDR333 at tCK=6ns; distributed refresh	IDD5
Self refresh current; CKE =< 0.2V; External clock on; tCK = 7.5ns for DDR266, 6ns for DDR333.	IDD6
Operating current - Four bank operation ; Four bank interleaving with BL=4 -Refer to the following page for detailed test condition	IDD7A

Input/Output Capacitance

(V_{DD}=2.5, V_{DDQ}=2.5V, T_A= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Delta	Unit	Note
Input capacitance (A0 ~ A11, BA0 ~ BA1, CKE, $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	CIN1	2	3	0.5	pF	4
Input capacitance(CK, $\overline{\text{CK}}$)	CIN2	2	3	0.25	pF	4
Data & DQS input/output capacitance	COU	4	5	0.5	pF	1,2,3,4
Input capacitance(DM for x4/8, UDM/LDM for x16)	CIN3	4	5		pF	1,2,3,4

Note : 1. These values are guaranteed by design and are tested on a sample basis only.

2. Although DM is an input -only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match signal propagation times of DQ, DQS, and DM in the system.

3. Unused pins are tied to ground.

4. This parameter is sampled. VDDQ = +2.5V +0.2V, VDD = +3.3V +0.3V or +2.5V+0.2V, f=100MHz, tA=25°C, Vout(dc) = VDDQ/2, Vout(peak to peak) = 0.2V. DM inputs are grouped with I/O pins - reflecting the fact that they are matched in loading (to facilitate trace matching at the board level).

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DDR SDRAM

DDR SDRAM I_{DD} spec table

(V_{DD}=2.7V, T = 10°C)

Symbol		32Mx4 (K4H280438F)			Unit	Notes
		A2(DDR266@CL=2.0)	B0(DDR266@CL=2.5)	A0(DDR200@CL=2.0)		
IDD0		80	80	75	mA	
IDD1		105	105	95	mA	
IDD2P		3	3	3	mA	
IDD2F		18	18	18	mA	
IDD2Q		15	15	15	mA	
IDD3P		25	25	25	mA	
IDD3N		35	35	35	mA	
IDD4R		105	105	105	mA	
IDD4W		120	120	120	mA	
IDD5		150	150	150	mA	
IDD6	Normal	2	2	2	mA	
	Low power	1	1	1	mA	Optional
IDD7A		280	280	240	mA	

Symbol		16Mx8 (K4H280838F)			Unit	Notes
		B3(DDR333@CL=2.5)	A2(DDR266@CL=2.0)	B0(DDR266@CL=2.5)		
IDD0		85	85	75	mA	
IDD1		110	110	100	mA	
IDD2P		3	3	3	mA	
IDD2F		22	20	20	mA	
IDD2Q		20	15	15	mA	
IDD3P		25	25	25	mA	
IDD3N		40	35	35	mA	
IDD4R		140	120	120	mA	
IDD4W		145	125	125	mA	
IDD5		165	155	155	mA	
IDD6	Normal	2	2	2	mA	
	Low power	1	1	1	mA	Optional
IDD7A		300	300	250	mA	

< Detailed test conditions for DDR SDRAM IDD1 & IDD7A >**IDD1 : Operating current: One bank operation**

1. Only one bank is accessed with $t_{RC}(\min)$, Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. $I_{out} = 0\text{mA}$

2. Timing patterns

- B0(133Mhz, CL=2.5) : $t_{CK} = 7.5\text{ns}$, CL=2.5, BL=4, $t_{RCD} = 3*t_{CK}$, $t_{RC} = 9*t_{CK}$, $t_{RAS} = 6*t_{CK}$
Read : A0 N N R0 N N P0 N N A0 N - repeat the same timing with random address changing
*50% of data changing at every burst

- A2 (133Mhz, CL=2) : $t_{CK} = 7.5\text{ns}$, CL=2, BL=4, $t_{RCD} = 3*t_{CK}$, $t_{RC} = 9*t_{CK}$, $t_{RAS} = 6*t_{CK}$
Read : A0 N N R0 N N P0 N N A0 N - repeat the same timing with random address changing
*50% of data changing at every burst

- AA (133Mhz, CL=2) : $t_{CK} = 7.5\text{ns}$, CL=2, BL=4, $t_{RCD} = 2*t_{CK}$, $t_{RC} = 8*t_{CK}$, $t_{RAS} = 6*t_{CK}$
Read : A0 N R0 N N N P0 N A0 N - repeat the same timing with random address changing
*50% of data changing at every burst

- B3(166Mhz, CL=2.5) : $t_{CK}=6\text{ns}$, CL=2.5, BL=4, $t_{RCD}=3*t_{CK}$, $t_{RC} = 10*t_{CK}$, $t_{RAS}=7*t_{CK}$
Read : A0 N N R0 N N P0 N N A0 N - repeat the same timing with random address changing
*50% of data changing at every burst

Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

IDD7A : Operating current: Four bank operation

1. Typical Case : $V_{dd} = 2.5\text{V}$, $T=25^\circ\text{C}$

2. Worst Case : $V_{dd} = 2.7\text{V}$, $T= 10^\circ\text{C}$

3. Four banks are being interleaved with $t_{RC}(\min)$, Burst Mode, Address and Control inputs on NOP edge are not changing. $I_{out} = 0\text{mA}$

4. Timing patterns

- B0(133Mhz, CL=2.5) : $t_{CK} = 7.5\text{ns}$, CL=2.5, BL=4, $t_{RRD} = 2*t_{CK}$, $t_{RCD} = 3*t_{CK}$, Read with autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
*100% of data changing at every burst

- A2(133Mhz, CL=2) : $t_{CK} = 7.5\text{ns}$, CL=2, BL=4, $t_{RRD} = 2*t_{CK}$, $t_{RCD} = 3*t_{CK}$, Read with autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
*100% of data changing at every burst

- AA(133Mhz, CL=2) : $t_{CK} = 7.5\text{ns}$, CL=2, BL=4, $t_{RRD} = 2*t_{CK}$, $t_{RCD} = 3*t_{CK}$, Read with autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing
*100% of data changing at every burst

- B3(166Mhz, CL=2.5) : $t_{CK}=6\text{ns}$, CL=2.5, BL=4, $t_{RRD}=2*t_{CK}$, $t_{RCD}=3*t_{CK}$, Read with autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
*100% of data changing at every burst

Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

AC Operating Conditions

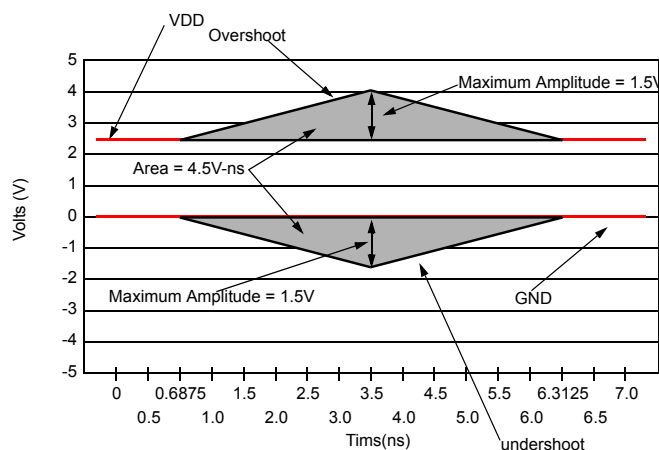
Parameter/Condition	Symbol	Min	Max-10	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	VIL(AC)		VREF - 0.31	V	
Input Differential Voltage, CK and /CK inputs	VID(AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and /CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Notes :

1. VID is the magnitude of the difference between the input level on CK and the input level on /CK.
2. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the dc level of the same.

AC Overshoot/Undershoot specification for Address and Control Pins

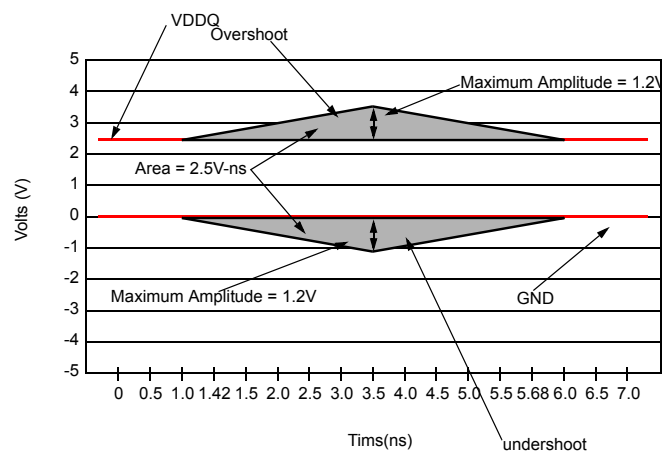
Parameter	Specification	
	DDR333	DDR266
Maximum peak amplitude allowed for overshoot	TBD	1.5 V
Maximum peak amplitude allowed for undershoot	TBD	1.5 V
The area between the overshoot signal and VDD must be less than or equal to	TBD	4.5 V-ns
The area between the undershoot signal and GND must be less than or equal to	TBD	4.5 V-ns



AC overshoot/Undershoot Definition

Overshoot/Undershoot specification for Data, Strobe, and Mask Pins

Parameter	Specification	
	DDR333	DDR266
Maximum peak amplitude allowed for overshoot	TBD	1.2 V
Maximum peak amplitude allowed for undershoot	TBD	1.2 V
The area between the overshoot signal and VDD must be less than or equal to	TBD	2.4 V-ns
The area between the undershoot signal and GND must be less than or equal to	TBD	2.4 V-ns



DQ/DM/DQS AC overshoot/Undershoot Definition

DDR SDRAM 128Mb F-die (x4, x8)

DDR SDRAM

AC Timing Parameters & Specifications

Parameter	Symbol	B3 (DDR333@CL=2.5)		A2 (DDR266@CL=2.0)		B0 (DDR266@CL=2.5)		A0 (DDR200@CL=2.0)		Unit	Note	
		Min	Max	Min	Max	Min	Max	Min	Max			
Row cycle time	tRC	60		65		65		70		ns		
Refresh row cycle time	tRFC	72		75		75		80		ns		
Row active time	tRAS	42	70K	45	120K	45	120K	48	120K	ns		
RAS to CAS delay	tRCD	18		20		20		20		ns		
Row precharge time	tRP	18		20		20		20		ns		
Row active to Row active delay	tRRD	12		15		15		15		ns		
Write recovery time	tWR	15		15		15		15		ns		
Last data in to Read command	tWTR	1		1		1		1		tCK		
Col. address to Col. address delay	tCCD	1		1		1		1		tCK		
Clock cycle time	CL=2.0	tCK	7.5	12	7.5	12	10	12	10	12	ns	
	CL=2.5		6	12	7.5	12	7.5	12			ns	
Clock high level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK		
Clock low level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK		
DQS-out access time from CK/CK	tDQSC	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns		
Output data access time from CK/CK	tAC	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns		
Data strobe edge to ouput data edge	tDQSQ	-	0.45	-	0.5	-	0.5	-	0.6	ns	12	
Read Preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK		
Read Postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK		
CK to valid DQS-in	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	tCK		
DQS-in setup time	tWPRES	0		0		0		0		ns	3	
DQS-in hold time	tWPRE	0.25		0.25		0.25		0.25		tCK		
DQS falling edge to CK rising-setup time	tDSS	0.2		0.2		0.2		0.2		tCK		
DQS falling edge from CK rising-hold time	tDSH	0.2		0.2		0.2		0.2		tCK		
DQS-in high level width	tDQSH	0.35		0.35		0.35		0.35		tCK		
DQS-in low level width	tDQSL	0.35		0.35		0.35		0.35		tCK		
DQS-in cycle time	tDSC	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK		
Address and Control Input setup time(fast)	tIS	0.75		0.9		0.9		1.1		ns	i,5.7	
Address and Control Input hold time(fast)	tIH	0.75		0.9		0.9		1.1		ns	i,5.7	
Address and Control Input setup time(slow)	tIS	0.8		1.0		1.0		1.1		ns	i,	
Address and Control Input hold time(slow)	tIH	0.8		1.0		1.0		1.1		ns	i,	
Data-out high impedance time from CK/CK	tHZ		+0.7		+0.75		+0.75	-0.8	+0.8	ns	1	
Data-out low impedance time from CK/CK	tLZ	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	1	
Mode register set cycle time	tMRD	12		15		15		16		ns		
DQ & DM setup time to DQS	tDS	0.45		0.5		0.5		0.6		ns	j, k	
DQ & DM hold time to DQS	tDH	0.45		0.5		0.5		0.6		ns	j, k	
Control & Address input pulse width	tIPW	2.2		2.2		2.2		2.5		ns	8	
DQ & DM input pulse width	tDIPW	1.75		1.75		1.75		2		ns	8	
Power down exit time	tPDEX	6		7.5		7.5		10		ns		
Exit self refresh to non-Read command	tXSNR	75		75		75		80		ns		
Exit self refresh to read command	tXSRD	200		200		200		200		tCK		
Refresh interval time	tREFI		7.8		7.8		7.8	15.6		us	4	
Output Slew Rate Matching Ratio(rise to fall)	tSLMR	0.67	1.5	0.67	1.5	0.67	1.5	0.67	1.5			

DDR SDRAM 128Mb F-die (x4, x8)

DDR SDRAM

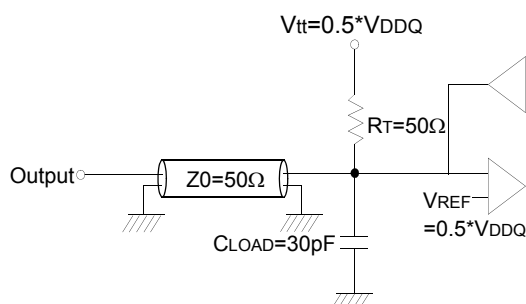
Parameter	Symbol	B3 (DDR333@CL=2.5))		A2 (DDR266@CL=2.0)		B0 (DDR266@CL=2.5))		A0 (DDR200@CL=2.0))		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Output DQS valid window	tQH	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	ns	11
Clock half period	tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	10, 11
Data hold skew factor	tQHS		0.55		0.75		0.75		0.8	ns	11
DQS write postamble time	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	2
Active to Read with Auto precharge command	tRAP	18		20		20		20			
Autoprecharge write recovery + Precharge time	tDAL	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		tCK	13

AC Operating Test Conditions

(VDD=2.5V, VDDQ=2.5V, TA= 0 to 70°C)

Parameter	Value	Unit	Note
Input reference voltage for Clock	0.5 * VDDQ	V	
Input signal maximum peak swing	1.5	V	
Input signal minimum slew rate (for input only)	0.5	V/ns	
Input slew rate (I/O pins)	0.5	V/ns	
Input Levels(VIH/VIL)	VREF+0.31/VREF-0.31	V	
Input timing measurement reference level	VREF	V	
Output timing measurement reference level	Vtt	V	
Output load condition	See Load Circuit		

AC operating test conditions



Output Load Circuit (SSTL_2)

DDR SDRAM 128Mb F-die (x4, x8)

DDR SDRAM

System Characteristics for DDR SDRAM

The following specification parameters are required in systems using DDR333, DDR266 devices to ensure proper system performance. these characteristics are for system simulation purposes and are guaranteed by design.

Table 1 : Input Slew Rate for DQ, DQS, and DM

AC CHARACTERISTICS		DDR333		DDR266		Units	Notes
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX		
DQ/DM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC)	DCSLEW	TBD	TBD	TBD	TBD	V/ns	a, m

Table 2 : Input Setup & Hold Time Derating for Slew Rate

Input Slew Rate	tIS	tIH	Units	Notes
0.5 V/ns	0	0	ps	i
0.4 V/ns	+50	0	ps	i
0.3 V/ns	+100	0	ps	i

Table 3 : Input/Output Setup & Hold Time Derating for Slew Rate

Input Slew Rate	tDS	tDH	Units	Notes
0.5 V/ns	0	0	ps	k
0.4 V/ns	+75	+75	ps	k
0.3 V/ns	+150	+150	ps	k

Table 4 : Input/Output Setup & Hold Derating for Rise/Fall Delta Slew Rate

Delta Slew Rate	tDS	tDH	Units	Notes
+/- 0.0 V/ns	0	0	ps	j
+/- 0.25 V/ns	+50	+50	ps	j
+/- 0.5 V/ns	+100	+100	ps	j

Table 5 : Output Slew Rate Characteristic (X4, X8 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Notes
Pullup Slew Rate	1.2 ~ 2.5	1.0	4.5	a,c,d,f,g,h
Pulldown slew	1.2 ~ 2.5	1.0	4.5	b,c,d,f,g,h

Table 6 : Output Slew Rate Characteristic (X16 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Notes
Pullup Slew Rate	1.2 ~ 2.5	0.7	5.0	a,c,d,f,g,h
Pulldown slew	1.2 ~ 2.5	0.7	5.0	b,c,d,f,g,h

Table 7 : Output Slew Rate Matching Ratio Characteristics

AC CHARACTERISTICS		DDR266		
PARAMETER		MIN	MAX	Notes
Output Slew Rate Matching Ratio (Pullup to Pulldown)		TBD	TBD	e,m

Component Notes

1. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. these parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ), or begins driving (LZ).
2. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
3. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. when no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
4. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
5. For command/address input slew rate ≥ 1.0 V/ns
6. For command/address input slew rate ≥ 0.5 V/ns and < 1.0 V/ns
7. For CK & $\overline{\text{CK}}$ slew rate ≥ 1.0 V/ns
8. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
9. Slew Rate is measured between VOH(ac) and VOL(ac).
10. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).....For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.
11. tQH = tHP - tQHS, where:
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
12. tDQSQ
Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
13. tDAL = (tWR/tCK) + (tRP/tCK)
For each of the terms above, if not already an integer, round to the next highest integer. Example: For DDR266B at CL=2.5 and tCK=7.5ns tDAL = (15 ns / 7.5 ns) + (20 ns / 7.5ns) = (2) + (3)
tDAL = 5 clocks

System Notes :

- a. Pullup slew rate is characterized under the test conditions as shown in Figure 1.

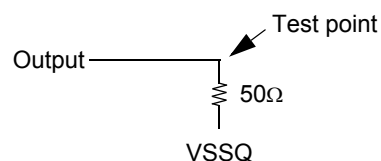


Figure 1 : Pullup slew rate test load

b. Pulldown slew rate is measured under the test conditions shown in Figure 2.

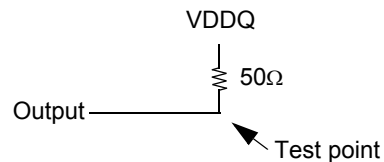


Figure 2 : Pulldown slew rate test load

c. Pullup slew rate is measured between (VDDQ/2 - 320 mV +/- 250 mV)

Pulldown slew rate is measured between (VDDQ/2 + 320 mV +/- 250 mV)

Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.

Example : For typical slew rate, DQ0 is switching

For minimum slew rate, all DQ bits are switching from either high to low, or low to high.

The remaining DQ bits remain the same as for previous state.

d. Evaluation conditions

Typical : 25 °C (T Ambient), VDDQ = 2.5V, typical process

Minimum : 70 °C (T Ambient), VDDQ = 2.3V, slow - slow process

Maximum : 0 °C (T Ambient), VDDQ = 2.7V, fast - fast process

e. The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

f. Verified under typical conditions for qualification purposes.

g. TSOP1 package devices only.

h. Only intended for operation up to 266 Mbps per pin.

i. A derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5V/ns

as shown in Table 2. The Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.

j. A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ, as shown in Tables 3 & 4.

Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.

The delta rise/fall rate is calculated as:

$$\{1/(\text{Slew Rate1})\} - \{1/(\text{Slew Rate2})\}$$

For example : If Slew Rate 1 is 0.5 V/ns and slew Rate 2 is 0.4 V/ns, then the delta rise, fall rate is - 0.5ns/V . Using the table given, this would result in the need for an increase in tDS and tDH of 100 ps.

k. Table 3 is used to increase tDS and tDH in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser of the AC - AC slew rate and the DC- DC slew rate. The input slew rate is based on the lesser of the slew rates determined by either VIH(ac) to VIL(ac) or VIH(DC) to VIL(DC), and similarly for rising transitions.

m. DQS, DM, and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotony.

IBIS :I/V Characteristics for Input and Output Buffers

DDR SDRAM Output Driver V-I Characteristics

DDR SDRAM Output driver characteristics are defined for full and half strength operation as selected by the EMRS bit A1.

Figures 3 and 4 show the driver characteristics graphically, and tables 8 and 9 show the same data in tabular format suitable for input into simulation tools. The driver characteristics evaluation conditions are:

Typical	25°C	Vdd/Vddq = 2.5V, typical process
Minimum	70°C	Vdd/Vddq = 2.3V, slow-slow process
Maximum	0°C	Vdd/Vddq = 2.7V, fast-fast process

Output Driver Characteristic Curves Notes:

1. The full variation in driver current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 3 and 4.
2. It is recommended that the "typical" IBIS V-I curve lie within the inner bounding lines of the V-I curves of Figure 3 and 4.
3. The full variation in the ratio of the "typical" IBIS pullup to "typical" IBIS pulldown current should be unity +/- 10%, for device drain to source voltages from 0.1 to 1.0. This specification is a design objective only. It is not guaranteed.

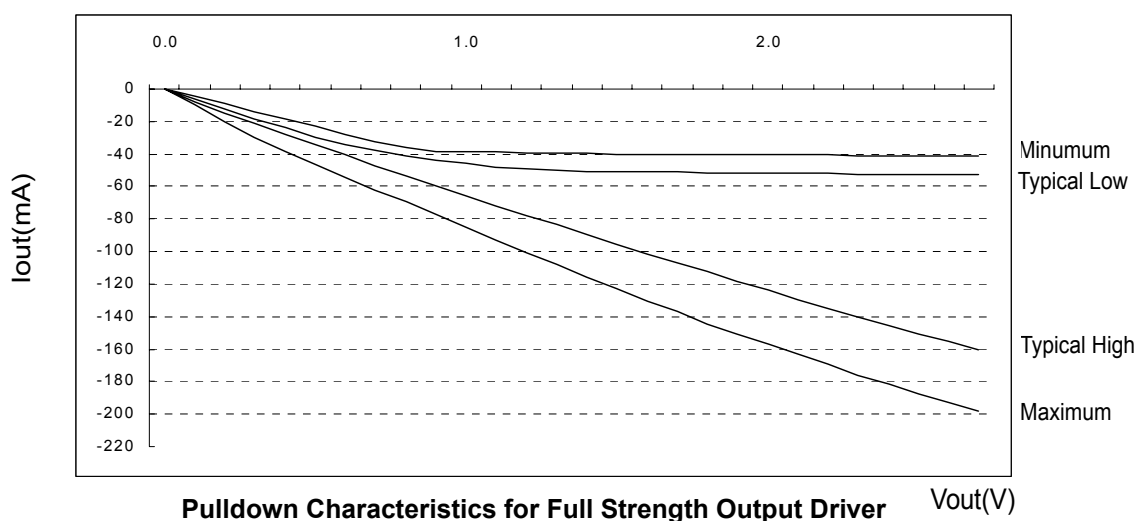
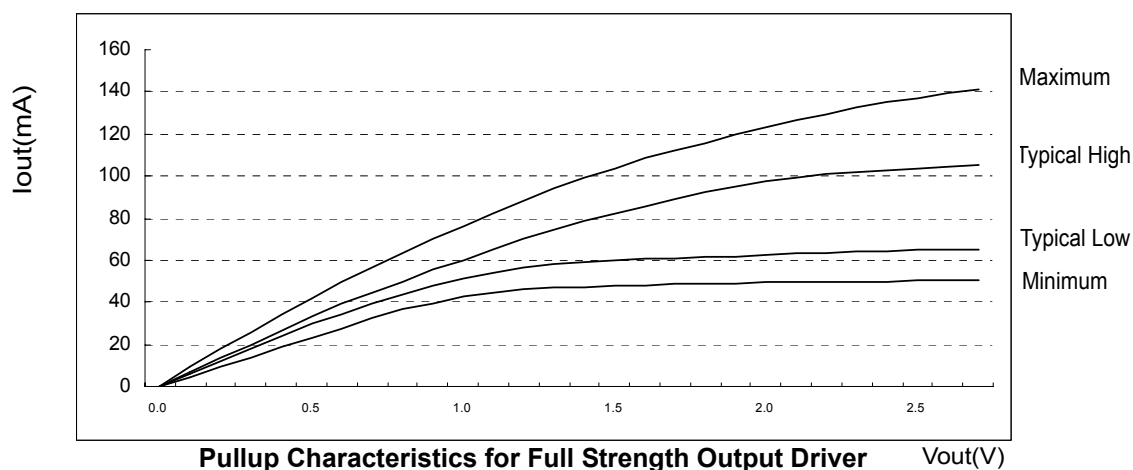


Figure 3. I/V characteristics for input/output buffers: Pull up(above) and pull down(below)

Voltage (V)	Pulldown Current (mA)				pullup Current (mA)			
	Typical Low	Typical High	Minimum	Maximum	Typical Low	Typical High	Minimum	Maximum
0.1	6.0	6.8	4.6	9.6	-6.1	-7.6	-4.6	-10.0
0.2	12.2	13.5	9.2	18.2	-12.2	-14.5	-9.2	-20.0
0.3	18.1	20.1	13.8	26.0	-18.1	-21.2	-13.8	-29.8
0.4	24.1	26.6	18.4	33.9	-24.0	-27.7	-18.4	-38.8
0.5	29.8	33.0	23.0	41.8	-29.8	-34.1	-23.0	-46.8
0.6	34.6	39.1	27.7	49.4	-34.3	-40.5	-27.7	-54.4
0.7	39.4	44.2	32.2	56.8	-38.1	-46.9	-32.2	-61.8
0.8	43.7	49.8	36.8	63.2	-41.1	-53.1	-36.0	-69.5
0.9	47.5	55.2	39.6	69.9	-41.8	-59.4	-38.2	-77.3
1.0	51.3	60.3	42.6	76.3	-46.0	-65.5	-38.7	-85.2
1.1	54.1	65.2	44.8	82.5	-47.8	-71.6	-39.0	-93.0
1.2	56.2	69.9	46.2	88.3	-49.2	-77.6	-39.2	-100.6
1.3	57.9	74.2	47.1	93.8	-50.0	-83.6	-39.4	-108.1
1.4	59.3	78.4	47.4	99.1	-50.5	-89.7	-39.6	-115.5
1.5	60.1	82.3	47.7	103.8	-50.7	-95.5	-39.9	-123.0
1.6	60.5	85.9	48.0	108.4	-51.0	-101.3	-40.1	-130.4
1.7	61.0	89.1	48.4	112.1	-51.1	-107.1	-40.2	-136.7
1.8	61.5	92.2	48.9	115.9	-51.3	-112.4	-40.3	-144.2
1.9	62.0	95.3	49.1	119.6	-51.5	-118.7	-40.4	-150.5
2.0	62.5	97.2	49.4	123.3	-51.6	-124.0	-40.5	-156.9
2.1	62.9	99.1	49.6	126.5	-51.8	-129.3	-40.6	-163.2
2.2	63.3	100.9	49.8	129.5	-52.0	-134.6	-40.7	-169.6
2.3	63.8	101.9	49.9	132.4	-52.2	-139.9	-40.8	-176.0
2.4	64.1	102.8	50.0	135.0	-52.3	-145.2	-40.9	-181.3
2.5	64.6	103.8	50.2	137.3	-52.5	-150.5	-41.0	-187.6
2.6	64.8	104.6	50.4	139.2	-52.7	-155.3	-41.1	-192.9
2.7	65.0	105.4	50.5	140.8	-52.8	-160.1	-41.2	-198.2

Table 8. Full Strength Driver Characteristics

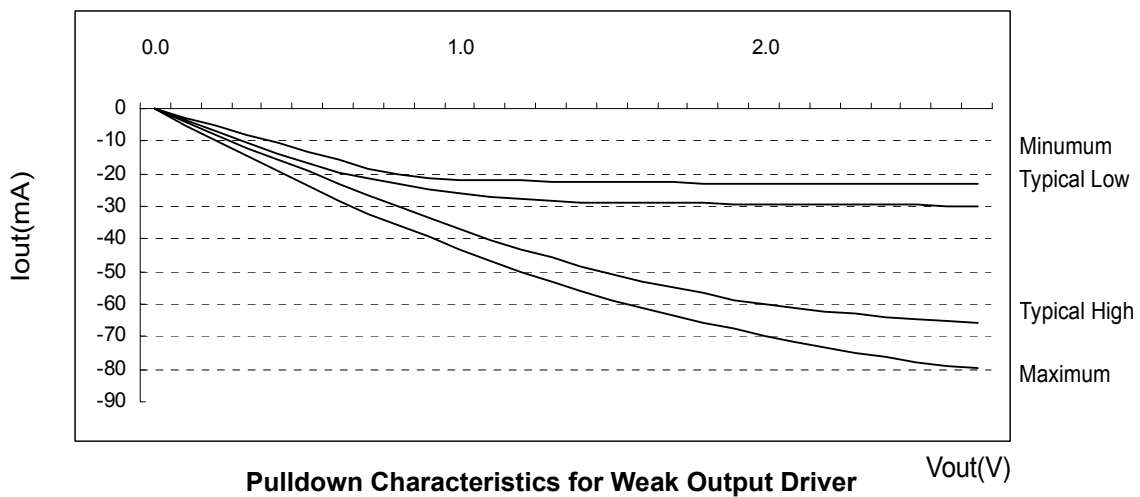
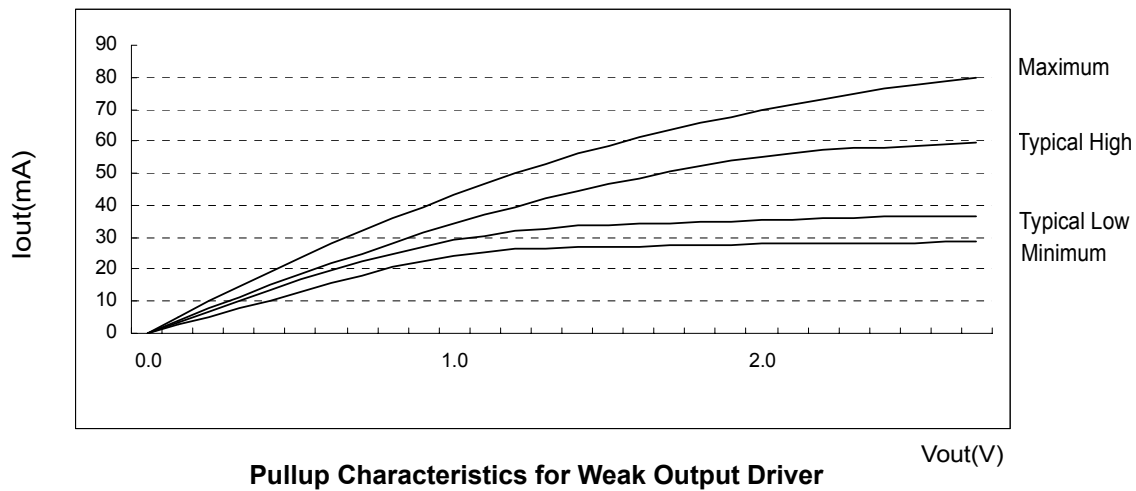


Figure 4. I/V characteristics for input/output buffers: Pull up (above) and pull down (below)

Voltage (V)	Pulldown Current (mA)				pullup Current (mA)			
	Typical Low	Typical High	Minimum	Maximum	Typical Low	Typical High	Minimum	Maximum
0.1	3.4	3.8	2.6	5.0	-3.5	-4.3	-2.6	-5.0
0.2	6.9	7.6	5.2	9.9	-6.9	-8.2	-5.2	-9.9
0.3	10.3	11.4	7.8	14.6	-10.3	-12.0	-7.8	-14.6
0.4	13.6	15.1	10.4	19.2	-13.6	-15.7	-10.4	-19.2
0.5	16.9	18.7	13.0	23.6	-16.9	-19.3	-13.0	-23.6
0.6	19.6	22.1	15.7	28.0	-19.4	-22.9	-15.7	-28.0
0.7	22.3	25.0	18.2	32.2	-21.5	-26.5	-18.2	-32.2
0.8	24.7	28.2	20.8	35.8	-23.3	-30.1	-20.4	-35.8
0.9	26.9	31.3	22.4	39.5	-24.8	-33.6	-21.6	-39.5
1.0	29.0	34.1	24.1	43.2	-26.0	-37.1	-21.9	-43.2
1.1	30.6	36.9	25.4	46.7	-27.1	-40.3	-22.1	-46.7
1.2	31.8	39.5	26.2	50.0	-27.8	-43.1	-22.2	-50.0
1.3	32.8	42.0	26.6	53.1	-28.3	-45.8	-22.3	-53.1
1.4	33.5	44.4	26.8	56.1	-28.6	-48.4	-22.4	-56.1
1.5	34.0	46.6	27.0	58.7	-28.7	-50.7	-22.6	-58.7
1.6	34.3	48.6	27.2	61.4	-28.9	-52.9	-22.7	-61.4
1.7	34.5	50.5	27.4	63.5	-28.9	-55.0	-22.7	-63.5
1.8	34.8	52.2	27.7	65.6	-29.0	-56.8	-22.8	-65.6
1.9	35.1	53.9	27.8	67.7	-29.2	-58.7	-22.9	-67.7
2.0	35.4	55.0	28.0	69.8	-29.2	-60.0	-22.9	-69.8
2.1	35.6	56.1	28.1	71.6	-29.3	-61.2	-23.0	-71.6
2.2	35.8	57.1	28.2	73.3	-29.5	-62.4	-23.0	-73.3
2.3	36.1	57.7	28.3	74.9	-29.5	-63.1	-23.1	-74.9
2.4	36.3	58.2	28.3	76.4	-29.6	-63.8	-23.2	-76.4
2.5	36.5	58.7	28.4	77.7	-29.7	-64.4	-23.2	-77.7
2.6	36.7	59.2	28.5	78.8	-29.8	-65.1	-23.3	-78.8
2.7	36.8	59.6	28.6	79.7	-29.9	-65.8	-23.3	-79.7

Table 9. Weak Driver Characteristics