DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD30181A, 30181AY

VR4181A™
64-/32-BIT MICROPROCESSOR

DESCRIPTION

The μPD30181A and 30181AY (VR4181A), which are high-performance 64-/32-bit microprocessors employing the RISC (reduced instruction set computer) architecture developed by MIPS™, are products in the VR Series™ of microprocessors manufactured by NEC.

The VR4181A includes as its CPU the VR4120™ core, an ultra-low-power-consumption core featuring cache memory, a high-speed product-sum operation unit, and a memory management unit. Other on-chip components include an LCD controller, CompactFlash controller, USB host/function controller, DMA controller, SDRAM controller, PWM controller, AC97/I²S audio interface, full-duplex asynchronous serial interface, IrDA interface, I²C serial interface, keyboard interface, touch panel interface, real-time clock, A/D converter, D/A converter, and other controllers and interfaces required for battery-driven mobile information devices, fixed compact information devices, car navigation systems, and compact embedded devices.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

- **VR4181A Hardware User's Manual (U16049E)**
- **VR4100 Series™ Architecture User's Manual (U15509E)**

FEATURES

- VR4120 core (64-bit RISC core) on chip as CPU
- Pipeline clock: 131 MHz
- Conforms to MIPS III (except for FPU, LL and SC instructions) and MIPS16 instruction sets
- Supports MACC and DMACC high-speed product-sum operation instructions
- On-chip cache memory
  Capacity includes 8 KB instruction cache and 8 KB data cache
- Employs a writeback cache
- Physical addresses: 32 bits
  Virtual addresses: 40 bits
- On-chip 32 double-entry TLB
- Effective power management using four modes: Fullspeed, Standby, Suspend, and Hibernate
- Employs a high-performance internal system bus (T-bus)
- DRAM controller supporting 64 Mb, 128 Mb, and 256 Mb SDRAMs
- External system bus interface supporting ROM, page ROM, flash memory, SRAM, ISA devices, IDE (ATA) devices, and SyncFlash™ memory
- UMA type LCD controller (supports STN and TFT panels)
- ExCA register-compatible CompactFlash interface (2 slots)
- USB host controller (Rev1.1, OHCI Rev1.0) controller
- USB function (Rev1.1) controller
- AC97 and I²S audio interfaces (1 channel each)
- Clocked serial interface (1 channel)
- NS16550-compatible serial interface (3 channels)
- IrDA (SIR) interface (1 channel)
- I²C bus interfaces (2 channels, μPD30181AY only)
- PWM controller (3 channels)
- DMA controller supporting chain mode (4 channels)
- Keyboard scan interface (supports 8 × 12 key matrix)
- X-Y coordinate auto scan touch panel interface
- On-chip A/D converter and D/A converter
- On-chip watchdog timer unit
- RTC unit (total of 3 timer and counter channels)
- On-chip PLL and clock generators
- Power supplies: 2.5 V for core, 3.3 V for I/O block
- Package: 240-pin plastic FBGA

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The mark ★ shows major revised points.

APPLICATIONS

- Car navigation systems
- Digital consumer devices (digital information home equipment)
- Battery-driven mobile information devices
- Controllers for embedded devices

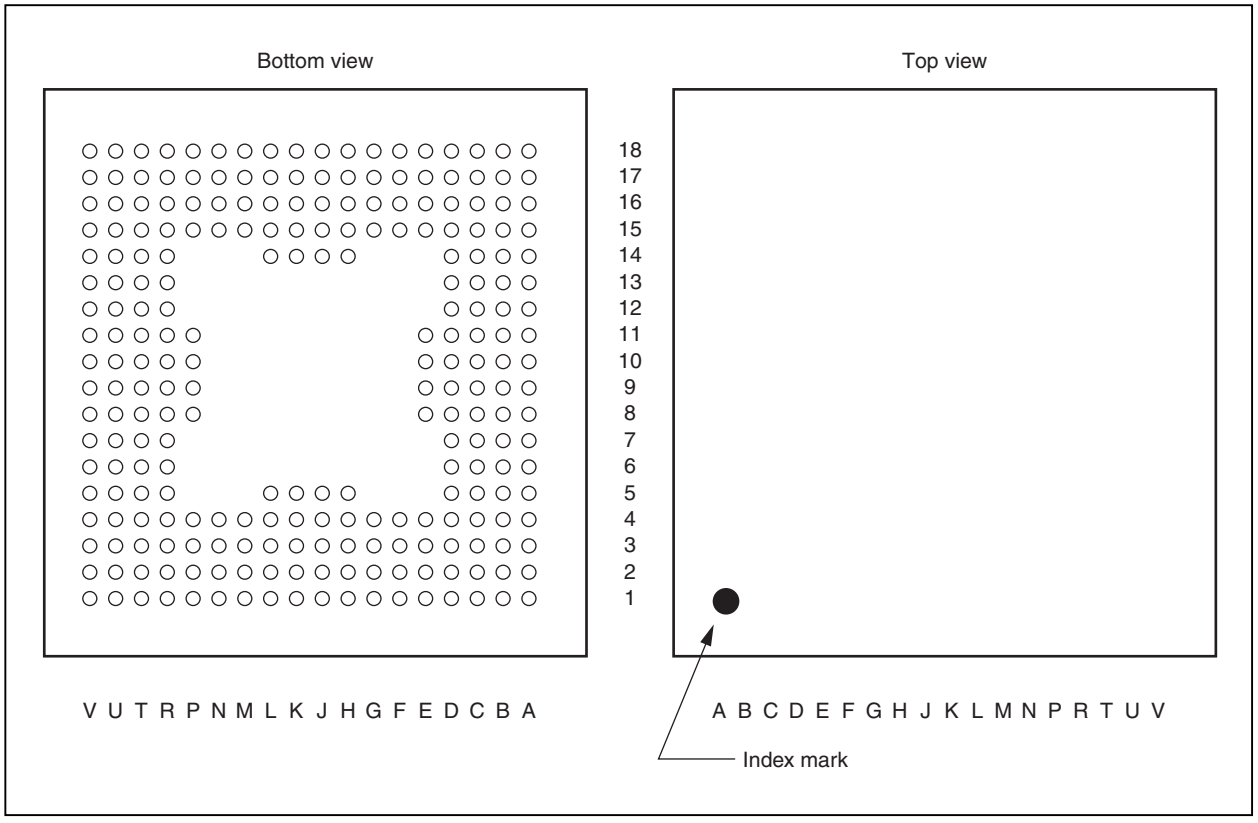
ORDERING INFORMATION

Part Number	Package	I^2C Bus Interface	Internal Maximum Operating Frequency
μPD30181AF1-131-GA3	240-pin plastic FBGA (16 × 16)	None	131 MHz
μPD30181AF1-131-GA3-A[Note]	240-pin plastic FBGA (16 × 16)	None	131 MHz
μPD30181AYF1-131-GA3	240-pin plastic FBGA (16 × 16)	On chip	131 MHz
μPD30181AYF1-131-GA3-A[Note]	240-pin plastic FBGA (16 × 16)	On chip	131 MHz

Note Lead-free product

PIN CONFIGURATION

- 240-pin plastic FBGA (16 × 16)



(1/3)

No.	Power Supply	Name	No.	Power Supply	Name
A1	3.3 V	D6	C5	3.3 V	D26
A2	3.3 V	D5	C6	3.3 V	D24
A3	3.3 V	D3	C7	3.3 V	D23
A4	3.3 V	D1	C8	3.3 V	D22
A5	3.3 V	D8	C9	3.3 V	D20
A6	3.3 V	D10	C10	3.3 V	D18
A7	3.3 V	D12	C11	3.3 V	UHDP
A8	3.3 V	D14	C12	3.3 V	UOC
A9	3.3 V	D16	C13	3.3 V	NMI#
A10	3.3 V	D17	C14	3.3 V	DQM2/LBE2#
A11	3.3 V	UDP	C15	3.3 V	PCS0#
A12	3.3 V	CLK48	C16	3.3 V	SYSEN#
A13	3.3 V	SDCS2#	C17	3.3 V	IORDY
A14	3.3 V	SDCS3#	C18	3.3 V	UBE#
A15	3.3 V	MEMWR#	D1	3.3 V	CAS#
A16	3.3 V	PCS4#	D2	3.3 V	RAS#
A17	3.3 V	PCS1#	D3	3.3 V	D29
A18	3.3 V	IORD#	D4	2.5 V	VDD2
B1	3.3 V	D7	D5	3.3 V	D25
B2	3.3 V	DQM1/LBE1#	D6	2.5 V	GND2
B3	3.3 V	D4	D7	2.5 V	VDD2
B4	3.3 V	D2	D8	3.3 V	D21
B5	3.3 V	D0	D9	3.3 V	D19
B6	3.3 V	D9	D10	3.3 V	GNDU
B7	3.3 V	D11	D11	3.3 V	VDDU
B8	3.3 V	D13	D12	3.3 V	GND3
B9	3.3 V	D15	D13	3.3 V	VDD3
B10	3.3 V	UDN	D14	2.5 V	GND2
B11	3.3 V	UHDN	D15	3.3 V	MEMRD#
B12	3.3 V	UPON	D16	3.3 V	PWM1/KSCAN6/GPIO9
B13	3.3 V	DQM3/LBE3#	D17	3.3 V	IOCS16#
B14	3.3 V	PCS3#	D18	3.3 V	PWM0/KSCAN7/GPIO8
B15	3.3 V	ROMCS#	E1	3.3 V	SDCLK
B16	3.3 V	PCS2#	E2	3.3 V	SDCS1#
B17	3.3 V	SYSDIR	E3	3.3 V	D30
B18	3.3 V	IOWR#	E4	3.3 V	VDD3
C1	3.3 V	DQM0/LBE0#	E8	3.3 V	VDD3
C2	3.3 V	WE#	E9	3.3 V	GND3
C3	3.3 V	D28	E10	2.5 V	GND2
C4	3.3 V	D27	E11	2.5 V	VDD2

Remark # indicates active low.

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No.	Power Supply	Name	No.	Power Supply	Name
E15	3.3 V	VDD3	K2	3.3 V	A12
E16	3.3 V	KPORT0/GPIO4	K3	3.3 V	A19/GPIO58
E17	3.3 V	PWM2/KSCAN5/GPIO10	K4	3.3 V	A20/GPIO59
E18	3.3 V	KPORT1/GPIO5	K5	3.3 V	VDD3
F1	3.3 V	SDCS0#	K14	3.3 V	VDD3
F2	3.3 V	CKE0	K15	3.3 V	SO/KSCAN9/GPIO21
F3	3.3 V	D31	K16	3.3 V	SCK/KSCAN11/GPIO23
F4	3.3 V	GND3	K17	3.3 V	FRM/KSCAN8/GPIO20
F15	2.5 V	GNDP	K18	3.3 V	CF1_VCCEN#/KSCAN4/GPIO37
F16	3.3 V	CF1_DIR/KPORT4/GPIO39	L1	3.3 V	A11
F17	3.3 V	KPORT2/GPIO6	L2	3.3 V	A9
F18	3.3 V	CLKX1	L3	3.3 V	A17/GPIO56
G1	3.3 V	A13	L4	3.3 V	A18/GPIO57
G2	3.3 V	A14	L5	2.5 V	VDD2
G3	3.3 V	TC0#/GPIO52	L14	2.5 V	GND2
G4	3.3 V	TC1#/GPIO53	L15	3.3 V	JTMS
G15	2.5 V	VDDP	L16	3.3 V	JTDO
G16	3.3 V	KPORT3/GPIO7	L17	3.3 V	SI/KSCAN10/GPIO22
G17	3.3 V	CF1_EN#/KPORT5/GPIO38	L18	3.3 V	JTCK
G18	3.3 V	CLKX2	M1	3.3 V	A8
H1	3.3 V	SA10	M2	3.3 V	A7
H2	3.3 V	A0	M3	3.3 V	A15/GPIO54
H3	3.3 V	A23/RP#	M4	3.3 V	A16/GPIO55
H4	3.3 V	A24/CKE1	M15	3.3 V	JTRST#
H5	2.5 V	GND2	M16	3.3 V	CF0_IOIS16#/GPIO34
H14	3.3 V	VDDO	M17	3.3 V	JTDI/RMODE#
H15	3.3 V	GNDO	M18	3.3 V	BKTGIO#
H16	3.3 V	KSCAN0/GPIO0	N1	3.3 V	A6
H17	3.3 V	KSCAN3/GPIO3	N2	3.3 V	A5
H18	3.3 V	RTCX2	N3	3.3 V	A10
J1	3.3 V	A1	N4	2.5 V	GND2
J2	3.3 V	A2	N15	2.5 V	VDD2
J3	3.3 V	A21/GPIO60	N16	3.3 V	CF0_CD2#/GPIO36
J4	3.3 V	A22/GPIO61	N17	3.3 V	CF0_CD1#/GPIO35
J5	3.3 V	GND3	N18	3.3 V	CF_WAIT#/GPIO33
J14	2.5 V	VDD2	P1	3.3 V	A4
J15	3.3 V	GND3	P2	3.3 V	DAK1#
J16	3.3 V	KSCAN1/GPIO1	P3	3.3 V	DRQ1#
J17	3.3 V	KSCAN2/GPIO2	P4	3.3 V	GNDAD
J18	3.3 V	RTCX1	P8	2.5 V	VDD2
K1	3.3 V	A3	P9	2.5 V	GND2

Remark # indicates active low.

(3/3)

No.	Power Supply	Name	No.	Power Supply	Name
P10	2.5 V	GND2	T16	3.3 V	FPD2
P11	3.3 V	GND3	T17	3.3 V	I.C. (GND3)[Note 2]
P15	3.3 V	CF0_CE2#/GPIO32	T18	3.3 V	CF0_EN#/GPIO26
P16	3.3 V	CF0_DIR/GPIO27	U1	3.3 V	MPOWER
P17	3.3 V	CF0_READY/GPIO29	U2	3.3 V	AIN0
P18	3.3 V	CF0_CE1#/GPIO31	U3	3.3 V	TPX0
R1	3.3 V	DRQ0#	U4	3.3 V	TPY0
R2	3.3 V	POWER	U5	3.3 V	TxD0/CLKSEL2[Note 1]
R3	3.3 V	RSTSW#	U6	3.3 V	RTS0#/GPIO19/CLKSEL1[Note 1]
R4	3.3 V	GNDTP	U7	3.3 V	RxD2/IRDIN
R5	3.3 V	VDDTP	U8	3.3 V	CTS2#/BITCLK/SCLK
R6	3.3 V	VDDAD	U9	3.3 V	I.C. (GND3)[Note 2]
R7	3.3 V	VDD3	U10	3.3 V	SCL0/KPORT7/GPIO12
R8	3.3 V	GND3	U11	3.3 V	VSYNC/FLM/BMODE1[Note 1]
R9	3.3 V	DCD2#/SDATAIN/SDI	U12	3.3 V	FPD15/CF1_READY/GPIO51
R10	3.3 V	SDA0/KPORT6/GPIO11	U13	3.3 V	FPD12/CF1_CE1#/GPIO48
R11	3.3 V	VPBIAS/GPO63	U14	3.3 V	FPD10/CF1_CD1#/GPIO46
R12	3.3 V	VPLCD/GPO62	U15	3.3 V	FPD6/GPIO42
R13	3.3 V	VDD3	U16	3.3 V	FPD4/GPIO40
R14	2.5 V	VDD2	U17	3.3 V	CF1_RESET/DBUS32[Note 1]
R15	3.3 V	GND3	U18	3.3 V	CF0_VCCEN#/GPIO24
R16	3.3 V	CF_REG#/GPIO25	V1	3.3 V	TPY1
R17	3.3 V	CF0_RESET/GPIO28	V2	3.3 V	AIN1
R18	3.3 V	CF0_STSCHG#/GPIO30	V3	3.3 V	AIN3
T1	3.3 V	RTCRST#	V4	3.3 V	AOUT
T2	3.3 V	POWERON	V5	3.3 V	RxD0
T3	3.3 V	DAK0#	V6	3.3 V	CTS0#/GPIO18
T4	3.3 V	TPX1	V7	3.3 V	DTR0#/RTS1#/GPIO17/CLKSEL0[Note 1]
T5	3.3 V	AIN2	V8	3.3 V	TxD2/IRDOUT/MIPS16EN[Note 1]
T6	3.3 V	DCD0#/GPIO16	V9	3.3 V	DSR2#/SRESET#
T7	3.3 V	DSR0#/CTS1#/GPIO15	V10	3.3 V	RxD1/SCL1/GPIO14
T8	3.3 V	RTS2#/SYNC/WS/DIVMODE1[Note 1]	V11	3.3 V	DCLK/SHCLK
T9	3.3 V	DTR2#/SDATAOUT/SDO/DIVMODE0[Note 1]	V12	3.3 V	HSYNC/LOCLK/NWIREEN[Note 1]
T10	3.3 V	TxD1/SDA1/GPIO13	V13	3.3 V	FPD11/CF1_CD2#/GPIO47
T11	3.3 V	ENAB/M/BMODE0[Note 1]	V14	3.3 V	FPD9/GPIO45
T12	3.3 V	FPD14/CF1_STSCHG#/GPIO50	V15	3.3 V	FPD7/GPIO43
T13	3.3 V	FPD13/CF1_CE2#/GPIO49	V16	3.3 V	FPD5/GPIO41
T14	3.3 V	FPD8/GPIO44	V17	3.3 V	FPD3
T15	3.3V	FPD0	V18	3.3 V	FPD1

Notes 1. These pins are used for mode settings. A mode setting is made according to the status of these pins at the rising edge of the RTCRST# signal. Use pull-up/pull-down resistors to set the pin statuses.

2. Be sure to connect these pins to GND3.

Remark # indicates active low.

PIN INDENTIFICATION (1/2)

A(24:0):	Address bus
AIN(3:0):	Analog data Input
AOUT:	Analog data output
BITCLK:	AC97 bit clock
BKTGIO#:	N-wire break trigger I/O
BMODE(1:0):	Boot mode
CAS#:	SDRAM column address strobe
CF_REG#:	CompactFlash register memory access
CF_WAIT#:	CompactFlash wait input
CF0_CD(2:1)#:	CompactFlash card detect
CF0_CE(2:1)#:	CompactFlash card enable
CF0_DIR:	CompactFlash data direction
CF0_EN#:	CompactFlash buffer enable
CF0_IOIS16#:	CompactFlash I/O is 16 bits
CF0_READY:	CompactFlash ready
CF0_RESET:	CompactFlash reset
CF0_STSCHG#:	CompactFlash status change
CF0_VCCEN#:	CompactFlash V_{CC} enable
CF1_CD(2:1)#:	CompactFlash card detect
CF1_CE(2:1)#:	CompactFlash card enable
CF1_DIR:	CompactFlash data direction
CF1_EN#:	CompactFlash buffer enable
CF1_READY:	CompactFlash ready
CF1_RESET:	CompactFlash reset
CF1_STSCHG#:	CompactFlash status change
CF1_VCCEN#:	CompactFlash V_{CC} enable
CKE0:	SDRAM Clock enable
CKE1:	SyncFlash memory clock enable
CLK48:	USB clock input
CLKSEL(2:0):	Pipeline clock select
CLKX(2:1):	Clock input
CTS0#, CTS1#, CTS2#:	16550 clear to send
D(31:0):	Data bus
DAK(1:0)#:	DMA acknowledge
DBUS32:	ROM data bus mode
DCD0#, DCD2#:	16550 data carrier detect
DCLK:	TFT dot clock
DIVMODE(1:0):	Divide-by mode
DQM(3:0):	SDRAM byte enable
DRQ(1:0)#:	DMA request
DSR0#, DSR2#:	16550 data set ready
DTR0#, DTR2#:	16550 data terminal ready
ENAB:	TFT display enable
FLM:	STN first line clock
FPD(15:0):	LCD display data
FRM:	CSI frame input
GND2:	Internal ground
GND3:	I/O ground
GNDAD:	A/D and D/A converter ground
GNDO:	Oscillator ground
GNDP:	PLL ground
GNDTP:	Touch panel ground
GNDU:	USB transceiver ground
GPIO(61:0):	General-purpose I/O
GPO(63:62):	General-purpose output
HSYNC:	TFT horizontal sync
I.C.:	Internally connected
IOCS16#:	I/O 16-bit bus sizing
IORD#:	I/O read
IORDY:	I/O ready
IOWR#:	I/O write
IRDIN:	IrDA data input
IRDOUT:	IrDA data output
JTCK:	N-wire clock
JTDI:	N-wire data input
JTDO:	N-wire data output
JTMS:	N-wire mode select
JTRST#:	N-wire reset
KPORT(7:0):	Key Scan input
KSCAN(11:0):	Key Scan output
LOCLK:	STN load clock
LBE(3:0)#:	System bus byte enable
M:	STN modulation clock
MEMRD#:	Memory read
MEMWR#:	Memory write
MIPS16EN:	MIPS16 enable
MPOWER:	Main power control
NMI#:	Non maskable interrupt

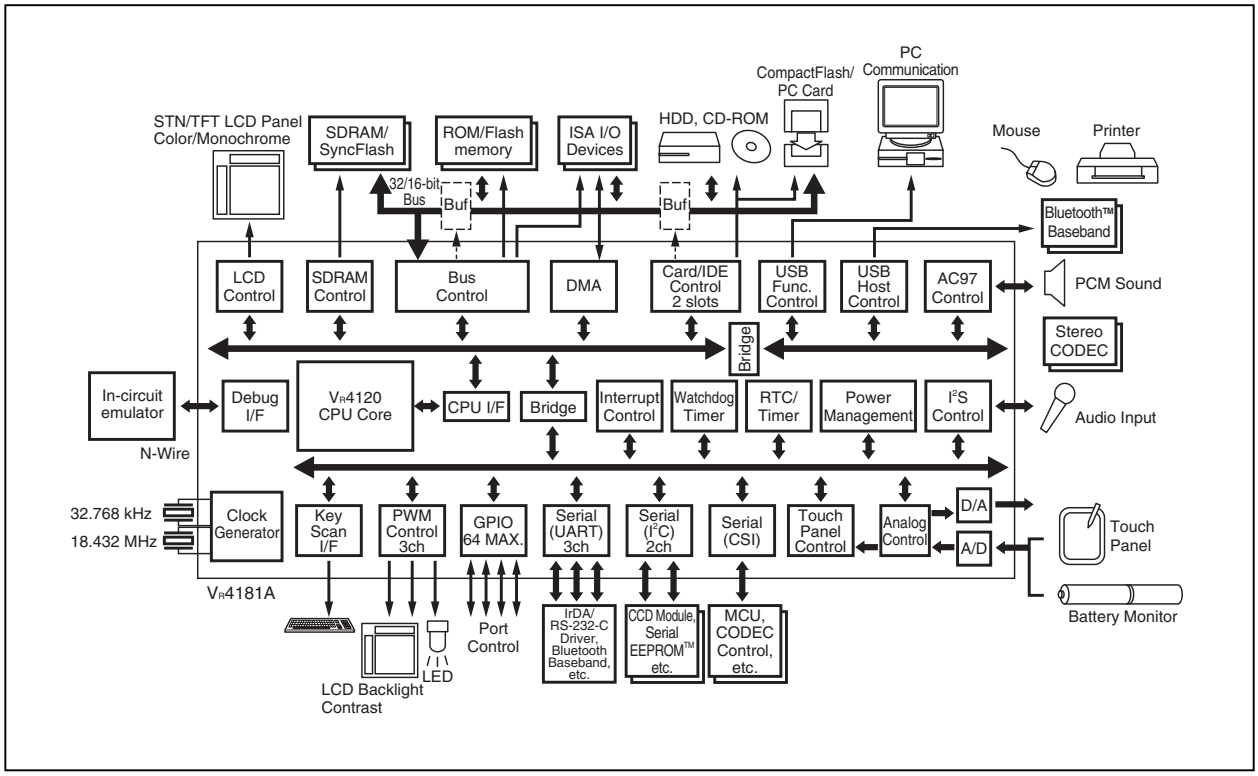
Remark # indicates active low.

PIN INDENTIFICATION (2/2)

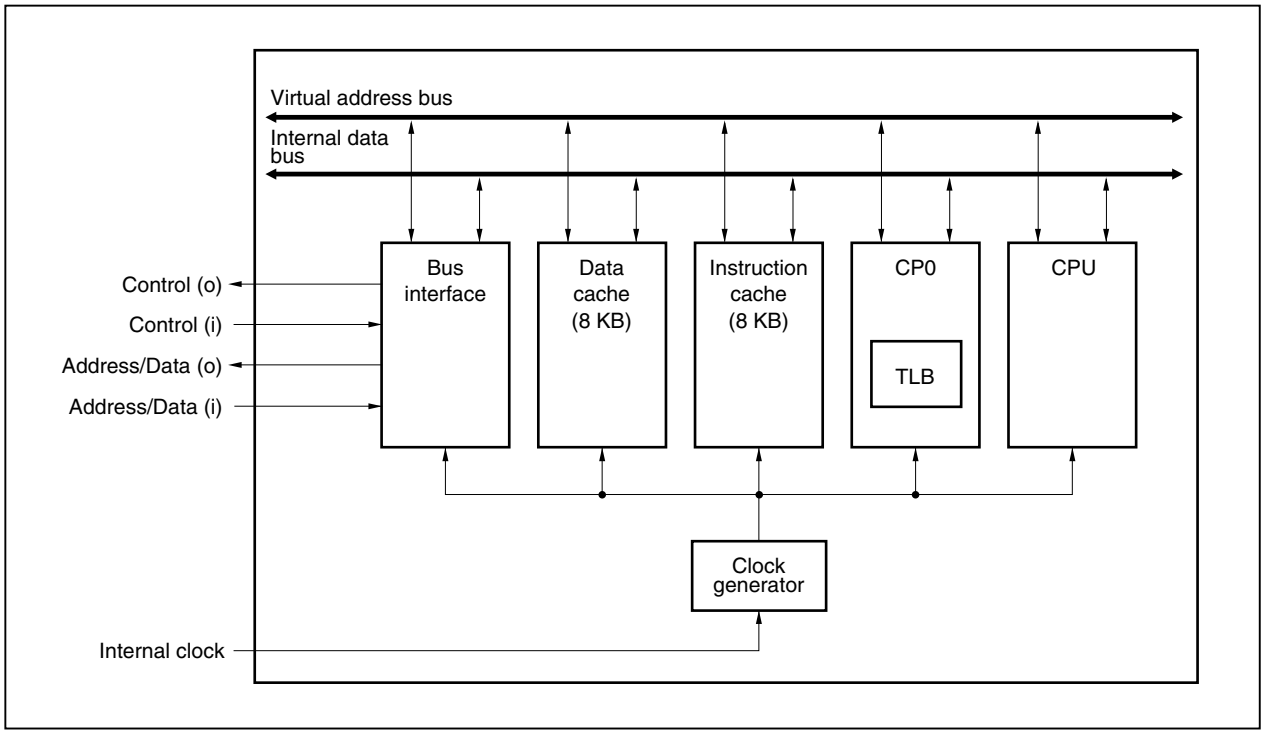
NWIREEN:	N-Wire enable	SO:	CSI data output
PCS(4:0)#:	Programmable chip select	SRESET#:	AC97 reset
POWER:	Power switch	SYNC:	AC97 synchronous clock
POWERON:	Power on state	SYSDIR:	System data direction
PWM(2:0):	Pulse width modulation	SYSEN#:	System data enable
RAS#:	SDRAM row address strobe	TC(1:0)#:	Terminal counter
RMODE#:	N-wire reset mode select	TPX(1:0):	Touch panel X coordinate data
ROMCS#:	Chip select for ROM	TPY(1:0):	Touch panel Y coordinate data
RP#:	SyncFlash memory reset/power-down	TxD0, TxD1, TxD2:	16550 transmit data
		UBE#:	Upper byte enable for system bus
RSTSW#:	Reset switch	UDN:	USB function negative data
RTCRST#:	Real-time clock reset	UDP:	USB function positive data
RTCX(2:1):	Real-time clock input	UHDN:	USB host negative data
RTS0#, RTS1#, RTS2#:	16550 data request to send	UHDP:	USB host positive data
RxD0, RxD1, RxD2:	16550 receive data	UOC:	USB host root hub port over current
SA10:	SDRAM address 10-bit	UPON:	USB host root hub port power control
SCLK:	I^2S continuous clock	VDD2:	Internal power supply
SCL1, SCL0:	I^2C clock	VDD3:	I/O power supply
SCK:	CSI serial clock	VDDAD:	A/D and D/A converter power supply
SDA1, SDA0:	I^2C data	VDDO:	Oscillator power supply
SDATAIN:	AC97 serial codec data input	VDDP:	PLL power supply
SDATAOUT:	AC97 serial codec data output	VDDTP:	Touch panel power supply
SDCLK:	SDRAM clock	VDDU:	USB transceiver power supply
SDCS(3:2)#:	SyncFlash memory chip select	VPBIAS:	Bias power control
SDCS(1:0)#:	SDRAM chip select	VPLCD:	Logic power control
SDI:	I^2S serial codec data input	VSYNC:	TFT vertical sync
SDO:	I^2S serial codec data output	WE#:	SDRAM write enable
SHCLK:	STN shift clock	WS:	I^2S word select
SI:	CSI data input		

Remark # indicates active low.

INTERNAL BLOCK DIAGRAM AND EXAMPLE OF CONNECTION OF EXTERNAL BLOCKS



CPU CORE INTERNAL BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

Remark # indicates active low.

1.1 Pin Functions

(1) System bus interface signals

(1/3)

Signal Name	I/O	Function	Alternate Function
A24	O	Address bus These pins are used to specify system bus addresses. They are used to access ROM, flash memory, SRAM, ISA devices, PC Cards, IDE (ATA) devices, and general-purpose devices.	CKE1
A23	O		RP#
A(22:15)	O		GPIO(61:54)
SA10	O	Address bit 10 for SDRAM or SyncFlash memory Instead of connecting to A10, connect this pin (SA10) to address bit 10 in SDRAM or SyncFlash memory.	–
A(14:0)	O	Address bus These pins are used to specify system bus addresses. They are used to access SDRAM, SyncFlash memory, ROM, flash memory, SRAM, ISA devices, CompactFlash/PC Cards, IDE (ATA) devices, and general-purpose devices.	–
D(31:0)	I/O	Data bus These pins are used to transfer data to the VR4181A and SDRAM, SyncFlash memory, ROM, flash memory, SRAM, ISA devices, CompactFlash/PC Cards, IDE (ATA) devices, and general-purpose devices.	–
PCS(4:0)#	O	Programmable chip select These pins can be set as active when the VR4181A accesses ROM, flash memory, SRAM, and general-purpose devices. They can be connected only to devices that are not subject to bus sizing via the IOCS16# pin.	–
ROMCS#	O	Boot ROM chip select This pin can be set as active when the VR4181A accesses boot ROM or flash memory. When the BMODE(1:0) pin status is 01 and the RTCRST# signal has been cleared, the VR4181A fetches the boot code from a device connected to the ROMCS# pin to activate this pin.	–
MEMRD#	O	System bus memory read This pin becomes active when the VR4181A reads data from any of the following devices. • ROM, flash memory, SRAM, or general-purpose devices controlled by the ROMCS# pin or PCS# pin • External ISA bus memory space devices and CompactFlash/PC Card memory space devices	–

(2/3)

Signal Name	I/O	Function	Alternate Function
MEMWR#	O	System bus memory write This pin becomes active when the VR4181A writes to any of the following devices. • ROM, flash memory, SRAM, or general-purpose devices controlled by the ROMCS# pin or PCS# pin • External ISA bus memory space devices and CompactFlash/PC Card memory space devices	–
IORD#	O	System bus I/O read This pin becomes active when the VR4181A reads data from the external ISA bus I/O space devices or CompactFlash/PC Card I/O ports. It is valid only when accessing the external ISA bus I/O space.	–
IOWR#	O	System bus I/O write This pin becomes active when the VR4181A writes data to external ISA bus I/O space devices or CompactFlash/PC Card I/O ports. It is valid only when accessing the external ISA bus I/O space.	–
IORDY	I	System bus I/O channel ready This pin (IORDY) is set as inactive in relation to read/write strobes from the VR4181A in order to extend the access time for a device connected to the system bus. It is set as active once the device is in a mode that supports access from the VR4181A. It can be used to access a device connected to the ROMCS# pin or PCS# pin or a device connected to the external ISA space.	–
IOCS16#	I	System bus sizing request Set this signal as active when an ISA device connected to the system bus accesses data in 16-bit width. Bus sizing that uses this pin IOCS16# is enabled only when accessing the external ISA space.	–
UBE#	O	System bus higher byte enable This pin becomes active during system bus access if the higher bytes of the 16-bit data bus are valid. It can be used if a device connected to the ROMCS# or PCS# pin or a device connected to the external ISA space uses 16-bit width.	–
LBE(3:0)#	O	System bus byte enable The LBE(3:0)# signal pins used for 32-bit general-purpose devices are shared as the DQM(3:0) signal pins for SDRAM and SyncFlash memory, so the function of this pin changes based on time division. When the VR4181A accesses a device that uses the ROMCS# pin or PCS# pin, the LBE(3:0)# signals become valid only when the SYSEN# signal is at low level. This signal indicates the data bus's valid byte lane. If the device connected to the ROMCS# pin or PCS# pin has 32-bit width, this pin can be used. When the SYSEN# pin is at high level, this pin operates as the DQM(3:0) pins that are referenced by SDRAM.	DQM(3:0)

(3/3)

Signal Name	I/O	Function	Alternate Function
SYSDIR[Note]	O	Data bus isolation buffer direction control This signal is valid only when accessing devices other than SDRAM or SyncFlash memory devices. The signal is at high level during read cycles and at low level during write cycles.	–
SYSEN#[Note]	O	Enables data bus isolation buffer connection This signal is set to high level during SDRAM and SyncFlash memory cycles and is at low level when accessing any other devices.	–
DRQ(1:0)#	I	DMA service request signal The DRQ(1:0)# signals are sampled at the rising edge of TClock. Be sure to hold this signal at active level until a DMA request is acknowledged. Set this signal as inactive when not using the DRQ(1:0)# signals.	–
DAK(1:0)#	O	Enables DMA service request This signal goes to active level when access to the target device occurs via DMA transfer.	–
TC(1:0)#	I/O	DMA transfer completion signal (open drain) This signal is driven at active level when a DMA transfer is completed. During a transfer, this signal operates as a DMA stop request input signal.	GPIO(53:52)
NMI#	I	Non-maskable interrupt input This is an interrupt request signal that cannot be masked in relation to the CPU core. When the VR4181A starts normally and the MPOWER signal is at high level, input from the NMI# pin is connected to the CPU core via the ICU. While the MPOWER signal is at low level, input to the NMI# pin is monitored by the PMU as a source of NMI shutdowns.	–

Note The SYSEN# and SYSDIR signals are buffer control signals used to isolate the SDRAM and SyncFlash memory buses from other low-speed device buses. Isolating high-speed memory access paths from other devices reduces the load on the system bus between the VR4181A and the SDRAM or SyncFlash memory. When using the system bus isolation buffer, the correspondence between the SYSEN# and SYSDIR signals and the data bus isolation status is as shown below.

SYSEN#	SYSDIR	Bus Operation
0	0	Enables connection via data bus isolation buffer • Write cycle for ROM, flash memory, SRAM, ISA device, CompactFlash/PC Card, or other general-purpose device • Hibernate mode
0	1	Enables connection via data bus isolation buffer • Read cycle for ROM, flash memory, SRAM, ISA device, CompactFlash/PC Card, or general-purpose device
1	0	Disables connection via data bus isolation buffer Read/write cycle for SDRAM or SyncFlash memory

(2) Memory interface signals

Signal Name	I/O	Function	Alternate Function
SDCLK	O	Operating clock for SDRAM and SyncFlash memory This signal can also be set (via register settings) to stop clock output when not accessing SDRAM or SyncFlash memory.	–
CKE1	O	Operating clock enable signal for SyncFlash memory	A24
CKE0	O	Operating clock enable signal for SDRAM	–
SDCS(3:2)#	O	Chip select signal for SyncFlash memory	–
SDCS(1:0)#	O	Chip select signal for SDRAM	–
RAS#	O	Row address strobe signal for SDRAM and SyncFlash memory	–
CAS#	O	Column address strobe signal for SDRAM and SyncFlash memory	–
DQM(3:0)	O	Byte enable signal for SDRAM and SyncFlash memory The DQM(3:0) signals for SDRAM and SyncFlash memory shares pins with the LBE(3:0)# signals for 32-bit general-purpose devices, so the function of these pins change based on time division. When the SYSEN# signal is at high level, the pin operates as the DQM(3:0) signals which are referenced by SDRAM.	LBE(3:0)#
WE#	O	Write enable signal for SDRAM and SyncFlash memory	–
RP#	O	SyncFlash memory initialization/power down signal	A23

(3) Initialization interface signals

Signal Name	I/O	Function	Alternate Function
POWER	I	VR4181A activation request (power switch) signal When the rising edge of this signal is detected in Hibernate mode, an activation factor occurs (the VR4181A restores to Fullspeed mode).	–
RSTSW#	I	VR4181A reset signal This signal initializes the internal statuses of all resettable devices except the RTC timer, PMU, GIU, and PWMU channels 0 and 1.	–
RTCRST#	I	VR4181A RTC reset signal This signal initializes the internal statuses of all resettable devices, including the RTC timer. When supplying power to a device for the first time, be sure to set this signal as active for external circuits.	–
POWERON	O	VR4181A activation indication When an activation factor has been detected, this signal becomes active (high level) for a specified amount of time.	–
MPOWER	O	VR4181A operation in progress indication When 2.5 V circuits are operating, this signal becomes active (high level). In Hibernate mode, it is inactive (low level). When this signal is inactive, the 2.5 V power supply can be stopped.	–

Remarks 1. Activation factors are used to restore from Hibernate mode to Fullspeed mode.

2. For further description of the operation of initialization interface signals, see **Hardware User's Manual**.

(4) Clock interface signals

Signal Name	I/O	Function	Alternate Function
RTCX(2:1)	–	32.768 kHz crystal resonator connection pin	–
CLKX(2:1)	–	18.432 MHz crystal resonator connection pin	–

(5) LCD interface signals

Signal Name	I/O	Function	Alternate Function
DCLK/SHCLK	O	Dot clock (DCLK) for TFT/shift clock (SHCLK) for STN	–
HSYNC/LOCLK	O	Horizontal sync signal for TFT/load clock for STN	NWIREEN
VSYNC/FLM	O	Vertical sync signal for TFT/first line clock for STN	BMODE1
ENAB/M	O	Display enable signal for TFT/M clock for STN	BMODE0
FPD15	O	LCD display data	CF1_READY, GPIO51
FPD14	O	LCD display data	CF1_STSCHG#, GPIO50
FPD(13:12)	O	LCD display data	CF1_CE(2:1)#, GPIO(49:48)
FPD(11:10)	O	LCD display data	CF1_CD(2:1)#, GPIO(47:46)
FPD(9:4)	O	LCD display data	GPIO(45:40)
FPD(3:0)	O	LCD display data	–
VPBIAS	O	LED bias power control This signal can be used as a general-purpose output when not using the LCD controller.	GPO63
VPLCD	O	LCD logic power control This signal can be used as a general-purpose output when not using the LCD controller.	GPO62

Caution The connection between the FPD(15:0) of the VR4181A and LCD panel data line corresponds to the panel data width, as shown below.

VR4181A	STN Panel Data (4 Bits)	STN Panel Data (8 Bits)	TFT Panel Data (12 Bits)	TFT Panel Data (16 Bits)
FPD0	Data line 0	Data line 0	Data line (B0)	Data line (B0)
FPD1	Data line 1	Data line 1	Data line (B1)	Data line (B1)
FPD2	Data line 2	Data line 2	Data line (B2)	Data line (B2)
FPD3	Data line 3	Data line 3	Data line (B3)	Data line (B3)
FPD4	–	Data line 4	Data line (G0)	Data line (B4)
FPD5	–	Data line 5	Data line (G1)	Data line (G0)
FPD6	–	Data line 6	Data line (G2)	Data line (G1)
FPD7	–	Data line 7	Data line (G3)	Data line (G2)
FPD8	–	–	Data line (R0)	Data line (G3)
FPD9	–	–	Data line (R1)	Data line (G4)
FPD10	–	–	Data line (R2)	Data line (G5)
FPD11	–	–	Data line (R3)	Data line (R0)
FPD12	–	–	–	Data line (R1)
FPD13	–	–	–	Data line (R2)
FPD14	–	–	–	Data line (R3)
FPD15	–	–	–	Data line (R4)

(6) CompactFlash/PC Card/IDE (ATA) interface signal

Signal Name	I/O	Function	Alternate Function
CF1_CD(2:1)#	I	CompactFlash/PC Card (slot 1) detection signal	FPD(11:10), GPIO(47:46)
CF1_CE(2:1)#	O	CompactFlash/PC Card (slot 1) enable signal	FPD(13:12), GPIO(49:48)
CF1_STSCHG#	I	CompactFlash/PC Card (slot 1) status change signal	FPD14, GPIO50
CF1_READY	I	CompactFlash/PC Card (slot 1) ready signal	FPD15, GPIO51
CF1_RESET	O	CompactFlash/PC Card (slot 1) reset signal	DBUS32
CF1_DIR	O	CompactFlash/PC Card (slot 1) data bus direction control signal	KPORT4, GPIO39
CF1_EN#	O	CompactFlash/PC Card (slot 1) buffer enable signal	KPORT5, GPIO38
CF1_VCCEN#	O	CompactFlash/PC Card (slot 1) V_{CC} enable signal	KSCAN4, GPIO37
CF0_CD(2:1)#	I	CompactFlash/PC Card (slot 0) detection signal	GPIO(36:35)
CF0_IOIS16#	I	CompactFlash/PC Card (slot 0) I/O 16-bit bus signal	GPIO34
CF_WAIT#	I	CompactFlash/PC Card (slots 0, 1) wait signal	GPIO33
CF0_CE(2:1)#	O	CompactFlash/PC Card (slot 0) enable signal	GPIO(32:31)
CF0_STSCHG#	I	CompactFlash/PC Card (slot 0) status change signal	GPIO30
CF0_READY	I	CompactFlash/PC Card (slot 0) ready signal	GPIO29
CF0_RESET	O	CompactFlash/PC Card (slot 0) reset signal	GPIO28
CF0_DIR	O	CompactFlash/PC Card (slot 0) data bus direction control signal	GPIO27
CF0_EN#	O	CompactFlash/PC Card (slot 0) buffer enable signal	GPIO26
CF_REG#	O	CompactFlash/PC Card (slots 0, 1) register select signal	GPIO25
CF0_VCCEN#	O	CompactFlash/PC Card (slot 0) V_{CC} enable signal	GPIO24

Cautions 1. Be sure to use MEMRD#, MEMWR#, IORD#, and IOWR# respectively as CompactFlash/PC Card access strobe signals OE#, WE#, IORD#, and IOWR#.

2. The CF0_EN#, CF1_EN#, CF0_DIR, and CF1_DIR signals are used to control the buffer that isolates the CompactFlash/PC Card's bus from other device's buses. This isolation of the CompactFlash/PC Card's bus enables hot plug-in support. The following table lists the correspondence between the CF0_EN#, CF1_EN#, CF0_DIR, and CF1_DIR signals and data bus isolation statuses when using the data bus isolation buffer.

CF0_EN#, CF1_EN#	CF0_DIR, CF1_DIR	Operation of Bus
0	0	Enable connection via data bus isolation buffer • Write cycle to CompactFlash/PC Card
0	1	Enable connection via data bus isolation buffer • Read cycle to CompactFlash/PC Card
1	– (Undefined)	Disable connection via data bus isolation buffer

(7) USB (host/function) interface signals

Signal Name	I/O	Function	Alternate Function
CLK48	I	USB clock (48 MHz)	–
UHDP	I/O	USB host serial data (+) signal Be sure to connect a 22 Ω resistor in series for impedance matching.	–
UHDN	I/O	USB host serial data (–) signal Be sure to connect a 22 Ω resistor in series for impedance matching.	–
UPON	O	USB host route hub power control signal	–
UOC	I	USB host route hub overcurrent input signal	–
UDP	I/O	USB function serial data (+) signal Be sure to connect a 22 Ω resistor in series for impedance matching.	–
UDN	I/O	USB function serial data (–) signal Be sure to connect a 22 Ω resistor in series for impedance matching.	–

(8) AC97/I^2S stereo audio interface signals

Signal Name	I/O	Function	Alternate Function
BITCLK/SCLK	I/O	Bit clock input (12.288 MHz) for AC97/input or output of I^2S clock (maximum frequency during input: 6.144 MHz). When used as the SCLK signal, this signal is output by the VR4181A when the I2SU is in master mode and is input from an external source in slave mode.	CTS2#
SYNC/WS	I/O	Synchronous clock output for AC97/input or output of I^2S word select signal When used as the WS signal, this signal is output by the VR4181A when the I2SU is in master mode and is input from an external source in slave mode.	RTS2#, DIVMODE1
SDATAOUT/SDO	O	Serial data output signal for AC97/serial data output signal for I^2S	DTR2#, DIVMODE0
SDATAIN/SDI	I	Serial data input signal for AC97/serial data input signal for I^2S	DCD2#
SRESET#	O	Reset signal for AC97	DSR2#

(9) Clocked serial interface signals

Signal Name	I/O	Function	Alternate Function
SCK	I/O	Serial clock (maximum frequency for input and output: 4.6 MHz) This signal is output by the VR4181A in master mode and is input from an external source in slave mode.	KSCAN11, GPIO23
SI	I	Serial data input signal	KSCAN10, GPIO22
SO	O	Serial data output signal This signal is set to high impedance when the value of the FRMEN bit and FRMMD bit is 1 in the CSIMODE register, and the FRM signal is at high level.	KSCAN9 , GPIO21
FRM	I	Serial frame signal This signal determines the data direction (transmit/receive), or it can be used to enable (low level) or disable (high level) transfers.	KSCAN8, GPIO20

(10) 16550 (UART) serial interface signals

Signal Name	I/O	Function	Alternate Function
RxD0	I	Serial (channel 0) receive data	–
TxD0	O	Serial (channel 0) transmit data	CLKSEL2
RTS0#	O	Serial (channel 0) transmit request signal	GPIO19, CLKSEL1
CTS0#	I	Serial (channel 0) transmit enable signal	GPIO18
DTR0#/RTS1#	O	Serial (channel 0) terminal ready signal/serial (channel 1) transmit request signal	GPIO17, CLKSEL0
DCD0#	I	Serial (channel 0) carrier detection signal	GPIO16
DSR0#/CTS1#	I	Serial (channel 0) data set ready signal/serial (channel 1) transmit enable signal	GPIO15
RxD1	I	Serial (channel 1) receive data	SCL1, GPIO14
TxD1	O	Serial (channel 1) transmit data	SDA1, GPIO13
RxD2	I	Serial (channel 2) receive data	IRDIN
TxD2	O	Serial (channel 2) transmit data	IRDOUT, MIPS16EN
RTS2#	O	Serial (channel 2) transmit request signal	SYNC, WS, DIVMODE1
CTS2#	I	Serial (channel 2) transmit enable signal	BITCLK, SCLK
DTR2#	O	Serial (channel 2) terminal ready signal	SDATAOUT, SDO, DIVMODE0
DCD2#	I	Serial (channel 2) carrier detection signal	SDATAIN, SDI
DSR2#	I	Serial (channel 2) data set ready signal	SRESET#

(11) IrDA interface signals

Signal Name	I/O	Function	Alternate Function
IRDIN	I	IrDA receive data input	RxD2
IRDOUT	O	IrDA transmit data output	TxD2, MIPS16EN

(12) I^2C serial interface signals (μPD30181AY only)

Signal Name	I/O	Function	Alternate Function
SCL1	I/O	Serial clock (open drain) for I^2C (channel 1)	RxD1, GPIO14
SDA1	I/O	Serial I/O data (open drain) for I^2C (channel 1)	TxD1, GPIO13
SCL0	I/O	Serial clock (open drain) for I^2C (channel 0)	KPORT7, GPIO12
SDA0	I/O	Serial I/O data (open drain) for I^2C (channel 0)	KPORT6, GPIO11

(13) PWM interface signals

Signal Name	I/O	Function	Alternate Function
PWM2	O	PWM output (channel 2)	KSCAN5, GPIO10
PWM1	O	PWM output (channel 1)	KSCAN6, GPIO9
PWM0	O	PWM output (channel 0)	KSCAN7, GPIO8

(14) Keyboard interface signals

Signal Name	I/O	Function	Alternate Function
KPORT7	I	Key scan input data	SCL0, GPIO12
KPORT6	I	Key scan input data	SDA0, GPIO11
KPORT5	I	Key scan input data	CF1_EN#, GPIO38
KPORT4	I	Key scan input data	CF1_DIR, GPIO39
KPORT(3:0)	I	Key scan input data	GPIO(7:4)
KSCAN11	O	Key scan output data	SCK, GPIO23
KSCAN10	O	Key scan output data	SI, GPIO22
KSCAN9	O	Key scan output data	SO, GPIO21
KSCAN8	O	Key scan output data	FRM, GPIO20
KSCAN7	O	Key scan output data	PWM0, GPIO8
KSCAN6	O	Key scan output data	PWM1, GPIO9
KSCAN5	O	Key scan output data	PWM2, GPIO10
KSCAN4	O	Key scan output data	CF1_VCCEN#, GPIO37
KSCAN(3:0)	O	Key scan output data	GPIO(3:0)

(15) Touch panel/analog interface signals

Signal Name	I/O	Function	Alternate Function
TPX(1:0)	I/O	Touch panel X coordinate data This signal is used to detect the X coordinate of the touch panel location that has been pressed when the supply voltage is applied to the X coordinates and Y coordinates.	–
TPY(1:0)	I/O	Touch panel Y coordinate data This signal is used to detect the Y coordinate of the touch panel location that has been pressed when the supply voltage is applied to the Y coordinates and X coordinates.	–
AIN(3:0)	I	General-purpose A/D data input	–
AOUT	O	General-purpose D/A data output	–

(16) Debug interface signals

Signal Name	I/O	Function	Alternate Function
JTCK	I	N-Wire clock	–
JTMS	I	N-Wire mode select signal This signal selects N-Wire serial transfer mode.	–
JTDI/RMODE#	I	N-Wire input data/N-Wire reset mode select signal This pin functions alternately as RMODE# and JTDI. When JTRST# is active it functions as RMODE#, and when JTRST# is inactive it functions as JTDI. • RMODE# input When JTRST# is active, this pin is the reset mode pin. The initial value for a debug reset is determined by the level of this signal. A debug reset is a reset of the processor, and there are two types: a debug cold reset and a debug soft reset. This serves the same function as Cold Reset input and Soft Reset input from various target systems. 0: Sets debug reset as valid and resets CPU core 1: Sets debug reset as invalid and does not reset CPU core • JTDI input When the JTRST# signal is inactive, this pin operates as the N-Wire serial data input.	–
JTDO	O	N-Wire serial data output	–
JTRST#	I	N-Wire reset signal	–
BKTGIO#	I/O	N-Wire break trigger I/O • BKTGIO#: When used for input setting When JTRST# is inactive and BKTGIO# is used for input setting, this pin is the event trigger/break request input pin. When break requests are valid, setting BKTGIO# to low level stops execution of user programs in normal mode and forcibly shifts the processor to debug mode. After BKTGIO# goes to low level in debug mode, break requests are retained until the processor is restored to normal mode. 0: Requests break and forcibly shifts processor to debug mode 1: Retains current status of processor • BKTGIO#: When used for output setting When JTRST# is inactive and BKTGIO# is used for output setting, this pin is the event trigger/break output pin. When the processor is operating in normal mode and an event is detected that meets any of the conditions for a hardware breakpoint (instruction address breakpoint or data access breakpoint), an event trigger is output from BKTGIO# as a low level signal (one pulse) and detection of the event is reported to the external debugging tool. Finally, after the event trigger is output, all detected events are reported as one event trigger. When the processor is shifted to debug mode, output continues at low level and all previously non-reported events are not reported. 0: Hardware breakpoint was detected The processor is shifted to debug mode. 1: The processor is in normal mode.	–

(17) General-purpose I/O signals

(1/2)

Signal Name	I/O	Function	Alternate Function
GPO63	O	General-purpose output ports	VPBIAS
GPO62	O		VPLCD
GPIO(61:54)	I/O	General-purpose I/O ports	A(22:15)
GPIO(53:52)	I/O		TC(1:0)#
GPIO51	I/O		FPD15, CF1_READY
GPIO50	I/O		FPD14, CF1_STSCHG#
GPIO(49:48)	I/O		FPD(13:12), CF1_CE(2:1)#
GPIO(47:46)	I/O		FPD(11:10), CF1_CD(2:1)#
GPIO(45:40)	I/O		FPD(9:4)
GPIO39	I/O		CF1_DIR, KPORT4
GPIO38	I/O		CF1_EN#, KPORT5
GPIO37	I/O		CF1_VCCEN#, KSCAN4
GPIO(36:35)	I/O		CF0_CD(2:1)#
GPIO34	I/O		CF0_IOIS16#
GPIO33	I/O		CF_WAIT#
GPIO(32:31)	I/O		CF0_CE(2:1)#
GPIO30	I/O		CF0_STSCHG#
GPIO29	I/O		CF0_READY
GPIO28	I/O		CF0_RESET
GPIO27	I/O		CF0_DIR
GPIO26	I/O		CF0_EN#
GPIO25	I/O		CF_REG#
GPIO24	I/O		CF0_VCCEN#
GPIO23	I/O		SCK, KSCAN11
GPIO22	I/O		SI, KSCAN10
GPIO21	I/O		SO, KSCAN9
GPIO20	I/O		FRM, KSCAN8
GPIO19	I/O		RTS0#/ CLKSEL1
GPIO18	I/O		CTS0#

(2/2)

Signal Name	I/O	Function	Alternate Function
GPIO17	I/O	General-purpose I/O ports	DTR0#, RTS1#, CLKSEL0
GPIO16	I/O		DCD0#
GPIO15	I/O		DSR0#, CTS1#
GPIO14	I/O		RxD1, SCL1
GPIO13	I/O		TxD1, SDA1
GPIO12	I/O		SCL0, KPORT7
GPIO11	I/O		SDA0, KPORT6
GPIO10	I/O		PWM2, KSCAN5
GPIO9	I/O		PWM1, KSCAN6
GPIO8	I/O		PWM0, KSCAN7
GPIO(7:4)	I/O		KPORT(3:0)
GPIO(3:0)	I/O		KSCAN(3:0)

(18) Mode setting signals

These signals are used to set various modes.

These signals are sampled only when the RTCRST# signal has changed to high level. At all other times, they can be used as alternate-function pins.

In order to disconnect a pull-up or pull-down resistor for mode setting during normal operation, use a switch linked to the RTCRST# signal.

Signal Name	I/O	Function	Alternate Function
BMODE1	I	Boot ROM type setting BMODE(1:0) = 01: ROM/flash memory BMODE(1:0) = 10: SyncFlash memory BMODE(1:0) = 00 or 11: Setting prohibited	VSYNC, FLM
BMODE0	I		ENAB, M
NWIREEN	I	N-Wire use enable signal 0: Disabled 1: Enabled	HSYNC, LOCLK
DBUS32	I	Boot ROM bus width specification 0: 16 bits 1: 32 bits	CF1_RESET
CLKSEL2	I	Set frequency of CPU core's pipeline reference clock (AClock) CLKSEL(2:0) = 111: Setting prohibited (147.4 MHz) CLKSEL(2:0) = 110: 131.1 MHz CLKSEL(2:0) = 101: 118.0 MHz CLKSEL(2:0) = 100: 98.3 MHz CLKSEL(2:0) = 011: 90.7 MHz CLKSEL(2:0) = 010: 84.1 MHz CLKSEL(2:0) = 001: 78.5 MHz CLKSEL(2:0) = 000: 73.7 MHz	TxD0
CLKSEL1	I		RTS0#, GPIO19
CLKSEL0	I		DTR0#, RTS1#, GPIO17
DIVMODE1	I	Set division ratio of AClock and internal system bus reference clock (TClock) DIVMODE(1:0) = 10: AClock/2 (DIV2 mode) DIVMODE(1:0) = 01: AClock/3 (DIV3 mode) DIVMODE(1:0) = 11, 00: Setting prohibited	RTS2#, SYNC, WS
DIVMODE0	I		DTR2#, SDO, SDATAOUT
MIPS16EN	I	Enables use of MIPS16 instruction set 0: Use disabled 1: Use enabled	TxD2, IRDOUT

(19) Dedicated V_{DD}/GND signals

Signal Name	Power Supply	Function
VDD2	2.5 V	Power supply for internal logic
GND2	2.5 V	GND for internal logic
VDD3	3.3 V	Power supply for I/O buffers (except for I/O buffer of USB transceiver)
GND3	3.3 V	GND for I/O buffers (except for I/O buffer of USB transceiver)
VDDU	3.3 V	Dedicated power supply for USB transceiver
GNDU	3.3 V	Dedicated GND for USB transceiver
VDDP	2.5 V	Dedicated power supply for PLL (analog unit)
GNDP	2.5 V	Dedicated GND for PLL (analog unit)
VDDO	3.3 V	Dedicated power supply for oscillator
GNDO	3.3 V	Dedicated GND for oscillator
VDDAD	3.3 V	Dedicated power supply for the A/D and D/A converters. The voltage applied to this pin becomes the maximum voltage value for the A/D and D/A converters' interface signals.
GNDAD	3.3 V	Dedicated GND for the A/D and D/A converters. The voltage applied to this pin becomes the minimum voltage value for the A/D and D/A converters' interface signals.
VDDTP	3.3 V	Dedicated power supply for touch panel interface
GNDTP	3.3 V	Dedicated GND for touch panel interface

Caution The V_R4181A includes two power supply systems, a 2.5 V system and a 3.3 V system. When applying a voltage, be sure to apply it to the 3.3 V power supply system first. Apply voltage to the 2.5 V power supply system according to the status of the MPOWER pin.

1.2 Pin Statuses in Specific Status

(1/7)

Pin Name (Signal Name)	Alternate-Function Pin Name (Alternate Signal Name)	During RTC Reset	After RTC Reset	After Reset by RSTSW or Watchdog Timer	In Suspend Mode	In Hibernate Mode or During Shutdown by HALTimer
A24	CKE1	0	0	0	**Note 1**	0
A23	RP#	0	0	0	**Note 1**	0
A(22:15)	GPIO(61:54)	0	0	0	**Note 1**	0
A(14:0)	–	0	0	0	**Note 1**	0
SA10	–	0	0	0	**Note 1**	0
D(31:0)	–	0	0	0	**Note 1**	0
IORD#	–	Hi-Z	Hi-Z	1	**Note 1**	Hi-Z
IOWR#	–	Hi-Z	Hi-Z	1	**Note 1**	Hi-Z
IORDY	–	Hi-Z	Hi-Z	–	–	Hi-Z
IOCS16#	–	Hi-Z	Hi-Z	–	–	Hi-Z
UBE#	–	0	0	1/0	**Note 1**	0
PCS(4:0)#	–	Hi-Z	Hi-Z	1	**Note 1**	Hi-Z
SYSDIR	–	0	0	0	**Note 1**	0
SYSEN#	–	0	0	1/0	**Note 1**	0
DRQ(1:0)#	–	Hi-Z	Hi-Z	–	–	Hi-Z
DAK(1:0)#	–	Hi-Z	Hi-Z	1	**Note 1**	Hi-Z
TC(1:0)#	GPIO(53:52)	Hi-Z	Hi-Z	–	**Note 1**	Hi-Z
NMI#	–	–	–	–	–	–
ROMCS#	–	Hi-Z	Hi-Z	1	**Note 1**	Hi-Z
MEMRD#	–	Hi-Z	Hi-Z	1	**Note 1**	Hi-Z
MEMWR#	–	Hi-Z	Hi-Z	1	**Note 1**	Hi-Z
RP#	A23	0	0	1	**Note 1**	0
SDCLK	–	0	Operating	Operating	0	0
CKE1	A24	0	1	1	**Note 1**	0
CKE0	–	0	1	**Note 2**	0	0
SDCS(3:2)#	–	0	1	1/0	1/0	0
SDCS(1:0)#	–	0	1	1/0	1/0	0
RAS#	–	0	1	1/0	1/0	0

Notes 1. The status in the previous Fullspeed mode is retained.

2. Changes according to the setting in the SDRAMACT register in the GIU.

When SDACT bit = 0: 1

When SDACT bit = 1: 0

Remarks 1. 0: Low level, 1: High level, Hi-Z: High impedance

2. When a pin has high impedance, the buffer's input enable setting is OFF. Leakage current will not occur even when an intermediate level is applied.

(2/7)

Pin Name (Signal Name)	Alternate-Function Pin Name (Alternate Signal Name)	During RTC Reset	After RTC Reset	After Reset by RSTSW or Watchdog Timer	In Suspend Mode	In Hibernate Mode or During Shutdown by HALTimer
CAS#	–	0	1	1/0	1/0	0
DQM(3:0), LBE(3:0)#	–	0	0	1/0	1/0	0
WE#	–	0	1	1/0	1/0	0
POWER	–	–	–	–	–	–
RSTSW#	–	–	–	–	–	–
RTCRST#	–	–	–	–	–	–
POWERON	–	0	0	0	0	0
MPOWER	–	0	0	1	1	0
RTCX(2:1)	–	–	–	–	–	–
CLKX(2:1)	–	–	–	–	–	–
DCLK, SHCLK	–	0	0	0	**Note 1**	0
HSYNC, LOCLK	NWIREEN	**Note 2**	0	0	**Note 1**	0
VSYNC, FLM	BMODE1	**Note 3**	0	0	**Note 1**	0
ENAB, M	BMODE0	**Note 3**	0	0	**Note 1**	0
FPD15	CF1_READY, GPIO51	Hi-Z	Hi-Z	0	**Note 1**	Hi-Z
FPD14	CF1_STSCHG#, GPIO50	Hi-Z	Hi-Z	0	**Note 1**	Hi-Z
FPD(13:12)	CF1_CE(2:1)#, GPIO(49:48)	Hi-Z	Hi-Z	0	**Note 1**	Hi-Z
FPD(11:10)	CF1_CD(2:1)#, GPIO(47:46)	Hi-Z	Hi-Z	0	**Note 1**	Hi-Z
FPD(9:4)	GPIO(45:40)	Hi-Z	Hi-Z	0	**Note 1**	0
FPD(3:0)	–	0	0	0	**Note 1**	0
VPLCD	GPO62	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
VPBIAS	GPO63	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Notes 1. The status in the previous Fullspeed mode is retained. If the LCD panel's voltage drops during Suspend mode, enter settings in the LCU register to stop output operations and set the pin's value to 0.

2. The input level is sampled when the RTCRST# signal has changed to high level in order to enable or disable use of the N-Wire.

3. The input level is sampled when the RTCRST# signal has changed to high level in order to set the boot ROM type.

Remarks 1. 0: Low level, 1: High level, Hi-Z: High impedance

2. When a pin has high impedance, the buffer's input enable setting is OFF. Leakage current will not occur even when an intermediate level is applied.

(3/7)

Pin Name (Signal Name)	Alternate-Function Pin Name (Alternate Signal Name)	During RTC Reset	After RTC Reset	After Reset by RSTSW or Watchdog Timer	In Suspend Mode	In Hibernate Mode or During Shutdown by HALTimer
CF1_CD(2:1)#	FPD(11:10), GPIO(47:46)	Hi-Z	Hi-Z	–	–	Hi-Z
CF1_CE(2:1)#	FPD(13:12) , GPIO(49:48)	Hi-Z	Hi-Z	Hi-Z	**Note 1**	Hi-Z
CF1_STSCHG#	FPD14, GPIO50	Hi-Z	Hi-Z	–	–	Hi-Z
CF1_READY	FPD15, GPIO51	Hi-Z	Hi-Z	–	–	Hi-Z
CF1_RESET	DBUS32	**Note 2**	Hi-Z	Hi-Z	**Note 1**	**Note 3**
CF1_DIR	KPORT4, GPIO39	Hi-Z	Hi-Z	0	**Note 1**	Hi-Z
CF1_EN#	KPORT5, GPIO38	Hi-Z	Hi-Z	Hi-Z	**Note 1**	Hi-Z
CF1_VCCEN#	KSCAN4, GPIO37	Hi-Z	Hi-Z	1	**Note 1**	Hi-Z
CF0_CD(2:1)#	GPIO(36:35)	Hi-Z	Hi-Z	–	–	Hi-Z
CF0_IOIS16#	GPIO34	Hi-Z	Hi-Z	–	–	Hi-Z
CF_WAIT#	GPIO33	Hi-Z	Hi-Z	–	–	Hi-Z
CF0_CE(2:1)#	GPIO(32:31)	Hi-Z	Hi-Z	Hi-Z	**Note 1**	Hi-Z
CF0_STSCHG#	GPIO30	Hi-Z	Hi-Z	–	–	Hi-Z
CF0_READY	GPIO29	Hi-Z	Hi-Z	–	–	–
CF0_RESET	GPIO28	Hi-Z	Hi-Z	Hi-Z	**Note 1**	Hi-Z
CF0_DIR	GPIO27	Hi-Z	Hi-Z	0	**Note 1**	Hi-Z
CF0_EN#	GPIO26	Hi-Z	Hi-Z	Hi-Z	**Note 1**	Hi-Z
CF_REG#	GPIO25	Hi-Z	Hi-Z	Hi-Z	**Note 1**	Hi-Z
CF0_VCCEN#	GPIO24	Hi-Z	Hi-Z	1	**Note 1**	Hi-Z
CLK48	–	Hi-Z	Hi-Z	**Note 3**	**Note 3**	Hi-Z
UHDP	–	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UHDN	–	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UPON	–	0	0	0	0	0
UOC	–	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UDP	–	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Notes 1. The status in the previous Fullspeed mode is retained.

2. The input level is sampled when the RTCRST# signal has changed to high level in order to set the boot ROM bus width.

3. The registers in the GIU can be used to set 1, 0, or high impedance.

Remarks 1. 0: Low level, 1: High level, Hi-Z: High impedance

2. When a pin has high impedance, the buffer's input enable setting is OFF. Leakage current will not occur even when an intermediate level is applied.

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Pin Name (Signal Name)	Alternate-Function Pin Name (Alternate Signal Name)	During RTC Reset	After RTC Reset	After Reset by RSTSW or Watchdog Timer	In Suspend Mode	In Hibernate Mode or During Shutdown by HALTimer
UDN	–	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
BITCLK	SCLK, CTS2#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
SYNC	WS, RTS2#, DIVMODE1	**Note 1**	Hi-Z	Hi-Z	Hi-Z	Hi-Z
SDATAOUT	SDO, DTR2#, DIVMODE0	**Note 1**	Hi-Z	Hi-Z	Hi-Z	Hi-Z
SDATAIN	SDI, DCD2#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
SRESET#	DSR2#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
SCLK	BITCLK, CTS2#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
WS	SYNC, RTS2#, DIVMODE1	**Note 1**	Hi-Z	Hi-Z	Hi-Z	Hi-Z
SDO	SDATAOUT, DTR2#, DIVMODE0	**Note 1**	Hi-Z	Hi-Z	Hi-Z	Hi-Z
SDI	SDATAIN, DCD2#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
SCK	KSCAN11, GPIO23	Hi-Z	Hi-Z	Hi-Z	**Note 2**	Hi-Z
SI	KSCAN10, GPIO22	Hi-Z	Hi-Z	Hi-Z	**Note 2**	Hi-Z
SO	KSCAN9, GPIO21	Hi-Z	Hi-Z	Hi-Z	**Note 2**	Hi-Z
FRM	KSCAN8, GPIO20	Hi-Z	Hi-Z	–	**Note 2**	Hi-Z
RxD0	–	Hi-Z	Hi-Z	–	–	Hi-Z
TxD0	CLKSEL2	**Note 3**	Hi-Z	1	**Note 2**	1
RTS0#	GPIO19, CLKSEL1	**Note 3**	Hi-Z	1	**Note 2**	1
CTS0#	GPIO18	Hi-Z	Hi-Z	–	–	Hi-Z

Notes 1. The input level is sampled when the RTCRST# signal has changed to high level in order to set the division ratio for the CPU core's pipeline reference clock (AClock) and the peripheral system bus's reference clock (TClock).

2. The status in the previous Fullspeed mode is retained.

3. The input level is sampled when the RTCRST# signal has changed to high level in order to set the frequency of the CPU core's pipeline reference clock (AClock).

Remarks 1. 0: Low level, 1: High level, Hi-Z: High impedance

2. When a pin has high impedance, the buffer's input enable setting is OFF. Leakage current will not occur even when an intermediate level is applied.

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Pin Name (Signal Name)	Alternate-Function Pin Name (Alternate Signal Name)	During RTC Reset	After RTC Reset	After Reset by RSTSW or Watchdog Timer	In Suspend Mode	In Hibernate Mode or During Shutdown by HALTimer
DTR0#	RTS1#, GPIO17, CLKSEL0	**Note 1**	Hi-Z	1	**Note 2**	Hi-Z
DCD0#	GPIO16	–	–	–	–	–
DSR0#	CTS1#, GPIO15	–	–	–	–	Hi-Z
RxD1	SCL1, GPIO14	Hi-Z	Hi-Z	–	–	Hi-Z
TxD1	SDA1, GPIO13	Hi-Z	Hi-Z	1	**Note 2**	Hi-Z
RTS1#	DTR0#, GPIO17, CLKSEL0	**Note 1**	Hi-Z	1	**Note 2**	Hi-Z
CTS1#	DSR0#, GPIO15	–	–	–	–	Hi-Z
RxD2	IRDIN	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
TxD2	IRDOUT, MIPS16EN	**Note 3**	Hi-Z	1	**Note 2**	Hi-Z
RTS2#	SYNC, WS, DIVMODE1	**Note 4**	Hi-Z	1	**Note 2**	Hi-Z
CTS2#	SCLK, BITCLK	Hi-Z	Hi-Z	Hi-Z	–	Hi-Z
DTR2#	SDO, SDATAOUT, DIVMODE0	**Note 4**	Hi-Z	1	**Note 2**	Hi-Z
DCD2#	SDI, SDATAIN	Hi-Z	Hi-Z	Hi-Z	–	Hi-Z
DSR2#	SRESET#	Hi-Z	Hi-Z	Hi-Z	–	Hi-Z
IRDIN	RxD2	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
IRDOUT	TxD2, MIPS16EN	**Note 3**	Hi-Z	0	**Note 2**	Hi-Z

Notes 1. The input level is sampled when the RTCRST# signal has changed to high level in order to set the frequency of the CPU core's pipeline reference clock (AClock).

2. The status in the previous Fullspeed mode is retained.

3. The input level is sampled when the RTCRST# signal has changed to high level in order to set whether to use the MIPS16 instruction set or not.

4. The input level is sampled when the RTCRST# signal has changed to high level in order to set the division ratio for the CPU core's pipeline reference clock (AClock) and the peripheral system bus's reference clock (TClock).

Remarks 1. 0: Low level, 1: High level, Hi-Z: High impedance

2. When a pin has high impedance, the buffer's input enable setting is OFF. Leakage current will not occur even when an intermediate level is applied.

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Pin Name (Signal Name)	Alternate-Function Pin Name (Alternate Signal Name)	During RTC Reset	After RTC Reset	After Reset by RSTSW or Watchdog Timer	In Suspend Mode	In Hibernate Mode or During Shutdown by HALTimer
SCL1[Note 1]	RxD1, GPIO14	Hi-Z	Hi-Z	Hi-Z	**Note 2**	Hi-Z
SDA1[Note 1]	TxD1, GPIO13	Hi-Z	Hi-Z	Hi-Z	**Note 2**	Hi-Z
SCL0[Note 1]	KPORT7, GPIO12	Hi-Z	Hi-Z	Hi-Z	**Note 2**	Hi-Z
SDA0[Note 1]	KPORT6, GPIO11	Hi-Z	Hi-Z	Hi-Z	**Note 2**	Hi-Z
PWM2	KSCAN5, GPIO10	Hi-Z	Hi-Z	0	**Note 2**	Hi-Z
PWM1	KSCAN6, GPIO9	Hi-Z	Hi-Z	**Note 2**	**Note 2**	**Note 2**
PWM0	KSCAN7, GPIO8	Hi-Z	Hi-Z	**Note 2**	**Note 2**	**Note 2**
KPORT7	SCL0, GPIO12	Hi-Z	Hi-Z	–	–	Hi-Z
KPORT6	SDA0, GPIO11	Hi-Z	Hi-Z	–	–	Hi-Z
KPORT5	CF1_EN#, GPIO38	Hi-Z	Hi-Z	–	–	Hi-Z
KPORT4	CF1_DIR, GPIO39	Hi-Z	Hi-Z	–	–	Hi-Z
KPORT(3:0)	GPIO(7:4)	Hi-Z	Hi-Z	–	–	Hi-Z
KSCAN11	SCK, GPIO23	Hi-Z	Hi-Z	0	**Note 2**	Hi-Z
KSCAN10	SI, GPIO22	Hi-Z	Hi-Z	0	**Note 2**	Hi-Z
KSCAN9	SO, GPIO21	Hi-Z	Hi-Z	0	**Note 2**	Hi-Z
KSCAN8	FRM, GPIO20	Hi-Z	Hi-Z	0	**Note 2**	Hi-Z
KSCAN7	PWM0, GPIO8	Hi-Z	Hi-Z	0	**Note 2**	Hi-Z
KSCAN6	PWM1, GPIO9	Hi-Z	Hi-Z	0	**Note 2**	Hi-Z
KSCAN5	PWM2, GPIO10	Hi-Z	Hi-Z	0	**Note 2**	Hi-Z
KSCAN4	CF1_VCCEN#, GPIO37	Hi-Z	Hi-Z	0	**Note 2**	Hi-Z
KSCAN(3:0)	GPIO(3:0)	Hi-Z	Hi-Z	0	**Note 2**	Hi-Z
TPX(1:0)	–	1	1	1	**Note 2**	1
TPY(1:0)	–	Hi-Z	Hi-Z	Hi-Z	**Note 2**	Hi-Z
AIN(3:0)	–	–	–	–	–	–
AOUT	–	0	0	0	**Note 2**	0

Notes 1. μPD30181AY only

2. The status in the previous Fullspeed mode is retained.

Remarks 1. 0: Low level, 1: High level, Hi-Z: High impedance

2. When a pin has high impedance, the buffer's input enable setting is OFF. Leakage current will not occur even when an intermediate level is applied.

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Pin Name (Signal Name)	Alternate-Function Pin Name (Alternate Signal Name)	During RTC Reset	After RTC Reset	After Reset by RSTSW or Watchdog Timer	In Suspend Mode	In Hibernate Mode or During Shutdown by HALTimer
JTCK[Note 1]	–	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
JTMS[Note 1]	–	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
JTDI[Note 1], RMODE#	–	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
JTDO[Note 1]	–	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
JTRST#[Note 1]	–	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
BKTGIO#[Note 1]	–	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
GPO63	VPBIAS	Hi-Z	HI-Z	Hi-Z	Hi-Z	Hi-Z
GPO62	VPLCD	HI-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
GPIO(61:54)[Note 2]	A(22:15)	Hi-Z	Hi-Z	**Note 3**	**Note 3**	**Note 3**
GPIO(53:0)	**Note 4**	Hi-Z[Note 5]	Hi-Z	**Note 3**	**Note 3**	**Note 3**

Notes 1. This is the pin status when the N-Wire function has been set to use prohibit status via a setting for the NWIREEN pin.

2. When SyncFlash memory has been selected as the boot ROM, this pin can be used as the GPIO pin.

3. The registers in the GIU can be used to set 1, 0, or high impedance.

4. See the other pin names and alternate-function pin names.

5. The GPIO19 and GPIO17 signals are sampled as CLKSEL(1:0) when the RTCRST# signal has changed to high level in order to set the frequency of the CPU core's pipeline reference clock (AClock).

Caution After an RTC reset, the GPIO pins are set in the input direction and input disable status is set. Input enable status can be set by software after an RTC reset. Accordingly, there is no need to externally add elements such as pull-up or pull-down resistors for unused GPIO pins in order to determine the signal status. However, GPIO(61:54), which are shared with A(22:15), function as GPIO pins only when SyncFlash memory has been selected. The status of output pins in Hibernate mode can be specified by using software to enter the required settings in internal registers in advance.

Remarks 1. 0: Low level, 1: High level, Hi-Z: High impedance

2. When a pin has high impedance, the buffer's input enable setting is OFF. Leakage current will not occur even when an intermediate level is applied.

1.3 Pin I/O Circuit Types and Recommended Connection of Unused Pins

(1/3)

Pin Name	I/O	I/O Circuit Type	Recommended Connection of Unused Pins
A24/CKE1	O	A	Leave open
A23/RP#	O	A	Leave open
A(22:15)/GPIO(61:54)	I/O	A	Leave open
A(14:0)	O	A	Leave open
SA10	O	A	Leave open
D(31:0)	I/O	A	Connect to VDD3 or GND3 via a resistor
IORD#	O	A	Leave open
IOWR#	O	A	Leave open
IORDY	I	A	Connect to VDD3
IOCS16#	I	A	Connect to VDD3
UBE#	O	A	Leave open
PCS(4:0)#	O	A	Leave open
SYSDIR	O	A	Leave open
SYSEN#	O	A	Leave open
DRQ(1:0)#	I	A	Connect to VDD3
DAK(1:0)#	O	A	Leave open
TC(1:0)#/GPIO(53:52)	I/O	A	Leave open
NMI#	I	A	Connect to VDD3
ROMCS#	O	A	Leave open
MEMRD#	O	A	Leave open
MEMWR#	O	A	Leave open
SDCLK	O	A	Leave open
CKE0	O	A	Leave open
SDCS(3:0)#	O	A	Leave open
RAS#	O	A	Leave open
CAS#	O	A	Leave open
DQM(3:0)/LBE(3:0)#	O	A	Leave open
WE#	O	A	Leave open
POWER	I	B	Connect to VDD3
RSTSW#	I	B	Connect to VDD3
RTCRST#	I	B	–
POWERON	O	A	Leave open
MPOWER	O	A	Leave open
DCLK/SHCLK	O	A	Leave open
HSYNC/LOCLK/NWIREEN[Note]	I/O	A	Connect to VDD3 or GND3 via a resistor
VSYNC/FLM/BMODE1[Note]	I/O	A	Connect to VDD3 or GND3 via a resistor

Note The signal level is sampled when the RTCRST# signal has changed to high level.

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Pin Name	I/O	I/O Circuit Type	Recommended Connection of Unused Pins
ENAB/M/BMODE0[Note]	I/O	A	Connect to VDD3 or GND3 via a resistor
FPD15/CF1_READY/GPIO51	I/O	A	Leave open
FPD14/CF1_STSCHG#/GPIO50	I/O	A	Leave open
FPD(13:12)/CF1_CE(2:1)#/GPIO(49:48)	I/O	A	Leave open
FPD(11:10)/CF1_CD(2:1)#/GPIO(47:46)	I/O	A	Leave open
FPD(9:4)/GPIO(45:40)	I/O	A	Leave open
FPD(3:0)	O	A	Leave open
VPLCD/GPO62	O	A	Leave open
VPBIAS/GPO63	O	A	Leave open
CF1_RESET/DBUS32[Note]	I/O	B	Connect to VDD3 or GND3 via a resistor
CF1_DIR/KPORT4/GPIO39	I/O	B	Leave open
CF1_EN#/KPORT5/GPIO38	I/O	B	Leave open
CF1_VCCEN#/KSCAN4/GPIO37	I/O	B	Leave open
CF0_CD(2:1)#/GPIO(36:35)	I/O	B	Leave open
CF0_IOIS16#/GPIO34	I/O	B	Leave open
CF_WAIT#/GPIO33	I/O	B	Leave open
CF0_CE(2:1)#/GPIO(32:31)	I/O	B	Leave open
CF0_STSCHG#/GPIO30	I/O	B	Leave open
CF0_READY/GPIO29	I/O	B	Leave open
CF0_RESET/GPIO28	I/O	B	Leave open
CF0_DIR/GPIO27	I/O	B	Leave open
CF0_EN#/GPIO26	I/O	B	Leave open
CF_REG#/GPIO25	I/O	B	Leave open
CF0_VCCEN#/GPIO24	I/O	B	Leave open
SCK/KSCAN11/GPIO23	I/O	B	Leave open
SI/KSCAN10/GPIO22	I/O	B	Leave open
SO/KSCAN9/GPIO21	I/O	B	Leave open
FRM/KSCAN8/GPIO20	I/O	B	Leave open
RxD2/IRDIN	I	B	Leave open
TxD2/IRDOUT/MIPS16EN[Note]	I/O	B	Connect to VDD3 or GND3 via a resistor
RTS2#/SYNC/WS/DIVMODE1[Note]	I/O	B	Connect to VDD3 or GND3 via a resistor
CTS2#/BITCLK/SCLK	I/O	B	Leave open
DTR2#/SDATAOUT/SDO/DIVMODE0[Note]	I/O	B	Connect to VDD3 or GND3 via a resistor
DCD2#/SDATAIN/SDI	I	B	Leave open
DSR2#/SRESET#	I/O	B	Leave open
RxD0	I	B	Connect to VDD3
TxD0/CLKSEL2[Note]	I/O	B	Connect to VDD3 or GND3 via a resistor
RTS0#/GPIO19/CLKSEL1[Note]	I/O	B	Connect to VDD3 or GND3 via a resistor

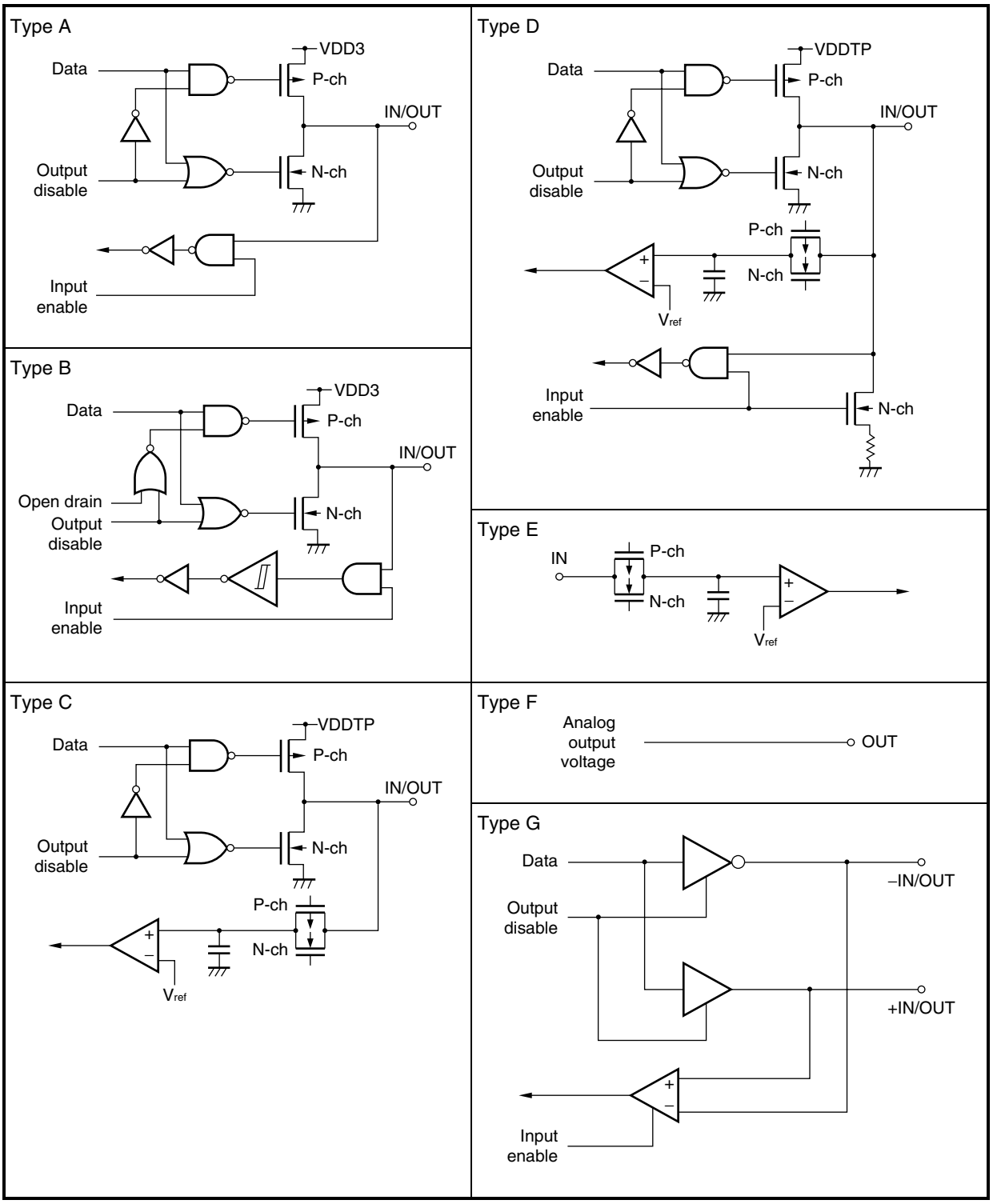
Note The signal level is sampled when the RTCRST# signal has changed to high level.

(3/3)

Pin Name	I/O	I/O Circuit Type	Recommended Connection of Unused Pins
CTS0#/GPIO18	I/O	B	Leave open
DTR0#/RTS1#/GPIO17/CLKSEL0[Note]	I/O	B	Connect to VDD3 or GND3 via a resistor
DCD0#/GPIO16	I/O	B	Leave open
DSR0#/CTS1#/GPIO15	I/O	B	Leave open
RxD1/SCL1/GPIO14	I/O	B	Leave open
TxD1/SDA1/GPIO13	I/O	B	Leave open
SCL0/KPORT7/GPIO12	I/O	B	Leave open
SDA0/KPORT6/GPIO11	I/O	B	Leave open
PWM2/KSCAN5/GPIO10	I/O	B	Leave open
PWM1/KSCAN6/GPIO9	I/O	B	Leave open
PWM0/KSCAN7/GPIO8	I/O	B	Leave open
KPORT(3:0)/GPIO(7:4)	I/O	B	Leave open
KSCAN(3:0)/GPIO(3:0)	I/O	B	Leave open
CLK48	I	A	Leave open
UHDP	I/O	G	Leave open
UHDN	I/O	G	Leave open
UPON	O	A	Leave open
UOC	I	B	Connect to GND3
UDP	I/O	G	Leave open
UDN	I/O	G	Leave open
TPX(1:0)	I/O	C	Leave open
TPY0	I/O	C	Leave open
TPY1	I/O	D	Leave open
AIN(3:0)	I	E	Leave open
AOUT	O	F	Leave open
JTCK	I	A	Leave open
JTMS	I	A	Leave open
JTDI/RMODE#	I	A	Leave open
JTDO	O	A	Leave open
JTRST#	I	A	Leave open
BKTGIO#	I/O	A	Leave open

Note The signal level is sampled when the RTCRST# signal has changed to high level.

1.4 Pin I/O Circuits



Remark Type A: Low slew-rate output
Type B: Schmitt-triggered input, low slew-rate output
Type G: Differential I/O

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD25}	2.5 V (VDD2, VDDP pins)	–0.5 to +3.6	V
	V_{DD33}	3.3 V (VDD3, VDDU, VDDTP, VDDAD, VDDO pins)	–0.5 to +4.0	V
Input voltage	V_I	$V_{DD33} \geq 3.7$ V	–0.5 to +4.0	V
		$V_{DD33} < 3.7$ V	–0.5 to V_{DD33} + 0.3	V
Storage temperature	T_{stg}		–65 to +125	°C

Cautions 1. Do not short-circuit two or more output pins simultaneously.

2. If even one of the above parameters exceeds the absolute maximum ratings even momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding which the product may be physically damaged. Use the product well within these ratings.

The specifications and conditions shown in DC Characteristics and AC Characteristics are the ranges for normal operation and quality assurance of the product.

3. V_I can be –1.5 V if the input pulse is less than 10 ns.

Operating Conditions

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Supply voltage	V_{DD25}	2.5 V (VDD2, VDDP pins)	2.3	2.7	V
	V_{DD33}	3.3 V (VDD3, VDDU, VDDTP, VDDAD, VDDO pins)	3.0	3.6	V
Ambient temperature	T_A	When operating at 131.1 MHz	–40	+85	°C
Oscillation start voltage[Note 1]	V_{DDS}			3.0	V
Oscillation hold voltage[Note 2]	V_{DDH1}			2.5	V
Oscillation hold voltage[Note 3]	V_{DDH2}			3.0	V

Notes 1. This is a voltage at which oscillation is always started after power application, and is applied to oscillators of 32.768 kHz and 18.432 MHz.

2. This is a voltage at which oscillation can be guaranteed if the voltage is lowered from the normal operation level, and is applied to an oscillator of 32.768 kHz.

3. This is a voltage at which oscillation can be guaranteed if the voltage is lowered from the normal operation level, and is applied to an oscillator of 18.432 MHz.

Remark The V_R4181A has two types of power supplies. The 3.3 V power supply should be turned on at first. Turn on/off the 2.5 V power supply depending on the status of the MPOWER pin.

Capacitance (T_A = –40 to +85°C, V_{DD33} = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	Unmeasured pins returned to 0 V.		10	pF
I/O capacitance[Note 1]	C_{I_USB}			20	pF
I/O capacitance[Note 2]	C_{IO}			10	pF

Notes 1. Applies to the UHDP, UHDN, UDP, and UDN pins.

2. Applies to I/O pins other than the UHDP, UHDN, UDP, and UDN pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD25} = 2.3 to 2.7 V, V_{DD33} = 3.0 to 3.6 V)

(1) Pins of I/O circuit types A, C, and D

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH}	Pins of types A[Note 1], C[Note 2], and D[Note 3], I_{OH} = –2 mA	$0.8V_{DD33}$			V
Output voltage, low	V_{OL}	Pins of types A[Note 1], C[Note 2], and D[Note 3], I_{OL} = 2 mA			0.4	V
Input voltage, high	V_{IH}	Pins of types A[Note 1] (excluding GPIO pin of edge triggered interrupt), C[Note 2], and D[Note 3]	2.0		V_{DD33} + 0.3	V
	V_{IH1E}	Pins of type A[Note 4] (GPIO pin of edge triggered interrupt)	$0.75V_{DD33}$		V_{DD33} + 0.3	V
Input voltage, low	V_{IL}	Pins of type A[Note 1] (excluding GPIO pin of edge triggered interrupt), C[Note 2], and D[Note 3]	–0.3		$0.25V_{DD33}$	V
	V_{IL1E}	Pins of type A[Note 4] (GPIO pin of edge triggered interrupt)	–0.3		0.5	V

Notes 1. Applies to the following pins.
D(31:0), IORDY, IOCS16#, DRQ(1:0)#, TC(1:0)#/GPIO(53:52), NMI#, HSYNC/LOCLK/NWIREEN, ENAB/M/BMODE0, VSYNC/FLM/BMODE1, FPD15/CF1_READY/GPIO51, FPD14/CF1_STSCHG#/GPIO50, FPD(13:12)/CF1_CE(2:1)#/GPIO(49:48), FPD(11:10)/CF1_CD(2:1)#/GPIO(47:46), FPD(9:4)/GPIO(45:40), CLK48, JTCK, JTMS, JTDI/RMODE#, JTRST#, BKTGIO#, A(14:0), A23/RP#, A24/CKE1, CAS#, CKE0, DAK(1:0)#, DCLK/SHCLK, DQM(3:0), FPD(3:0), IORD#, JTDO, MEMRD#, MEMWR#, MPOWER, PCS(4:0)#, POWERON, RAS#, ROMCS#, SA10, SDCLK, SDCS(3:0)#, SYSDIR, SYSEN#, UBE#, UPON, VPBIAS/GPO63, VPLCD/GPO62, WE#

2. Applies to the TPX(1:0) and TPY0 pins.

3. Applies to the TPY1 pin.

4. Applies to the following pins.
FPD(9:4)/GPIO(45:40), FPD(11:10)/CF1_CD(2:1)#/GPIO(47:46), FPD(13:12)/CF1_CE(2:1)#/GPIO(49:48), FPD14/CF1_STSCHG#/GPIO50, FPD15/CF1_READY/GPIO51, TC(1:0)#/GPIO(53:52), A(22:15)/GPIO(61:54)

Remark For details of the I/O circuits, refer to **1.4 Pin I/O Circuits**

(2) Pins of I/O circuit types B and G

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH2}	Pins of type B[Note 1], I_{OH} = –2 mA	$0.8V_{DD33}$			V
	V_{OH_USB}	Pins of type G[Note 2], R_{PD} = 15 kΩ	2.8		3.6	V
Output voltage, low	V_{OL2}	Pins of type B[Note 1], I_{OL} = 2 mA			0.4	V
	V_{OL_USB}	Pins of type G[Note 2], R_{PU} = 1.5 kΩ			0.3	V
Input voltage, high	V_{IH2}	Pins of type B[Note 1]	$0.75V_{DD33}$		V_{DD33} + 0.3	V
	V_{IH_USB}	Pins of type G[Note 2], single end	2.0			V
Input voltage, low	V_{IL2}	Pins of type B[Note 1]	–0.3		0.6	V
	V_{IL_USB}	Pins of type G[Note 2], single end			0.8	V
Hysteresis voltage[Note 3]	V_H	Pins of type B[Note 1]		$0.17V_{DD33}$		V
Output cross level[Note 4]	V_{CRS_USB}	Pins of type G[Note 2]	1.3		2.0	V
Differential input sensitivity[Note 4]	V_{DI_USB}	Pins of type G[Note 2]	0.2			V
Differential input common mode range[Note 4]	V_{CM_USB}	Pins of type G[Note 2], V_{DI} < 200 mV	0.8		2.5	V
External pull-up resistor	R_{PU}	Pins of type G[Note 2]	1.425		1.575	kΩ
External pull-down resistor	R_{PD}	Pins of type G[Note 2]	14.25		15.75	kΩ
External resistor for impedance adjustment[Note 5]	R_S	Pins of type G[Note 2]	20.9		23.1	Ω

Notes 1. Applies to the following pins.
POWER, RSTSW#, RTCRST#, CF1_RESET/DBUS32, RxD0, TxD0/CLKSEL2, RxD2/IRDIN, TxD2/IRDOUT/MIPS16EN, CTS2#/BITCLK/SCLK, DTR2#/SDATAOUT/SDO/DIVMODE0, RTS2#/SYNC/WS/DIVMODE1, DCD2#/SDATAIN/SDI, DSR2#/SRESET#, UOC, CF1_DIR/KPORT4/GPIO39, CF1_EN#/KPORT5/GPIO38, CF1_VCCEN#/KSCAN4/GPIO37, CF0_CD2#/GPIO36, CF0_CD1#/GPIO35, CF0_IOIS16#/GPIO34, CF_WAIT#/GPIO33, CF0_CE2#/GPIO32, CF0_CE1#/GPIO31, CF0_STSCHG#/GPIO30, CF0_READY/GPIO29, CF0_RESET/GPIO28, CF0_DIR/GPIO27, CF0_EN#/GPIO26, CF_REG#/GPIO25, CF0_VCCEN#/GPIO24, SCK/KSCAN11/GPIO23, SI/KSCAN10/GPIO22, SO/KSCAN9/GPIO21, FRM/KSCAN8/GPIO20, RTS0#/GPIO19/CLKSEL1, CTS0#/GPIO18, DTR0#/RTS1#/GPIO17/CLKSEL0, DCD0#/GPIO16, DSR0#/CTS1#/GPIO15, RxD1/SCL1/GPIO14, TxD1/SDA1/GPIO13, SCL0/KPORT7/GPIO12, SDA0/KPORT6/GPIO11, PWM(2:0)/KSCAN(5:7)/GPIO(10:8), KPORT(3:0)/GPIO(7:4), KSCAN(3:0)/GPIO(3:0)

2. Applies to the UHDP, UHDN, UDP, and UDN pins

3. Hysteresis voltage: Difference between the minimum voltage at which the high level of a Schmitt input signal is not recognized when the signal goes from low to high and the maximum voltage at which the low level is not recognized when the signal goes from high to low.

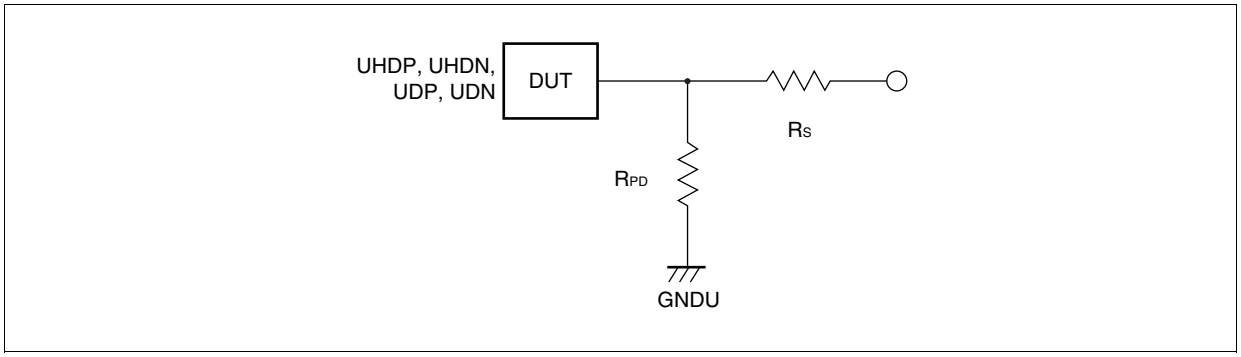
4. Precision tests have not been performed. Only guaranteed as design characteristics.

5. The recommended value is 22 Ω.

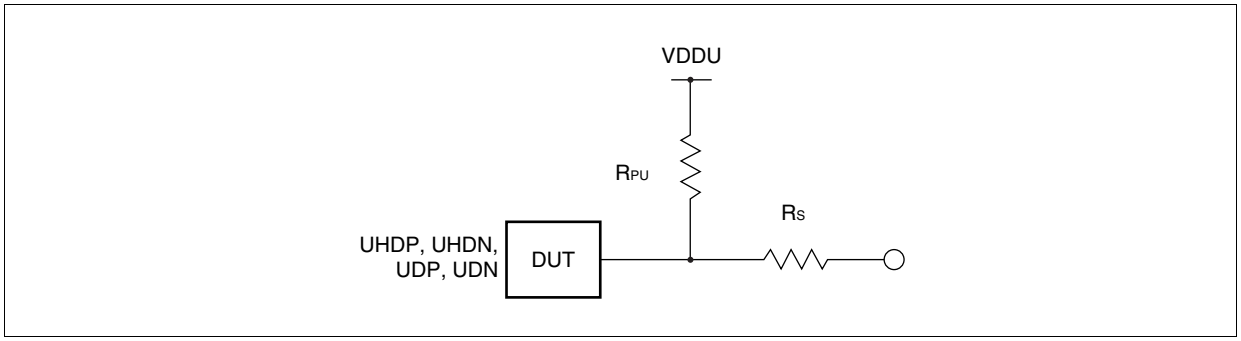
Remark For details of the I/O circuits, refer to **1.4 Pin I/O Circuits**.

Connection example of external resistor

(a) When pulled down



(b) When pulled up



(3) Common

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD25}[Note 2]	Fullspeed mode				350	mA
		Fullspeed mode, program using cache operating, DMA controller operating, clock supplied to PCI unit			165		mA
		Fullspeed mode, program using cache operating, DMA controller operating			100		mA
		Fullspeed mode, program not using cache operating, all peripheral bus masters stopped, all clocks of unused units stopped			80		mA
		Standby mode, peripheral bus master operating continuously			70	90	mA
		Standby mode, all peripheral bus masters stopped, all clocks of unused unit stopped			45	53	mA
		Suspend mode			10	20	mA
		Hibernate mode, V_{DD25} = 0 V			0	0	mA
	I_{DD33}[Note 3]	Fullspeed mode	32-bit bus		45	58	mA
			16-bit bus		40	50	mA
		Standby mode, peripheral bus master operating continuously	32-bit bus		45	58	mA
			16-bit bus		40	50	mA
		Standby mode, all peripheral bus masters stopped, all clocks of unused units stopped			2	4	mA
		Suspend mode			2	4	mA
		Hibernate mode, PWMU channel 0 operating			2	4	mA
		Hibernate mode, PWMU channel 0 stopped			25	50	μA
	I_{DDAD}[Note 4]	A/D, D/A converters operating			3	9	mA
Input leakage current[Note 5]	I_{LI}	V_{DD33} = 3.6 V, V_I = V_{DD33}, 0 V				±5	μA
Output leakage current	I_{LO}	V_{DD33} = 3.6 V, V_I = V_{DD33}, 0 V				±5	μA

Notes 1. Value when AClock = 131.1 MHz, TClock = 65.55 MHz, Div2 mode.

2. I_{DD25} is the total current flowing to the VDD2 and VDDP pins.

3. I_{DD33} is the total current flowing to the VDD3, VDDU, VDDTP, and VDDO pins.

4. I_{DDAD} is the current flowing to the VDDAD pin when Vref is supplied to the A/D and D/A converters.

5. Excluding the I.C. pin.

Remarks 1. In Suspend mode, the internal LCD controller does not operate because the memory controller (MCU) clock and LCD controller (LCU) clock are stopped.

2. Each current value is the average value that flows under the specified conditions. Design the power supply so that the current under the MAX. condition can be supplied stably (so that voltage drop or ripple do not occur in the whole system).

3. The peripheral bus master indicates the following peripheral units.
LCU, DCU, IOPCIU, USBHU, USBFU, AC97U

Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data retention voltage	V_{DDDR3}	Hibernate mode, 3.3 V power supply	2.5	3.6	V
Data retention high-level input voltage	V_{IHDR}	Hibernate mode, RTCRST# pin	$0.9V_{DDDR3}$		V

The data retention voltage and data retention high-level input voltage are the voltages that guarantee the operation of ElapsedTime counter in the RTC and the data retention of the registers (using a 3.3 V power supply) of the following peripheral units. These voltages do not apply to the data in the CPU core (using a 2.5 V power supply).

PMU: PMUINTREG, PMUCNTREG, PMUWAITREG, PMUDIVREG

RTC: ETIMELREG, ETIMEMREG, ETIMEHREG, ECMPLREG, ECMPMREG, ECMPHREG

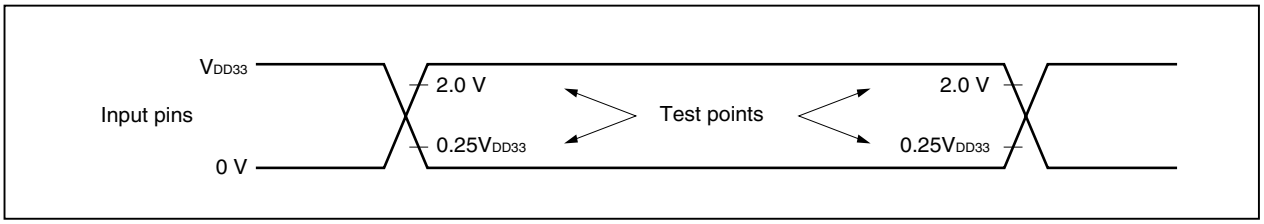
GIU: GPMODE0, GPMODE1, GPMODE2, GPMODE3, GPMODE4, GPMODE5, GPMODE6, GPMODE7, GPDATA0, GPDATA1, GPDATA2, GPDATA3, GPINEN0, GPINEN1, GPINEN2, GPINEN3, GPINTMSK0, GPINTMSK1, GPINTMSK2, GPINTMSK3, GPINTTYP0, GPINTTYP1, GPINTTYP2, GPINTTYP3, GPINTTYP4, GPINTTYP5, GPINTTYP6, GPINTTYP7, GPINTSTAT0, GPINTSTAT1, GPINTSTAT2, GPINTSTAT3, PINMODE, SDRAMACT, NVREG0, NVREG1, NVREG2, NVREG3

PWMU: PWM0ATSREG, PWM0IATSREG, PWM0CNTREG, PWM0ASTCREG, PWM0INTREG, PWM1CTRL, PWM1BUF

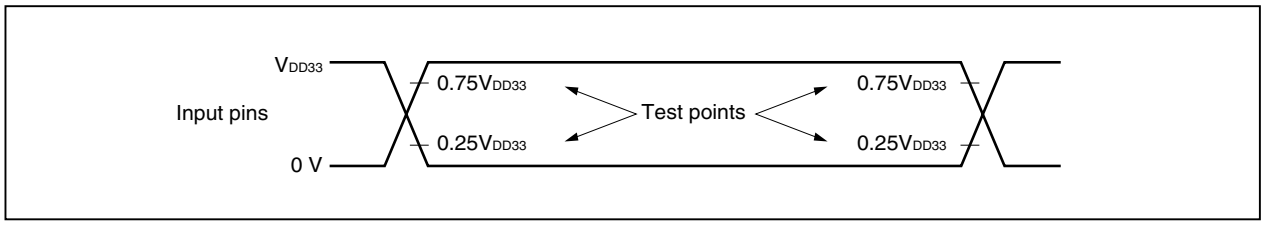
AC Characteristics (T_A = −40 to +85°C, V_{DD25} = 2.3 to 2.7 V, V_{DD33} = 3.0 to 3.6 V)

AC test input test points

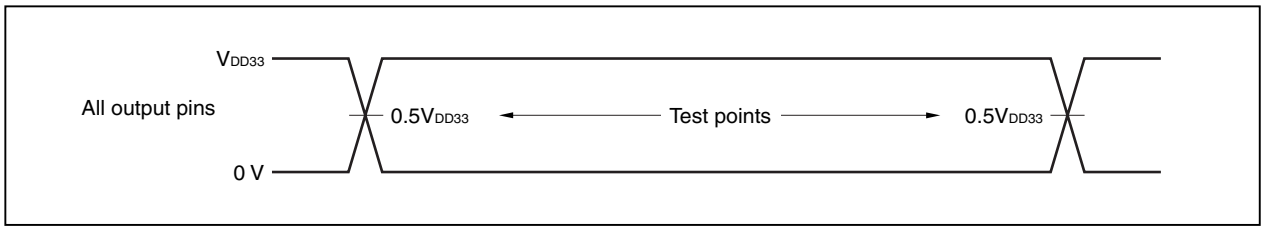
(a) D(31:0), IORDY, IOCS16#, DRQ(1:0)#, TC(1:0)#/GPIO(53:52), NMI#, HSYNC/LOCLK/NWIREEN, VSYNC/FLM/BMODE1, FPD15/CF1_READY/GPIO51, FPD14/CF1_STSCHG#/GPIO50, FPD(13:12)/CF1_CE(2:1)#/GPIO(49:48), FPD(11:10)/CF1_CD(2:1)#/GPIO(47:46), FPD(9:4)/GPIO(45:40), CLK48, JTCK, JTMS, JTDI/RMODE#, JTRST#, BKTGIO#, TPX(1:0), TPY(1:0)



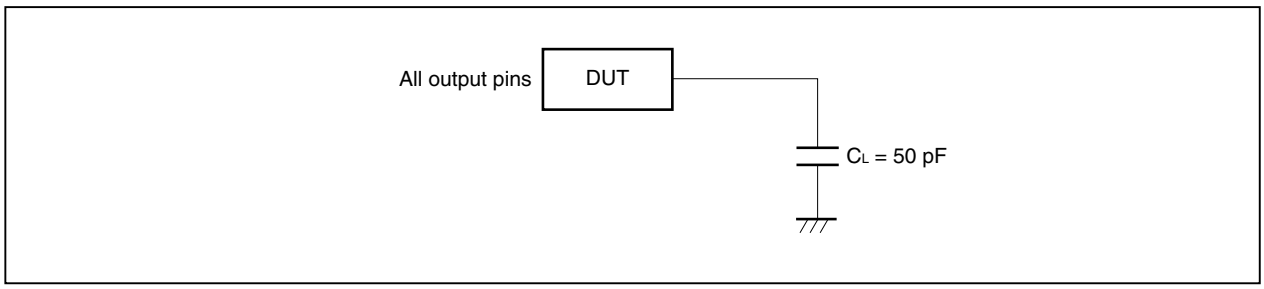
(b) A(22:15)/GPIO(61:54), POWER, RSTSW#, RTCRST#, CF1_RESET/DBUS32, RxD0, TxD0/CLKSEL2, RxD2/IRDIN, TxD2/IRDOUT/MIPS16EN, CTS2#/BITCLK/SCLK, DTR2#/SDATAOUT/SDO/DIVMODE0, RTS2#/SYNC/WS/DIVMODE1, DCD2#/SDATAIN/SDI, DSR2#/SRESET#, UOC, CF1_DIR/KPORT4/GPIO39, CF1_EN#/KPORT5/GPIO38, CF1_VCCEN#/KSCAN4/GPIO37, CF0_CD(2:1)#/GPIO(36:35), CF0_IOIS16#/GPIO34, CF_WAIT#/GPIO33, CF0_CE(2:1)#/GPIO(32:31), CF0_STSCHG#/GPIO30, CF0_READY/GPIO29, CF0_RESET/GPIO28, CF0_DIR/GPIO27, CF0_EN#/GPIO26, CF_REG#/GPIO25, CF0_VCCEN#/GPIO24, SCK/KSCAN11/GPIO23, SI/KSCAN10/GPIO22, SO/KSCAN9/GPIO21, FRM/KSCAN8/GPIO20, RTS0#/GPIO19/CLKSEL1, CTS0#/GPIO18, DTR0#/RTS1#/GPIO17/CLKSEL0, DCD0#/GPIO16, DSR0#/CTS1#/GPIO15, RxD1/SCL1/GPIO14, TxD1/SDA1/GPIO13, SCL0/KPORT7/GPIO12, SDA0/KPORT6/GPIO11, PWM(2:0)/KSCAN(5:7)/GPIO(10:8), KPORT(3:0)/GPIO(7:4), KSCAN(3:0)/GPIO(3:0)



AC test output test points



Load condition



(1) Clock parameters

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU core operating frequency	f_{AClock}	CLKSEL(2:0) = 111 Note		147.4		MHz
		CLKSEL(2:0) = 110		131.1		MHz
		CLKSEL(2:0) = 101		118.0		MHz
		CLKSEL(2:0) = 100		98.3		MHz
		CLKSEL(2:0) = 011		90.7		MHz
		CLKSEL(2:0) = 010		84.1		MHz
		CLKSEL(2:0) = 001		78.5		MHz
		CLKSEL(2:0) = 000		73.7		MHz
TClock, SDCLK frequency	f_{TClock}	DIVMODE(1:0) = 11 Note	18.432	f_{AClock}/1	65.55	MHz
		DIVMODE(1:0) = 10	18.432	f_{AClock}/2	65.55	MHz
		DIVMODE(1:0) = 01	18.432	f_{AClock}/3	65.55	MHz
		DIVMODE(1:0) = 00 Note	18.432	f_{AClock}/4	65.55	MHz
MasterOut frequency	$f_{MasterOut}$			f_{TClock}/4		MHz
PCIClock frequency	$t_{PCIClock}$	PCICLKDIV(1:0) = 00		f_{TClock}/8	32.78	MHz
		PCICLKDIV(1:0) = 01		f_{TClock}/4	32.78	MHz
		PCICLKDIV(1:0) = 10 Note		f_{TClock}/2	32.78	MHz
		PCICLKDIV(1:0) = 11 Note		f_{TClock}/1	32.78	MHz
LClock frequency	f_{LClock}	LCLKDIV(1:0) = 11 Note		f_{TClock}/1		MHz
		LCLKDIV(1:0) = 01		f_{TClock}/2		MHz
		LCLKDIV(1:0) = 10		f_{TClock}/3		MHz
		LCLKDIV(1:0) = 00		f_{TClock}/4		MHz
PClock frequency	f_{PClock}	PCLKDIV(1:0) = 00	18.432	f_{TClock}/1	32.78	MHz
		PCLKDIV(1:0) = 01	18.432	f_{TClock}/2	32.78	MHz
		PCLKDIV(1:0) = 10	18.432	f_{TClock}/4	32.78	MHz
		PCLKDIV(1:0) = 11 Note	18.432	f_{TClock}/8	32.78	MHz
ECU_SysClock frequency	$f_{ECU\_SysClock}$	ECUSYSCLKDIV(1:0) = 00 Note		f_{TClock}/1	32.78	MHz
		ECUSYSCLKDIV(1:0) = 01		f_{TClock}/2	32.78	MHz
		ECUSYSCLKDIV(1:0) = 10		f_{TClock}/4	32.78	MHz
		ECUSYSCLKDIV(1:0) = 11		f_{TClock}/8	32.78	MHz

Note These values cannot be set in the current VR4181A.

Remarks 1. The settings of the CLKSEL(2:0) and DIVMODE(1:0) signals are sampled when the RTCRST# signal changes to high level.

2. PCICLKDIV(1:0): Bits 9 and 8 of the CLKDIVCTRL register in the CCU. Set these bits before starting use of the on-chip peripheral PCI unit.

3. LCLKDIV(1:0): Bits 5 and 4 of the EXIBUCFG register in the EXIBU. Set these bits before setting the timing parameters for each register of the EXIBU.

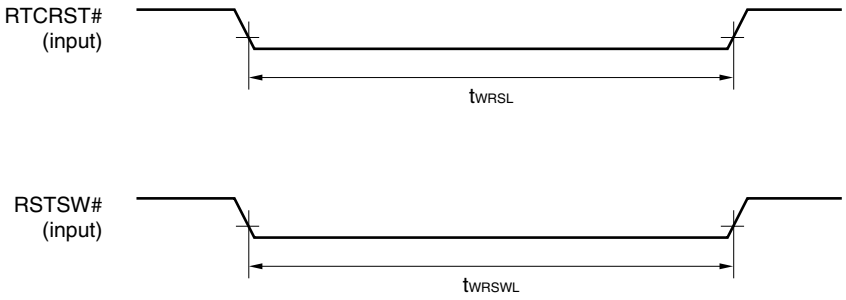
4. PCLKDIV(1:0): Bits 1 and 0 of the CLKDIVCTRL register in the CCU.

5. ECUSYSCLKDIV(1:0): Bits 5 and 4 of the CLKDIVCTRL register in the CCU. Set these bits before starting use of the ECU.

(2) Reset parameters

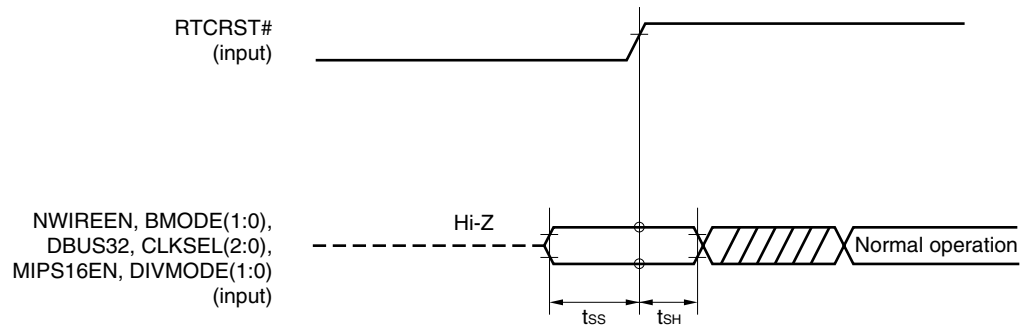
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
RTC reset input low-level width	t_{WRSL}	Applies to RTCRST# signal	600		ms
RSTSW reset input low-level width	t_{WRSWL}	Applies to RSTSW# signal	100		μs

Remark If the low-level width of reset input is the MIN. value or lower, a reset sequence may not be started.



(3) Initial setting parameters

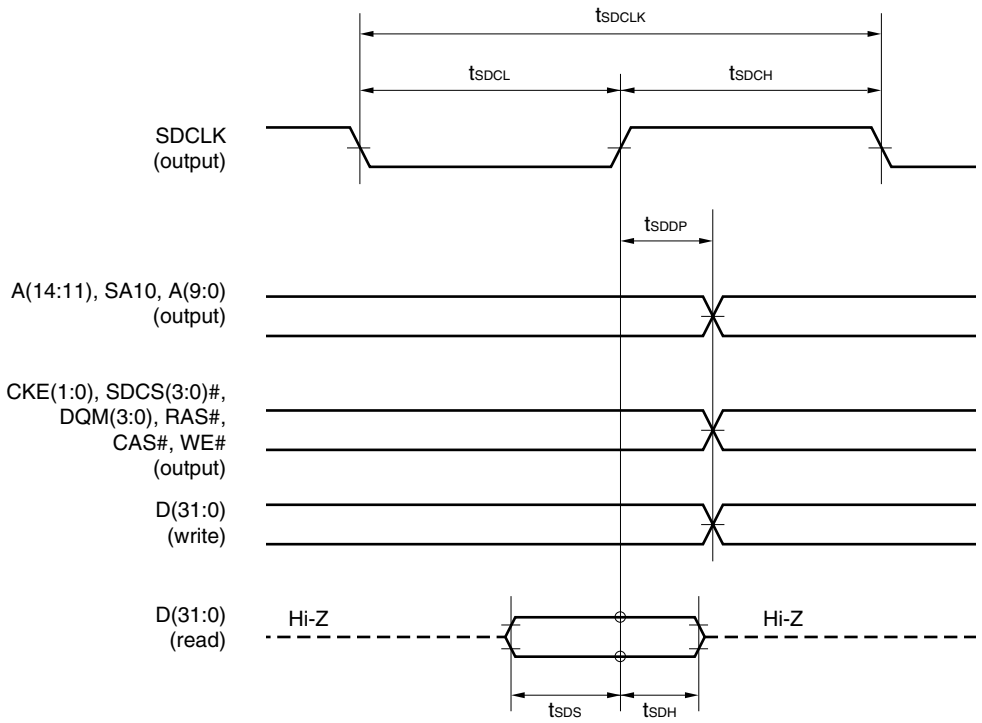
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Setup time (to RTCRST#↑)	t_{SS}		91.6		μs
Hold time (from RTCRST#↑)	t_{SH}		–10		μs



Remark The circles indicate the sampling timing.

(4) SDRAM, SyncFlash interface (MCU) parameters

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SDCLK frequency	f_{SDCLK}			65.55	MHz
SDCLK cycle	t_{SDCLK}		15.26		ns
SDCLK high-level width	t_{SDCH}		3.5		ns
SDCLK low-level width	t_{SDCL}		3.5		ns
Output delay time (from SDCLK↑)	t_{SDDP}		1.5	11.7	ns
Data setup time	t_{SDS}		6.2		ns
Data hold time	t_{SDH}		2.9		ns



Remark The circles indicate the sampling timing.

(5) ROM, flash memory, SRAM, ISA interface (EXIBU) parameters

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
TClock frequency	f_{TClock}			65.55	MHz
TClock cycle	t_{TClock}		15.26		ns
LClock frequency	f_{LClock}			32.78	MHz
LClock cycle	t_{LClock}		30.52		ns
Output delay time	t_{EXD}		0	12	ns
Data input setup time	t_{EXS}		5		ns
Data input hold time	t_{EXH}		0		ns
Data output float delay time	t_{EXZ}			10	ns
Data output setup time (from command signal↓)	t_{EXCL}		0		ns
IORDY input hold time	t_{EXRDYH}		0		ns
IOCS16# input hold time	$t_{EXCS16H}$		0		ns
DRQn# input inactive setup time	t_{DRQNEG}		20		ns

Remarks 1. n = 0, 1

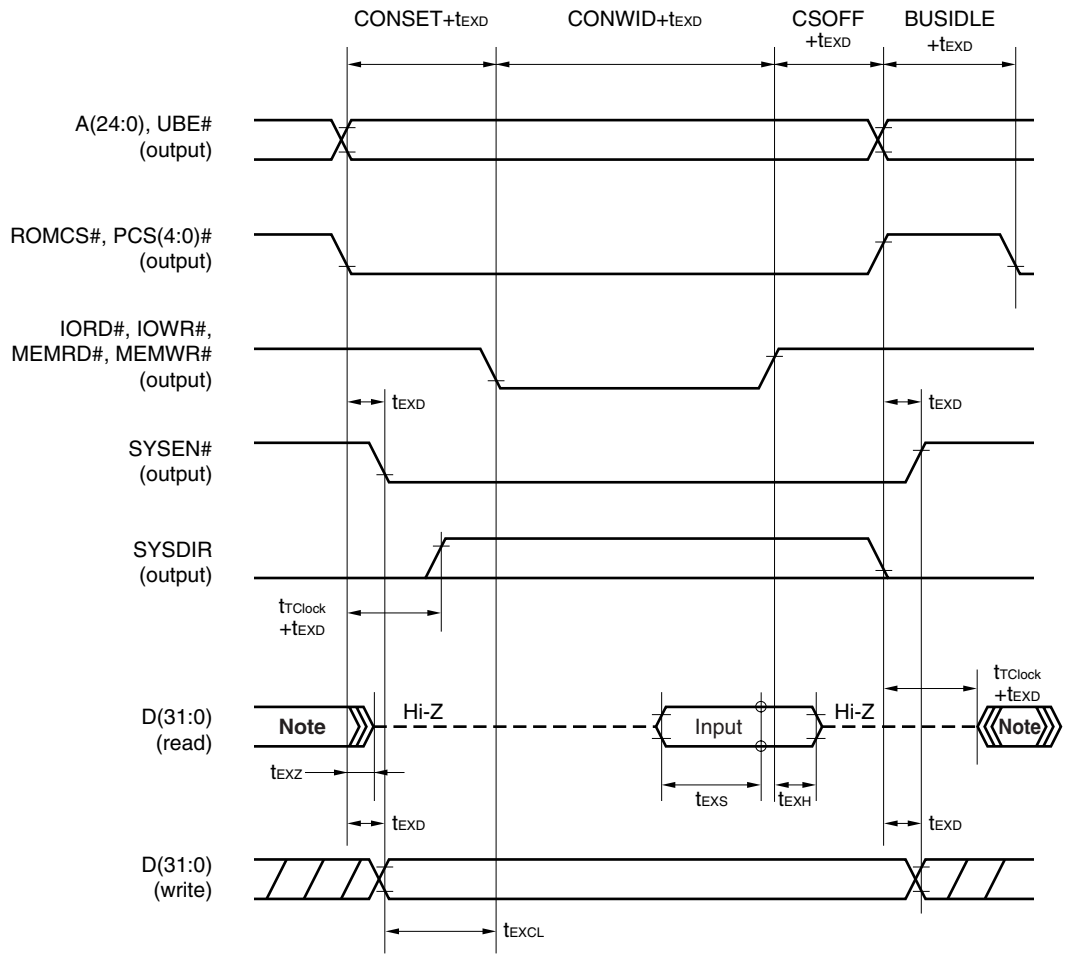
2. TClock is generated by dividing AClock in accordance with the setting of the DIVMODE(1:0) signals when the RTCRST# signal changes to high level.

After releasing the RTC reset, the division ratio of TClock can be changed by setting the PMUDIVREG register.

3. LClock is generated by dividing Tclock in accordance with the setting of the LCLKDIV(1:0) bits of the EXIBUCFG register in the EXIBU.

4. The MEMRD#, MEMWR#, IORD#, and IOWR# signals are called as command signals for the external system bus interface.

(a) Non-READY mode timing

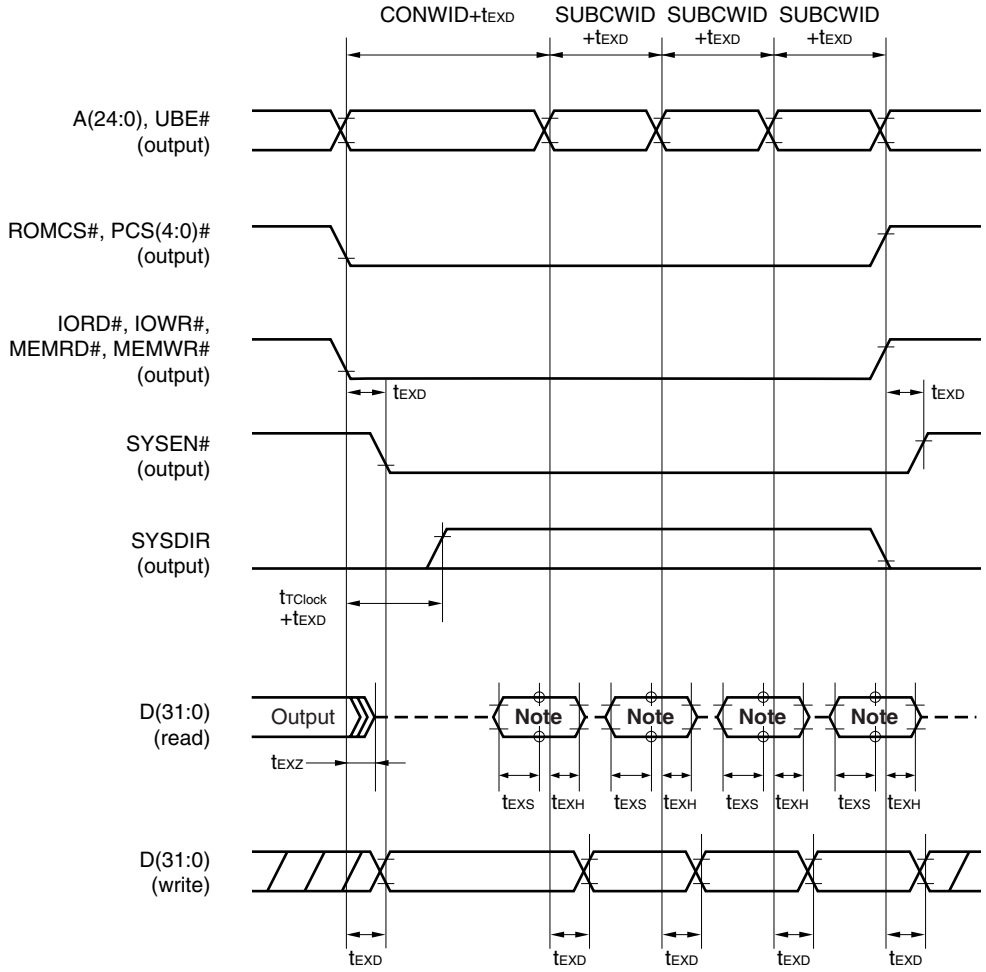


Note Output

Remarks 1. CONSET, CONWID, CSOFF, and BUSIDLE are the timing parameters that can be changed by setting registers of the EXIBU. Each timing parameter is defined as the number of LClock cycles.

2. The circles indicate the sampling timing.

(b) Page access timing (CONSET = 0, CSOFF = 0)



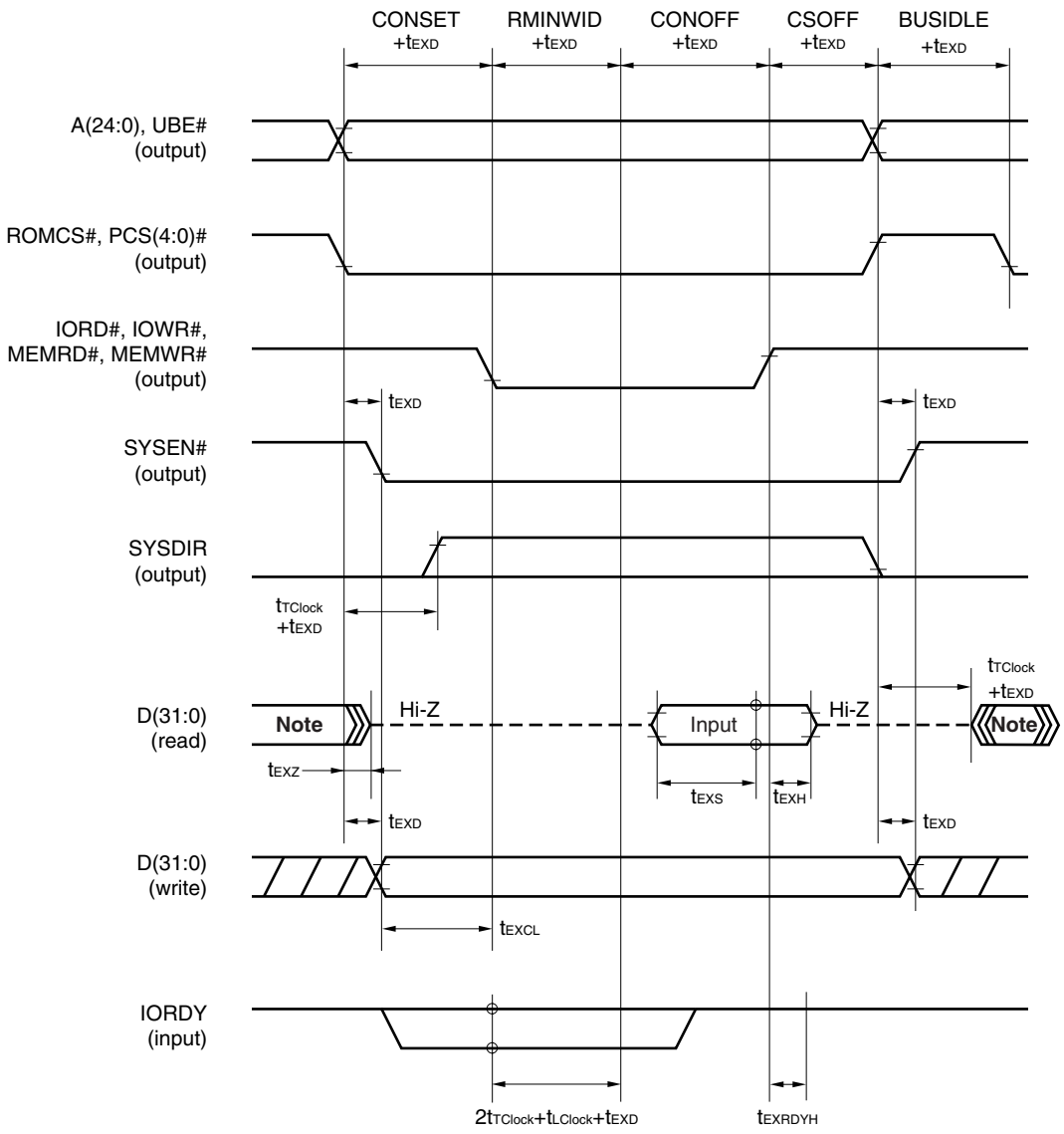
Note Input

Remarks 1. CONWID and SUBCWID are the timing parameters that can be changed by setting registers of the EXIBU. Each timing parameter is defined as the number of LClock cycles.

2. The circles indicate the sampling timing.

3. The broken lines indicate high impedance.

(c) READY mode timing (RDYSYN = 1)

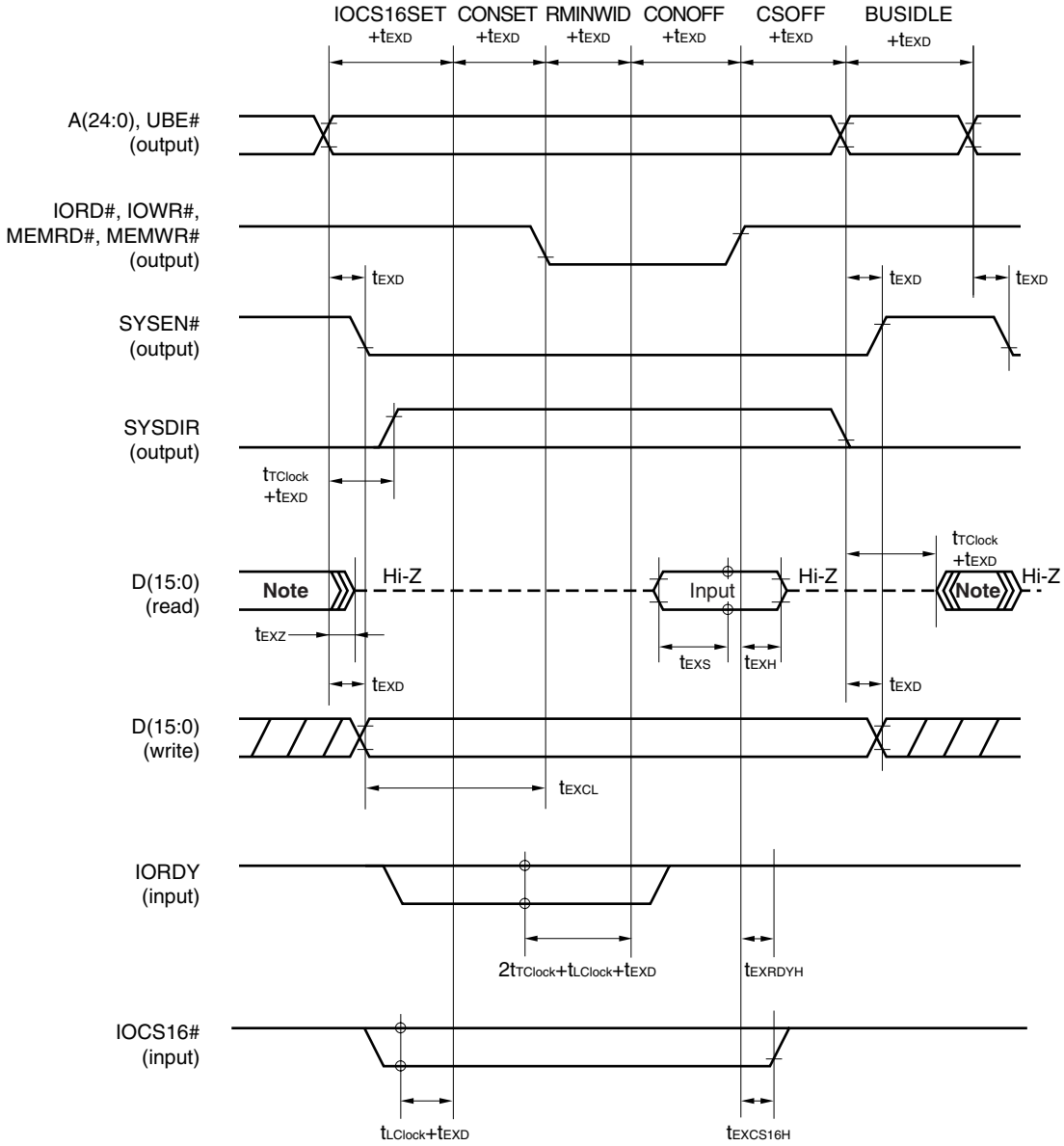


Note Output

Remarks 1. CONSET, CSOFF, RMINWID, CONOFF, and BUSIDLE are the timing parameters that can be changed by setting registers of the EXIBU. Each timing parameter is defined as the number of LClock cycles.

2. The circles indicate the sampling timing.

(d) External ISA bus space access (READY mode) timing (RDYSYN = 1)

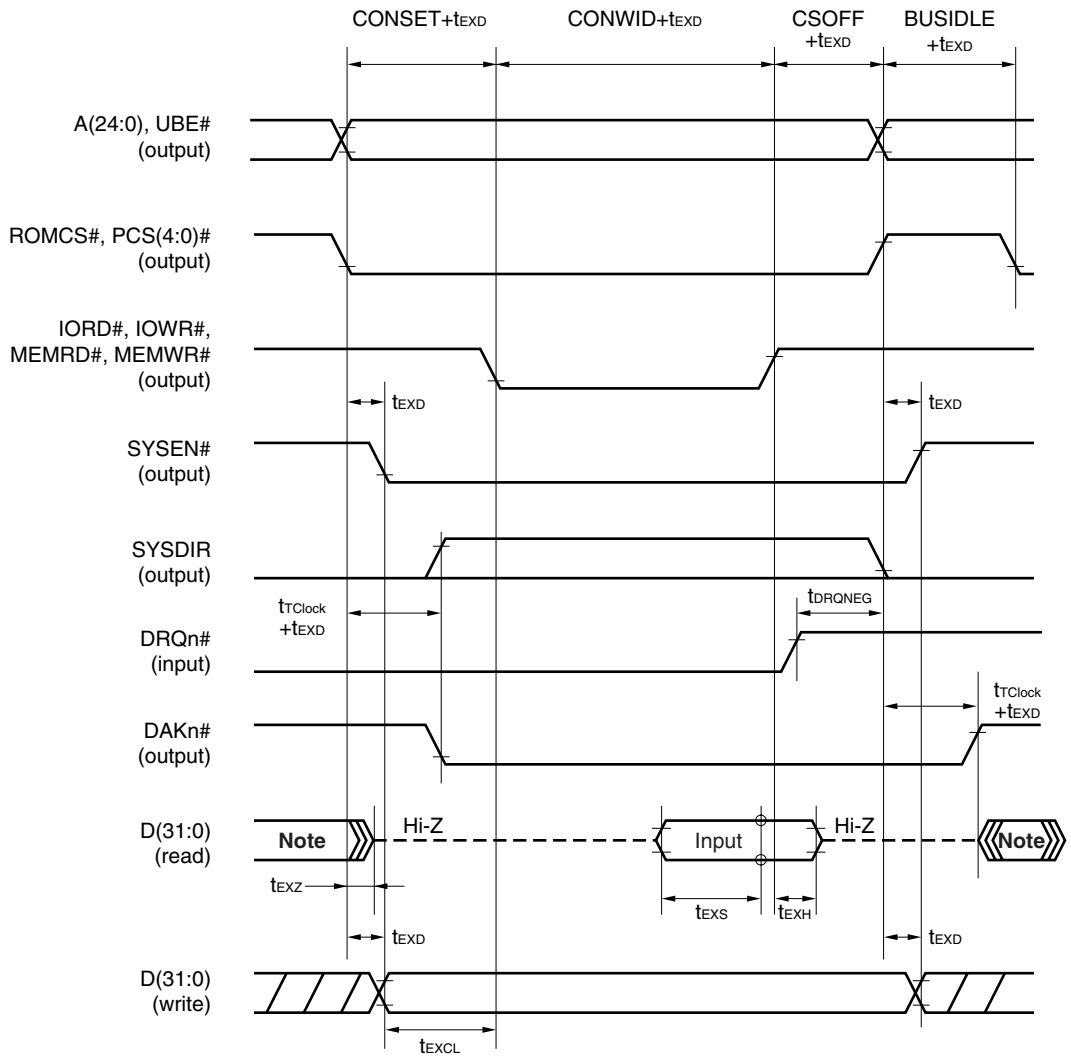


Note Output

Remarks 1. IOCS16SET, CONSET, CSOFF, RMINWID, CONOFF, and BUSIDLE are the timing parameters that can be changed by setting registers of the EXIBU. Each timing parameter is defined as the number of LClock cycles.

2. The circles indicate the sampling timing.

(e) DMA transfer timing



Note Output

Remarks 1. CONSET, CONWID, CSOFF, and BUSIDLE are the timing parameters that can be changed by setting registers of the EXIBU. Each timing parameter is defined as the number of LClock cycles.

2. The circles indicate the sampling timing.

3. n = 0, 1

(6) CompactFlash/PC Card/ATA (IDE) interface (ECU) parameters

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
TClock frequency	f_{TClock}			65.55	MHz
TClock cycle	t_{TClock}		15.26		ns
LClock frequency	f_{LClock}			32.78	MHz
LClock cycle	t_{LClock}		30.52		ns
ECU_SysClock frequency	$f_{ECU\_SysClock}$			32.78	MHz
ECU_SysClock cycle	$t_{ECU\_SysClock}$		30.52		ns
Output delay time (EXIBU)	t_{EXD}		0	12	ns
Output delay time (ECU)	t_{ECUD}		0	TBD	ns
Data input setup time	t_{EXS}		5		ns
Data input hold time	t_{EXH}		0		ns
Data output float delay time	t_{EXZ}			10	ns
Data output setup time (to command signal↓)	t_{EXCL}		0		ns
CF_WAIT# input hold time	$t_{ECURDYH}$		0		ns
CF0_IOIS16# input hold time	$t_{ECUCS16H}$		0		ns

Remarks 1. TClock is generated by dividing AClock in accordance with the setting of the DIVMODE(1:0) signals when the RTCRST# signal changes to high level. After releasing the RTC reset, the division ratio of TClock can be changed by setting the PMUDIVREG register.

2. LClock is generated by dividing TClock in accordance with the setting of the LCLKDIV(1:0) bits of the EXIBUCFG register in the EXIBU.

3. ECU_SysClock is generated by dividing TClock in accordance with the setting of the ECUSYSCLKDIV(1:0) bits of the CLKDIVCTRL register in the CCU.

4. MEMRD#, MEMWR#, IORD#, and IOWR# signals are called as command signals for the external system bus interface.

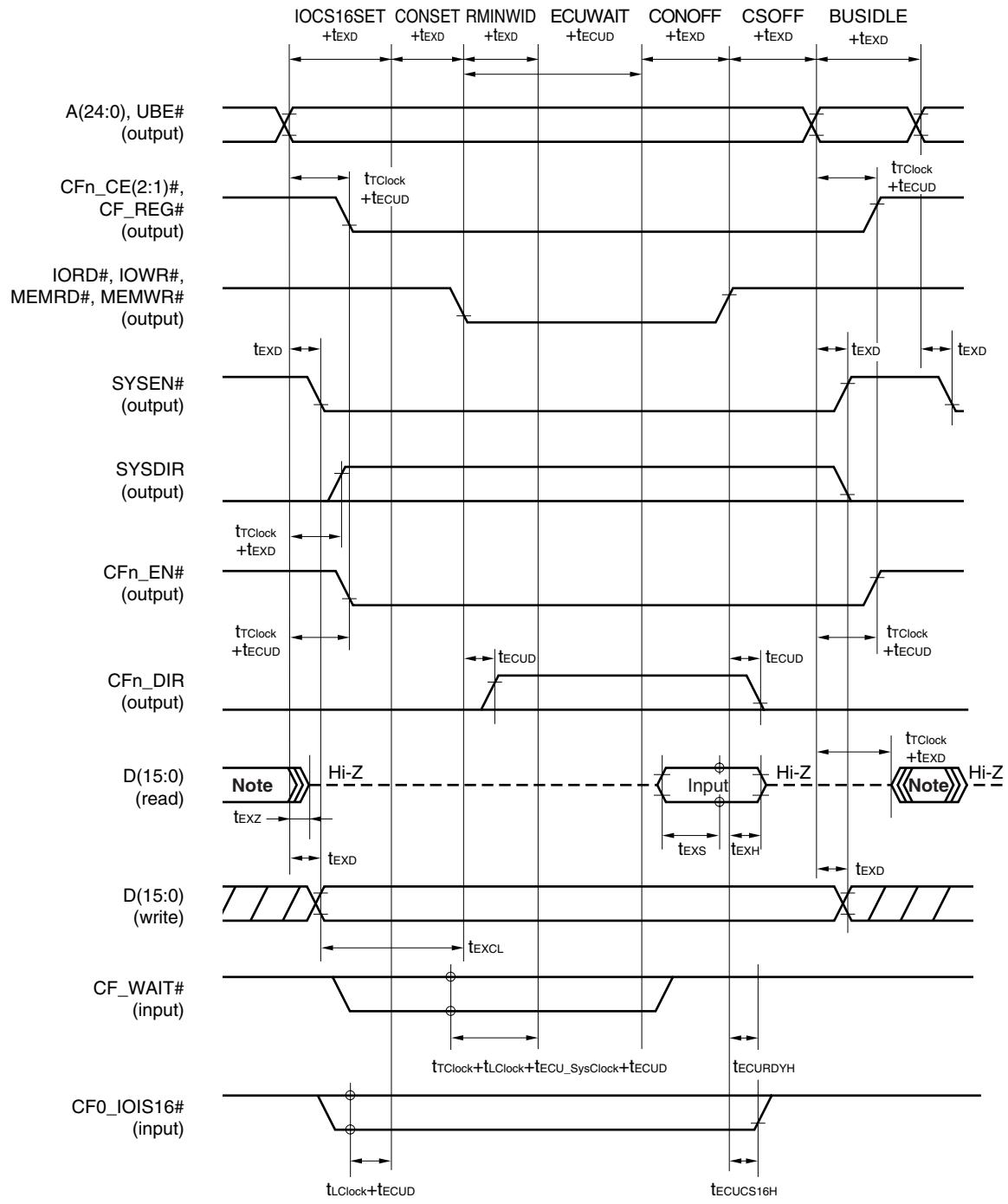
(a) Relationship between ECU bus cycle type and ECUWAIT

Bus Cycle	Number of Wait Cycles	ECUWAIT Value (ns)	
		MIN.	MAX.
16-bit I/O cycle (IOnWT = 1)	2	$t_{ECU\_SysClock} \times 2$	
16-bit I/O cycle(IOnWT = 0)	3	$t_{ECU\_SysClock} \times 3$	
8-bit I/O cycle (Wn_IOWS = 1)	4	$t_{ECU\_SysClock} \times 4$	
8-bit I/O cycle (Wn_IOWS = 0)	5	$t_{ECU\_SysClock} \times 5$	
16-bit memory cycle (ZWSEN = 1 and M16W(1:0) = 0)	0		
16-bit memory cycle (ZWSEN = 0 and M16W(1:0) = N)	N + 1	$t_{ECU\_SysClock} \times (N + 1)$	
8-bit memory cycle (ZWSEN = 1)	0	0	
8-bit memory cycle (ZWSEN = 0)	5	$t_{ECU\_SysClock} \times 4$	

Remarks 1. IOnWT, Wn_IOWS, ZWSEN, and M16W(1:0) are bits of the register in the ECU.

2. n = 0, 1

(b) External ISA bus space access (READY mode) timing (RDYSYN = 1)



Note Output

Remarks 1. IOCS16SET, CONSET, CSOFF, RMINWID, CONOFF, and BUSIDLE are the timing parameters that can be changed by setting registers of the EXIBU. Each timing parameter is defined as the number of LClock cycles.

2. The circles indicate the sampling timing.

3. n = 0, 1

(7) USB interface (USBHU, USBFU) parameters

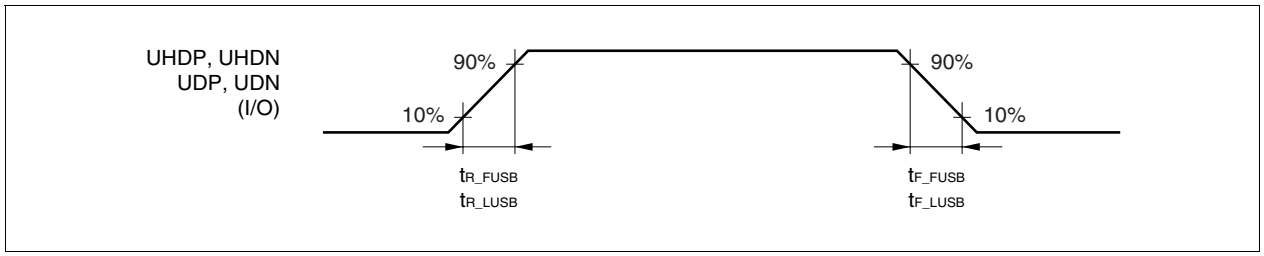
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Rise time[Note 1]	t_{R_FUSB}	Fullspeed (12 Mbps) mode	4	20	ns
	t_{R_LUSB}	Low speed (1.5 Mbps) mode	75	300	ns
Fall time[Note 1]	t_{F_FUSB}	Fullspeed (12 Mbps) mode	4	20	ns
	t_{F_LUSB}	Low speed (1.5 Mbps) mode	75	300	ns
Vp-p output potential width[Notes 1, 2]	t_{RFM_FUSB}	Fullspeed (12 Mbps) mode	90	111	%
	t_{RFM_LUSB}	Low speed (1.5 Mbps) mode	80	125	%

Notes 1. Precision tests have not been performed. Only guaranteed as design characteristics.

2. Indicated by the following expressions.

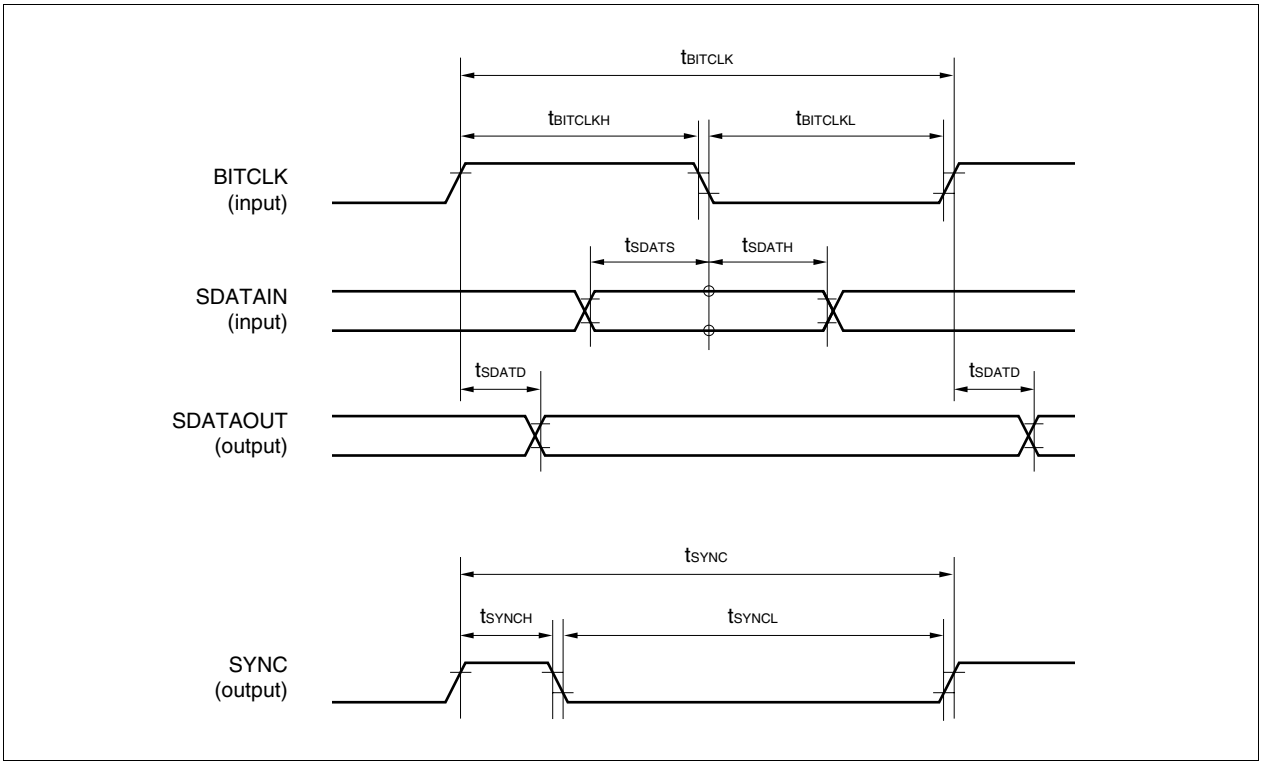
$t_{RFM\_FUSB} = t_{R\_FUSB}/t_{F\_FUSB}$

$t_{RFM\_LUSB} = t_{R\_LUSB}/t_{F\_LUSB}$



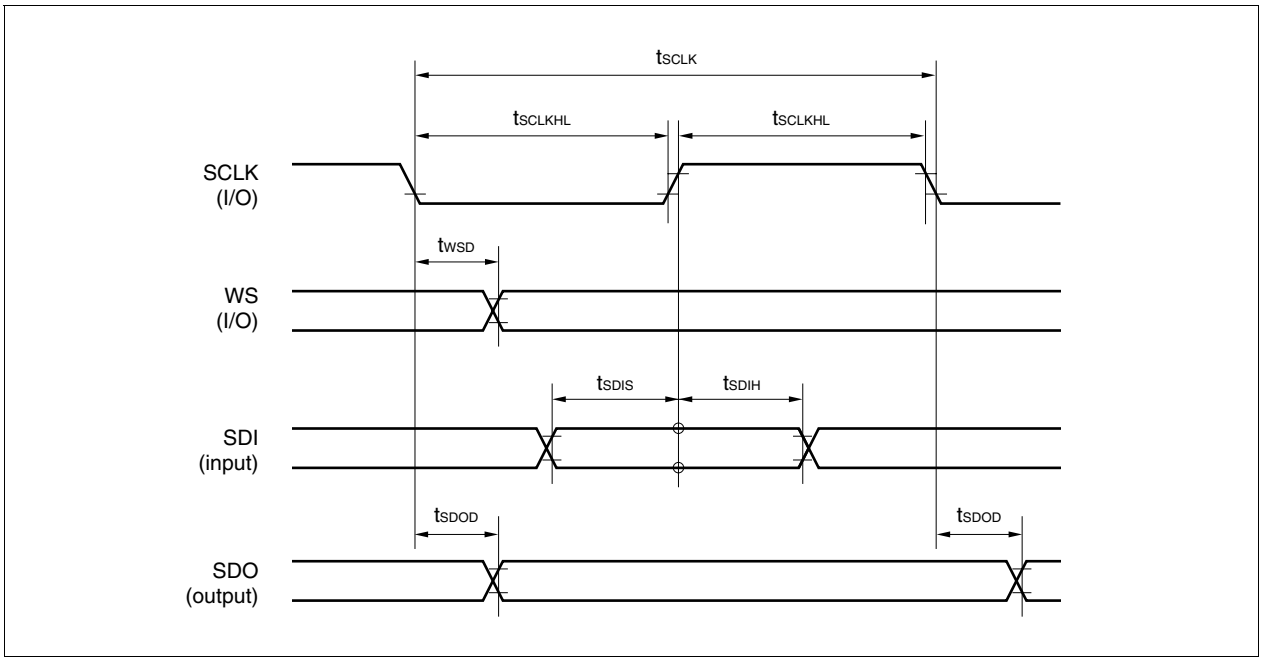
(8) AC97 interface (AC97U) parameters

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
BITCLK frequency	f_{BITCLK}			12.288		MHz
BITCLK cycle	t_{BITCLK}			81.4		ns
BITCLK high-level width	$t_{BITCLKH}$		36	40.7	45	ns
BITCLK low-level width	$t_{BITCLKL}$		36	40.7	45	ns
SYNC frequency	f_{SYNC}			48		kHz
SYNC cycle	t_{SYNC}			20.8		μs
SYNC high-level width	t_{SYNCH}			1.3		μs
SYNC low-level width	t_{SYNCL}			19.5		μs
SDATAIN input setup time (to BITCLK↓)	t_{SDATS}		10			ns
SDATAIN input hold time (to BITCLK↓)	t_{SDATH}		10			ns
SDATAOUT output delay time (to BITCLK↑)	t_{SDATD}				25	ns



(9) I^2S interface (I2SU) parameters

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLK frequency	f_{SCLK}			6.114	MHz
SCLK cycle	t_{SCLK}		163		ns
SCLK high-/low-level width	t_{SCLKHL}		$t_{SCLK}/2 - 20$	$t_{SCLK}/2 + 20$	ns
SDI input setup time (to SCLK↑)	t_{SDIS}		30		ns
SDI input hold time (from SCLK↑)	t_{SDIH}		30		ns
SDO output delay time (from SCLK↓)	t_{SDOD}			30	ns
WS delay time (from SCLK↓)	t_{WSD}			30	ns



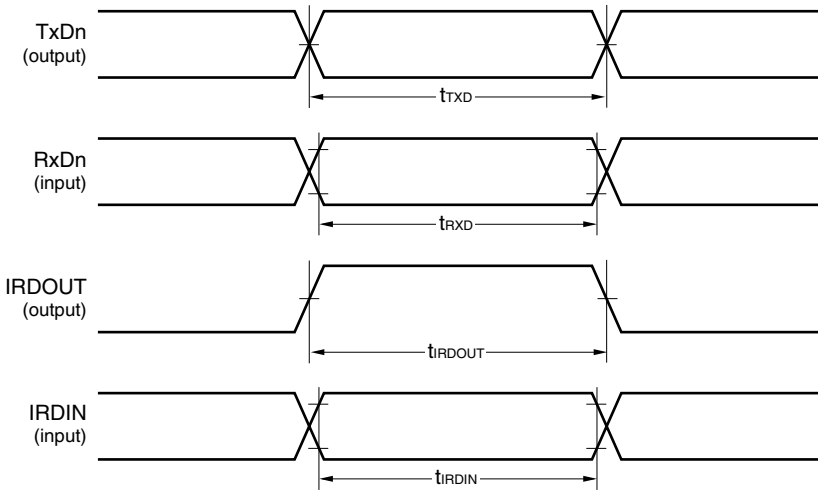
(10) Serial interface (SIU) parameters

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
TxD0, TxD1, TxD2 output pulse width	t_{TXD}		N – 0.1	N + 0.1	μs
RxD0, RxD1, RxD2 input pulse width	t_{RXD}		(9/16) × N		μs
IRDOUT high-level output pulse width	t_{IRDOUT}		(3/16) × N – 0.1	(3/16) × N + 0.1	μs
IRDIN input pulse width	t_{IRDIN}		1		μs

Remark N is the data transfer cycle per bit determined by the divisor of the baud rate generator set in the SIUDLL and SIUDLM registers.

Baud Rate (bps)	Divisor (DLM(7:0)||DLL(7:0))	N (μs)
50	23040	20000.00
75	15360	13333.33
110	10473	9090.91
134.5	8565	7434.94
150	7680	6666.67
300	3840	3333.33
600	1920	1666.67
1200	960	833.33
1800	640	555.56
2000	576	500.00
2400	480	416.67
3600	320	277.78
4800	240	208.33
7200	160	138.89
9600	120	104.17
19200	60	52.08
38400	30	26.04
57600	20	17.36
115200	10	8.68
128000	9	7.81
144000	8	6.94
192000	6	5.21
230400	5	4.34
288000	4	3.47
384000	3	2.60
576000	2	1.74
1152000	1	0.868

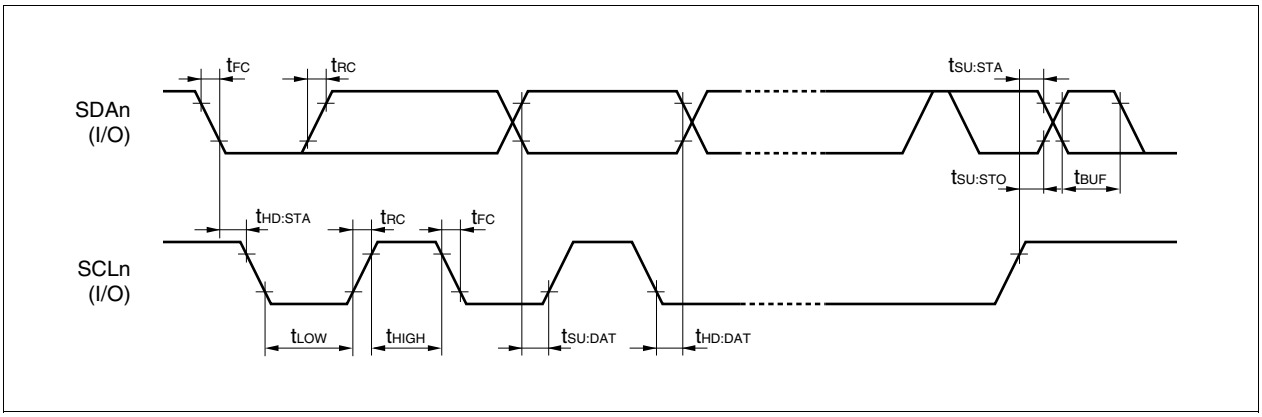
Remark Baud rate = (18.432 MHz/16)/(value set in the SIUDLM or SIUDLL register)



Remark n = 0 to 2

(11) I²C bus interface (I2CU) parameters (μPD30181AY only)

Parameter	Symbol	Condition	Normal Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLn frequency	f_{SCL}		0	100	0	400	kHz
Start condition hold time	$t_{HD:STA}$		4.0		0.6		μs
SCLn low-level width	t_{LOW}		4.7		1.3		μs
SCLn high-level width	t_{HIGH}		4.0		0.6		μs
Rise time	t_{RC}			1.0		0.3	μs
Fall time	t_{FC}			0.3		0.3	μs
Data setup time	$t_{SU:DAT}$		0.25		0.1		μs
Data retention time	$t_{HD:DAT}$		0		0		μs
Repeat start setup time	$t_{SU:STA}$		4.7		0.6		μs
Stop condition setup time	$t_{SU:STO}$		4.0		0.6		μs
Bus release time	t_{BUF}		4.7		1.3		μs

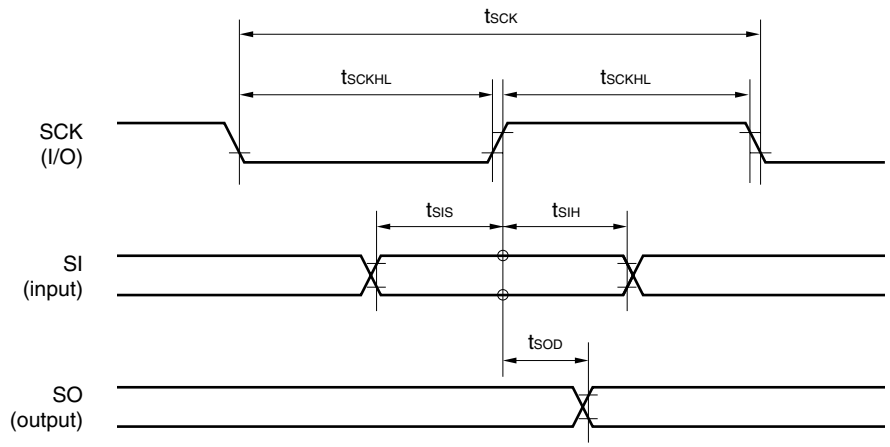


Remark n = 0, 1

(12) Clocked serial interface (CSI) parameters

Parameter	Symbol	Condition	MIN.	MAX.	Unit
SCK frequency	f_{SCK}			4.608	MHz
SCK cycle	t_{SCK}		217		ns
SCK high-/low-level width	t_{SCKHL}		$t_{SCK}/2 - 20$	$t_{SCK}/2 + 20$	ns
SI input setup time (to SCK edge[Note])	t_{SIS}		50		ns
SI input hold time (from SCK edge[Note])	t_{SIH}		50		ns
SO output delay time (from SCK edge[Note])	t_{SOD}			50	ns

Note The SCK edge used differs depending on the settings of the CKMD and CKPOL bits of the CSIMODE register.

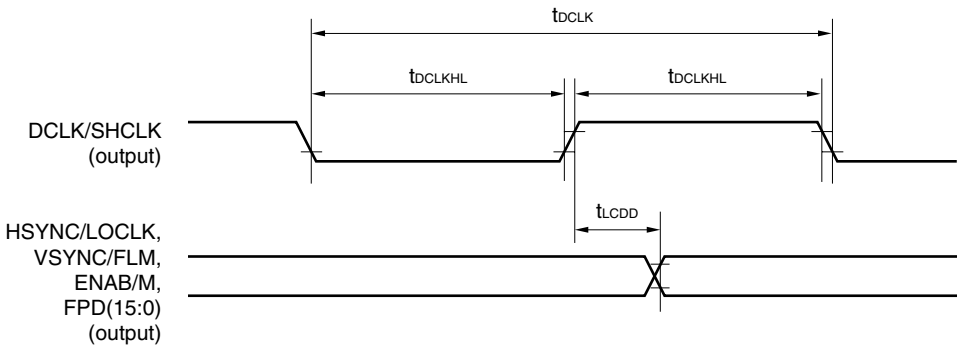


Remark This diagram shows the timing when using the SCK rising edge (CKMD = 0 and CKPOL = 0, or CKMD = 1 and CKPOL = 1).

(13) LCD interface (LCU) parameters

Parameter	Symbol	Condition	MIN.	MAX.	Unit
DCLK/SHCLK frequency	f_{DCLK}			32.775	MHz
DCLK/SHCLK cycle	t_{DCLK}		30		ns
DCLK/SHCLK high-/low-level width	t_{DCLKHL}		$t_{DCLK}/2 - 5$	$t_{DCLK}/2 + 5$	ns
Output delay time (from DCLK/SHCLK edge[Note])	t_{LCDD}	Applies to HSYNC/LOCLK, VSYNC/FLM, ENAB/M, and FPD(15:0) signals		30	ns

Note The DCLK/SHCLK edge used differs depending on the setting of the SCLKPOL bit of the LCDCTRLREG register.



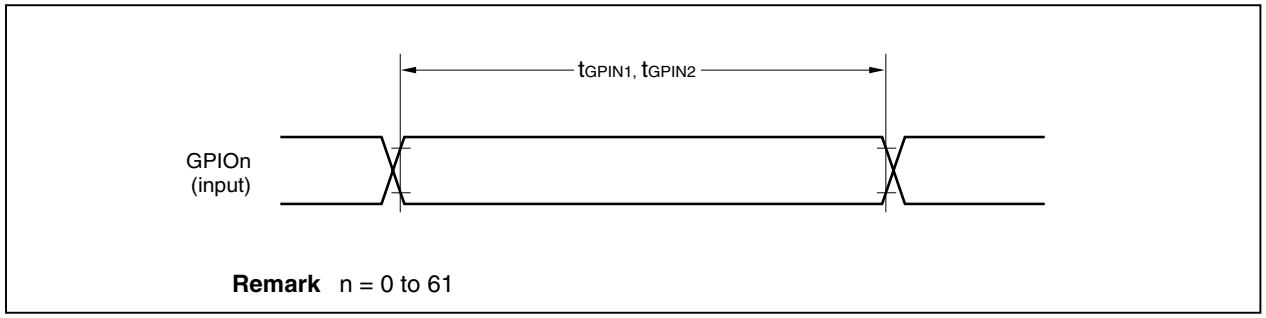
Remark This diagram shows the timing when using the DCLK/SHCLK rising edge (SCLKPOL = 1).

(14) GPIO interface (GIU) parameters

Parameter	Symbol	Condition	MIN.	MAX.	Unit
GPIO input level width	t_{GPIN1}	Restoring from Hibernate mode when level trigger is selected.	100		μs
	t_{GPIN2}	Interrupt input when level trigger is selected.	($t_{TClock} \times 4$) $\times 3$		ns
GPIO input rise time[Note]	t_{GPINR}	GPIO(61:40) pins		10	ns
	t_{GPINR2}	GPIO pins other than above		200	ns
GPIO input fall time[Note]	t_{GPINF}	GPIO(61:40) pins		10	ns
	t_{GPINF2}	GPIO pins other than above		200	ns

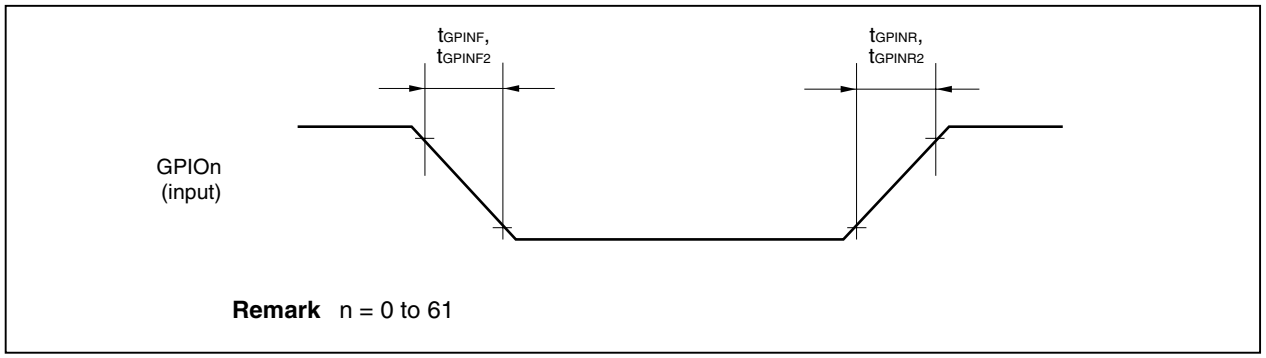
Note Precision tests have not been performed. Only guaranteed as design characteristics.

(a) GPIO input level width



Remark n = 0 to 61

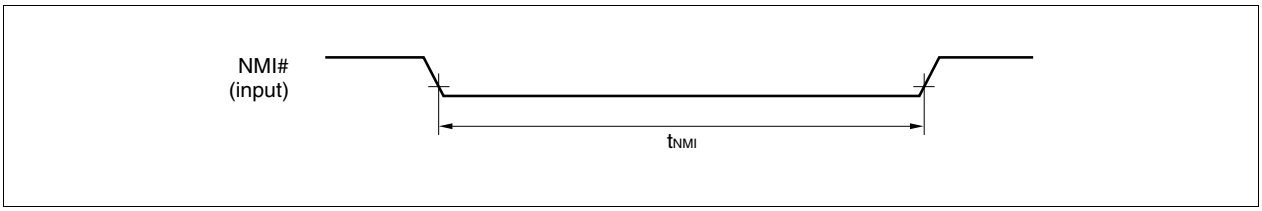
(b) GPIO input rise/fall time



Remark n = 0 to 61

(15) NMI parameters

Parameter	Symbol	Condition	MIN.	MAX.	Unit
NMI# input low-level width	t_{NMI}		100		μs



A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD25} = 2.3 to 2.7 V, V_{DD33} = 3.0 to 3.6 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Zero-scale error[Notes 1, 2]	ZSE			±4.0		LSB
Full-scale error[Notes 1, 2]	RSE			±5.0		LSB
Integral linearity error[Notes 1, 2]	INL			±3.0		LSB
Differential linearity error[Notes 1, 2]	DNL			±3.0		LSB
Analog input voltage[Note 1]	VIAN		–0.3		V_{DDAD} + 0.3	V
Analog input equivalent resistance[Note 1]	R_{AIN}			1.53		kΩ
Analog input equivalent capacitance[Note 1]	C_{AIN}			6.5		pF
Analog signal source allowable output impedance[Note 1]	R_{EXOUT}	When pin input capacitance C_I = 3 pF			3.5	kΩ

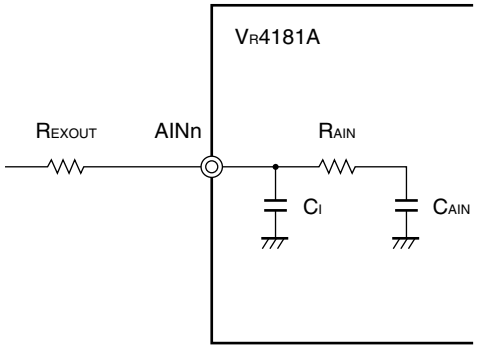
Notes 1. Applies to TPX(1:0), TPY(1:0), and AIN(3:0) pins.

2. Excluding quantization error.

Remark LSB: Least significant bit

V_{DDAD}: Voltage supplied to VDDAD pin

A/D converter input equivalent circuit



Remark n = 0 to 3

D/A Converter Characteristics (T_A = –40 to +85°C, V_{DD25} = 2.3 to 2.7 V, V_{DD33} = 3.0 to 3.6 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Integral linearity error[Notes 1, 2]	INL			±3.0		LSB
Differential linearity error[Notes 1, 2]	DNL			±3.0		LSB
String unit resistor	R_{ST}			4		Ω
String output equivalent resistor	R_{STOUT}			1110		Ω

Notes 1. Applies to AOUT pin.

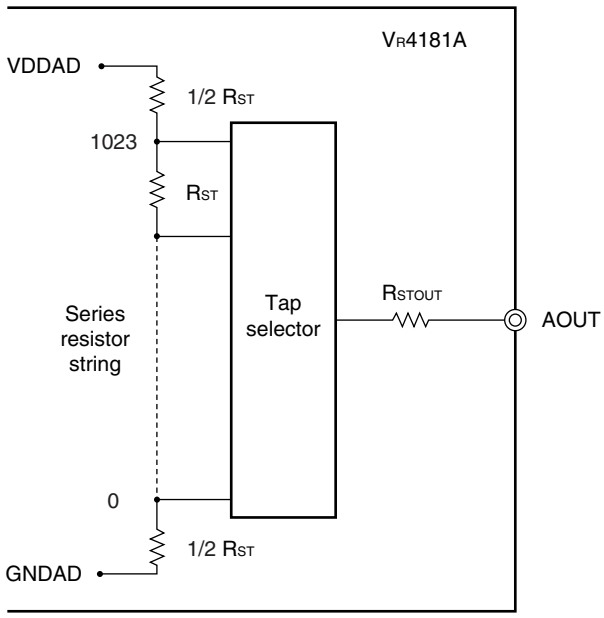
2. Excluding quantization error.

Remark LSB: Least significant bit

Cautions 1. The output impedance of the D/A converter is too large to latch the current from AOUT pin. If the load input impedance is small, insert a buffer amplifier between the load and the AOUT pin. Make the wiring between the buffer amplifier and load as short as possible.
If the wiring is long, processing is required such as enclosing the wiring in a with ground pattern.

2. The output voltage of the D/A converter changes in steps, so use the output signal from the D/A converter after passing it through a low pass filter.

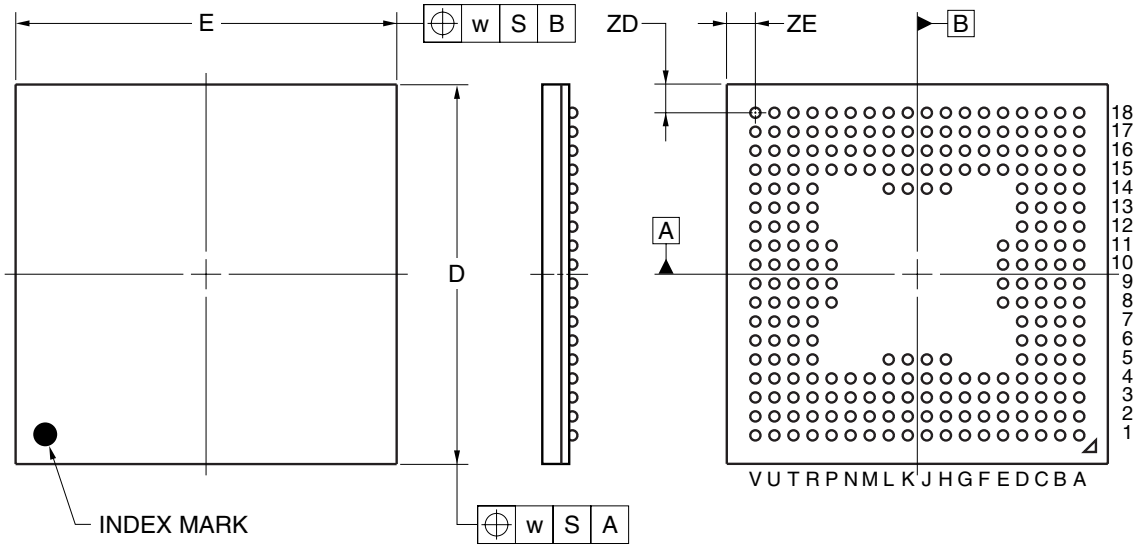
D/A converter output equivalent circuit

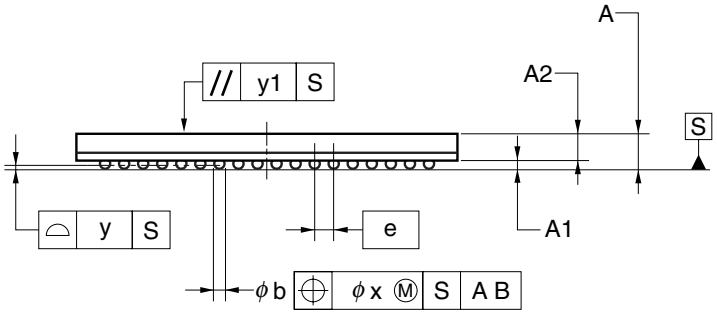


Remark The series resistor string is connected between the reference voltage for the A/D converter (VDDAD) and GND (GNDAD) for the A/D converter. To make the 1024 equivalent voltage steps between the two pins, this circuit consists of 1023 equivalent unit resistors (R_{ST}) and two resistors with a resistance of half R_{ST}. The equivalent output impedance of the AOUT pin is the value calculated by adding R_{STOUT} to the total R_{ST} value corresponding to the selected voltage step.

3. PACKAGE DRAWING

240-PIN PLASTIC FBGA (16x16)





(UNIT:mm)

ITEM	DIMENSIONS
D	16.00±0.10
E	16.00±0.10
w	0.20
A	1.48±0.10
A1	0.35±0.06
A2	1.13
e	0.80
b	$0.50^{+0.05}_{-0.10}$
x	0.08
y	0.10
y1	0.20
ZD	1.20
ZE	1.20

P240F1-80-GA3

4. RECOMMENDED SOLDERING CONDITIONS

The μPD30181A and 30181AY should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to our document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 4-1. Soldering Conditions for Surface-Mount Type

(a) μPD30181AF1-131-GA3: 240-pin plastic FBGA (16 × 16)
μPD30181AYF1-131-GA3: 240-pin plastic FBGA (16 × 16)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds or less (210°C or higher), Count: two times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 20 hours)	IR35-203-2

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

(b) μPD30181AF1-131-GA3-A[Note]: 240-pin plastic FBGA (16 × 16)
μPD30181AYF1-131-GA3-A[Note]: 240-pin plastic FBGA (16 × 16)

For soldering methods and conditions, contact an NEC sales representative.

Note Lead-free product

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

Reference document Electrical Characteristics for Microcomputer (U15170J)[Note]

Note This document number is that of the Japanese version.

The documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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