

LH28F128SPHTD-PTLZ5

Flash Memory

128Mbit (8Mbitx16 / 16Mbitx8)

(Model Number: LHF12PZ5)

Spec. Issue Date: December 15, 2004
Spec No: EL16Y377

SPEC No. EL16Y377

ISSUE: Dec. 15, 2004

To; _____

S P E C I F I C A T I O N S

Product Type 128 Mbit Flash Memory

L H 2 8 F 1 2 8 S P H T D — P T L Z 5

Model No. (L H F 1 2 P Z 5)

If you have any objections, please contact us before issuing purchasing order.

* This specifications contains 40 pages including the cover and appendix.

* Refer to LH28F640SP series Appendix (FUM03201).

CUSTOMERS ACCEPTANCE

DATE: _____

BY: _____

PRESENTED

BY: M. Nawaki

M. NAWAKI

Dept. General Manager

REVIEWED BY:

PREPARED BY:

Y. Suminaga S. Kouchi

Product Development Dept. II

System-Flash Division

Integrated Circuits Group

SHARP CORPORATION

- Handle this document carefully for it contains material protected by international copyright law. Any reproduction, full or in part, of this material is prohibited without the express written permission of the company.
- When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.
 - (1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).
 - Office electronics
 - Instrumentation and measuring equipment
 - Machine tools
 - Audiovisual equipment
 - Home appliance
 - Communication equipment other than for trunk lines
 - (2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
 - Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
 - Mainframe computers
 - Traffic control systems
 - Gas leak detectors and automatic cutoff devices
 - Rescue and security equipment
 - Other safety devices and safety equipment, etc.
 - (3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
 - Aerospace equipment
 - Communications equipment for trunk lines
 - Control equipment for the nuclear power industry
 - Medical equipment related to life support, etc.
 - (4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.
- Please direct all queries regarding the products covered herein to a sales representative of the company.

CONTENTS

	PAGE		PAGE
56-Lead TSOP (Normal Bend) Pinout	3	1 Electrical Specifications	17
Pin Descriptions.....	4	1.1 Absolute Maximum Ratings.....	17
CE ₀ , CE ₁ , BS Truth Table	5	1.2 Operating Conditions	17
Memory Map	6	1.2.1 Capacitance.....	18
Identifier Codes Address	8	1.2.2 AC Input/Output Test Conditions.....	18
OTP Block Address Map.....	9	1.2.3 DC Characteristics.....	19
Bus Operation	10	1.2.4 AC Characteristics - Read-Only Operations	21
Command Definitions	11	1.2.5 AC Characteristics - Write Operations	25
Functions of Block Lock	13	1.2.6 Reset Operations.....	27
Status Register Definition.....	14	1.2.7 Block Erase, (Page Buffer) Program and Block Lock Configuration Performance.....	28
Extended Status Register Definition	15	2 Related Document Information	29
STS Configuration Definition	16	3 Package and packing specification.....	30

LH28F128SPHTD-PTLZ5 128Mbit (8Mbit×16/16Mbit×8) Page Mode Flash MEMORY

- 128-Mbit Density
 - Bit Organization ×8/×16
- High Performance Page Mode Reads for Memory Array
 - 120/25ns 4-Word/ 8-Byte Page Mode
- $V_{CC}=2.7V-3.6V$ Operation
 - V_{CCQ} for Input/Output Power Supply Isolation
 - Automatic Power Savings Mode reduces I_{CCR} in Static Mode
- OTP (One Time Program) Block
 - 4-Word/ 8-Byte Factory-Programmed Area
 - 3963-Word/ 7926-Byte User-Programmable Area
- High Performance Program with Page Buffer
 - 16-Word/ 32-Byte Page Buffer
 - Page Buffer Program Time 12.5μs/byte (Typ.)
- Operating Temperature -40°C to +85°C
- Symmetrically-Blocked Architecture
 - One-hundred and twenty-eight 64-KWord/ 128-KByte Blocks
- Enhanced Data Protection Features
 - Individual Block Lock
 - Absolute Protection with $V_{PEN} \leq V_{PENLK}$
 - Block Erase, (Page Buffer) Program Lockout during Power Transitions
- Automated Erase/Program Algorithms
 - Program Time 210μs (Typ.)
 - Block Erase Time 1s (Typ.)
- Cross-Compatible Command Support
 - Basic Command Set
 - Common Flash Interface (CFI)
- Extended Cycling Capability
 - Minimum 100,000 Block Erase Cycles
- 56-Lead TSOP (Normal Bend)
- CMOS Process (P-type silicon substrate)
- ETOXTM* Flash Technology
- Not designed or rated as radiation hardened

The product, which is Page Mode Flash memory, is a high density, low cost, nonvolatile read/write storage solution for a wide range of applications. The product can operate at $V_{CC}=2.7V-3.6V$ and $V_{PEN}=2.7V-3.6V$

The product supports high performance page mode. It allows code execution directly from Flash, thus eliminating time consuming wait states.

Fast program capability is provided through the use of high speed Page Buffer Program.

The block locking scheme is available for memory array and this scheme provides maximum flexibility for safe nonvolatile code and data storage.

OTP (One Time Program) block provides an area to store security code and to protect its code.

* ETOX is a trademark of Intel Corporation.

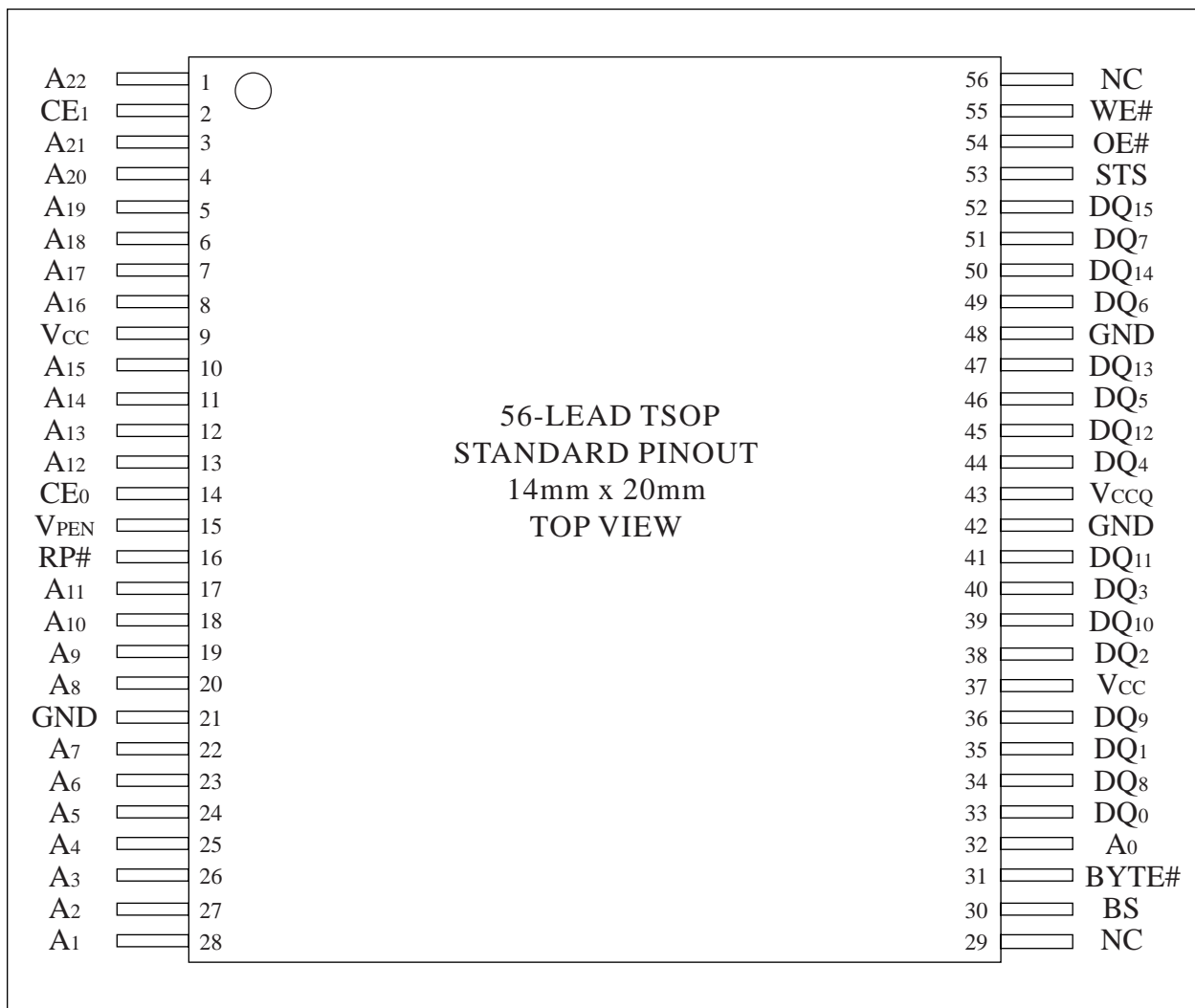


Figure 1. 56-Lead TSOP (Normal Bend) Pinout

Table 1. Pin Descriptions

Symbol	Type	Name and Function
A_0	INPUT	ADDRESS INPUTS: Lowest address input in byte mode ($BYTE\# = V_{IL} : \times 8$ bit). Address is internally latched during an erase or a program cycle. This pin is not used in word mode ($BYTE\# = V_{IH} : \times 16$ bit).
$A_{22}-A_1$	INPUT	ADDRESS INPUTS: Inputs for addresses during read, erase and program operations. Addresses are internally latched during an erase or a program cycle.
BS	INPUT	BANK SELECT: Bank 0 is selected by $BS = V_{IL}$. Bank 1 is selected by $BS = V_{IH}$.
$DQ_{15}-DQ_0$	INPUT/ OUTPUT	DATA INPUTS/OUTPUTS: Inputs data and commands during CUI (Command User Interface) write cycles, outputs data during memory array, status register, query code, identifier code reads. Data pins float to high-impedance (High Z) when the chip or outputs are deselected. Data is internally latched during an erase or program cycle. $DQ_{15}-DQ_8$ pins are not used in byte mode ($BYTE\# = V_{IL} : \times 8$ bit).
CE_0, CE_1	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. When the device is de-selected, power consumption reduces to standby levels. Refer to Table 2 to determine whether the device is selected or de-selected depending on the state of CE_0, CE_1 and BS.
RP#	INPUT	RESET: When low (V_{IL}), RP# resets internal automation and inhibits erase and program operations, which provides data protection. RP#-high (V_{IH}) enables normal operation. After power-up or reset mode, the device is automatically set to read array mode. RP# must be low during power-up/down.
OE#	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
WE#	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the first edge of CE_0 or CE_1 that disables the device or the rising edge of WE# (whichever occurs first). BS transitions must not occur when $CE_0 = CE_1 = V_{IL}$ and $WE\# = V_{IL}$.
STS	OPEN DRAIN OUTPUT	STATUS: Indicates the status of the internal WSM (Write State Machine). When configured in level mode (default mode), STS acts as a RY/BY# pin (STS is V_{OL} when the WSM is executing internal erase or program algorithms). When configured in one of its pulse modes, STS can pulse to indicate erase/program completion. Refer to Table 9 for STS configuration.
BYTE#	INPUT	BYTE ENABLE: $BYTE\# V_{IL}$ places the device in byte mode ($\times 8$). In this mode, $DQ_{15}-DQ_8$ is floated (High Z) and A_0 is the lowest address input. $BYTE\# V_{IH}$ places the device in word mode ($\times 16$) and A_1 is the lowest address input.
V_{PEN}	INPUT	MONITORING POWER SUPPLY VOLTAGE: V_{PEN} is not used for power supply pin. With $V_{PEN} \leq V_{PENLK}$, block erase, (page buffer) program, block lock configuration and OTP program cannot be executed and should not be attempted.
V_{CC}	SUPPLY	DEVICE POWER SUPPLY (2.7V-3.6V): With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (refer to DC Characteristics) produce spurious results and should not be attempted.
V_{CCQ}	SUPPLY	INPUT/OUTPUT POWER SUPPLY (2.7V-3.6V): Power supply for all input/output pins.
GND	SUPPLY	GROUND: Do not float any ground pins.
NC		NO CONNECT: Lead is not internally connected; it may be driven or floated.

Table 2. CE₀, CE₁, BS Truth Table ^{(1), (2)}

BS	CE ₁	CE ₀	Device
V _{IL}	V _{IL}	V _{IL}	Bank 0 Enabled
	V _{IL}	V _{IH}	Disabled
	V _{IH}	V _{IL}	Disabled
	V _{IH}	V _{IH}	Disabled
V _{IH}	V _{IL}	V _{IL}	Bank 1 Enabled
	V _{IL}	V _{IH}	Disabled
	V _{IH}	V _{IL}	Disabled
	V _{IH}	V _{IH}	Disabled

- NOTE:
- 1. For single-chip applications, CE₁ can be connected to GND.
 - 2. BS transitions must not occur when CE₀=CE₁=V_{IL} and WE#=V_{IL}.

Selected by BS=V_{IL} (Bank 0)

[A ₂₂ -A ₁]		[A ₂₂ -A ₀]		[A ₂₂ -A ₁]		[A ₂₂ -A ₀]
3FFFFF	64-Kword/128-Kbyte Block 63	7FFFFF		1FFFFF	64-Kword/128-Kbyte Block 31	3FFFFF
3F0000		7E0000		1F0000		3E0000
3EFFFF	64-Kword/128-Kbyte Block 62	7DFFFF		1EFFFF	64-Kword/128-Kbyte Block 30	3DFFFF
3E0000		7C0000		1E0000		3C0000
3DFFFF	64-Kword/128-Kbyte Block 61	7BFFFF		1DFFFF	64-Kword/128-Kbyte Block 29	3BFFFF
3D0000		7A0000		1D0000		3A0000
3CFFFF	64-Kword/128-Kbyte Block 60	79FFFF		1CFFFF	64-Kword/128-Kbyte Block 28	39FFFF
3C0000		780000		1C0000		380000
3BFFFF	64-Kword/128-Kbyte Block 59	77FFFF		1BFFFF	64-Kword/128-Kbyte Block 27	37FFFF
3B0000		760000		1B0000		360000
3AFFFF	64-Kword/128-Kbyte Block 58	75FFFF		1AFFFF	64-Kword/128-Kbyte Block 26	35FFFF
3A0000		740000		1A0000		340000
39FFFF	64-Kword/128-Kbyte Block 57	73FFFF		19FFFF	64-Kword/128-Kbyte Block 25	33FFFF
390000		720000		190000		320000
38FFFF	64-Kword/128-Kbyte Block 56	71FFFF		18FFFF	64-Kword/128-Kbyte Block 24	31FFFF
380000		700000		180000		300000
37FFFF	64-Kword/128-Kbyte Block 55	6FFFFF		17FFFF	64-Kword/128-Kbyte Block 23	2FFFFF
370000		6E0000		170000		2E0000
36FFFF	64-Kword/128-Kbyte Block 54	6DFFFF		16FFFF	64-Kword/128-Kbyte Block 22	2DFFFF
360000		6C0000		160000		2C0000
35FFFF	64-Kword/128-Kbyte Block 53	6BFFFF		15FFFF	64-Kword/128-Kbyte Block 21	2BFFFF
350000		6A0000		150000		2A0000
34FFFF	64-Kword/128-Kbyte Block 52	69FFFF		14FFFF	64-Kword/128-Kbyte Block 20	29FFFF
340000		680000		140000		280000
33FFFF	64-Kword/128-Kbyte Block 51	67FFFF		13FFFF	64-Kword/128-Kbyte Block 19	27FFFF
330000		660000		130000		260000
32FFFF	64-Kword/128-Kbyte Block 50	65FFFF		12FFFF	64-Kword/128-Kbyte Block 18	25FFFF
320000		640000		120000		240000
31FFFF	64-Kword/128-Kbyte Block 49	63FFFF		11FFFF	64-Kword/128-Kbyte Block 17	23FFFF
310000		620000		110000		220000
30FFFF	64-Kword/128-Kbyte Block 48	61FFFF		10FFFF	64-Kword/128-Kbyte Block 16	21FFFF
300000		600000		100000		200000
2FFFFF	64-Kword/128-Kbyte Block 47	5FFFFF		0FFFFF	64-Kword/128-Kbyte Block 15	1FFFFF
2F0000		5E0000		0F0000		1E0000
2EFFFF	64-Kword/128-Kbyte Block 46	5DFFFF		0EFFFF	64-Kword/128-Kbyte Block 14	1DFFFF
2E0000		5C0000		0E0000		1C0000
2DFFFF	64-Kword/128-Kbyte Block 45	5BFFFF		0DFFFF	64-Kword/128-Kbyte Block 13	1BFFFF
2D0000		5A0000		0D0000		1A0000
2CFFFF	64-Kword/128-Kbyte Block 44	59FFFF		0CFFFF	64-Kword/128-Kbyte Block 12	19FFFF
2C0000		580000		0C0000		180000
2BFFFF	64-Kword/128-Kbyte Block 43	57FFFF		0BFFFF	64-Kword/128-Kbyte Block 11	17FFFF
2B0000		560000		0B0000		160000
2AFFFF	64-Kword/128-Kbyte Block 42	55FFFF		0AFFFF	64-Kword/128-Kbyte Block 10	15FFFF
2A0000		540000		0A0000		140000
29FFFF	64-Kword/128-Kbyte Block 41	53FFFF		09FFFF	64-Kword/128-Kbyte Block 9	13FFFF
290000		520000		090000		120000
28FFFF	64-Kword/128-Kbyte Block 40	51FFFF		08FFFF	64-Kword/128-Kbyte Block 8	11FFFF
280000		500000		080000		100000
27FFFF	64-Kword/128-Kbyte Block 39	4FFFFF		07FFFF	64-Kword/128-Kbyte Block 7	0FFFFF
270000		4E0000		070000		0E0000
26FFFF	64-Kword/128-Kbyte Block 38	4DFFFF		06FFFF	64-Kword/128-Kbyte Block 6	0DFFFF
260000		4C0000		060000		0C0000
25FFFF	64-Kword/128-Kbyte Block 37	4BFFFF		05FFFF	64-Kword/128-Kbyte Block 5	0BFFFF
250000		4A0000		050000		0A0000
24FFFF	64-Kword/128-Kbyte Block 36	49FFFF		04FFFF	64-Kword/128-Kbyte Block 4	09FFFF
240000		480000		040000		080000
23FFFF	64-Kword/128-Kbyte Block 35	47FFFF		03FFFF	64-Kword/128-Kbyte Block 3	07FFFF
230000		460000		030000		060000
22FFFF	64-Kword/128-Kbyte Block 34	45FFFF		02FFFF	64-Kword/128-Kbyte Block 2	05FFFF
220000		440000		020000		040000
21FFFF	64-Kword/128-Kbyte Block 33	43FFFF		01FFFF	64-Kword/128-Kbyte Block 1	03FFFF
210000		420000		010000		020000
20FFFF	64-Kword/128-Kbyte Block 32	41FFFF		00FFFF	64-Kword/128-Kbyte Block 0	01FFFF
200000		400000		000000		000000

Figure 2.1. Memory Map (Memory Area selected by BS=V_{IL})

Selected by BS=V_{IH} (Bank 1)

[A ₂₂ -A ₁]		[A ₂₂ -A ₀]		[A ₂₂ -A ₁]		[A ₂₂ -A ₀]
3FFFFF	64-Kword/128-Kbyte Block 63	7FFFFF		1FFFFF	64-Kword/128-Kbyte Block 31	3FFFFF
3F0000		7E0000		1F0000		3E0000
3EFFFF	64-Kword/128-Kbyte Block 62	7DFFFF		1EFFFF	64-Kword/128-Kbyte Block 30	3DFFFF
3E0000		7C0000		1E0000		3C0000
3DFFFF	64-Kword/128-Kbyte Block 61	7BFFFF		1DFFFF	64-Kword/128-Kbyte Block 29	3BFFFF
3D0000		7A0000		1D0000		3A0000
3CFFFF	64-Kword/128-Kbyte Block 60	79FFFF		1CFFFF	64-Kword/128-Kbyte Block 28	39FFFF
3C0000		780000		1C0000		380000
3BFFFF	64-Kword/128-Kbyte Block 59	77FFFF		1BFFFF	64-Kword/128-Kbyte Block 27	37FFFF
3B0000		760000		1B0000		360000
3AFFFF	64-Kword/128-Kbyte Block 58	75FFFF		1AFFFF	64-Kword/128-Kbyte Block 26	35FFFF
3A0000		740000		1A0000		340000
39FFFF	64-Kword/128-Kbyte Block 57	73FFFF		19FFFF	64-Kword/128-Kbyte Block 25	33FFFF
390000		720000		190000		320000
38FFFF	64-Kword/128-Kbyte Block 56	71FFFF		18FFFF	64-Kword/128-Kbyte Block 24	31FFFF
380000		700000		180000		300000
37FFFF	64-Kword/128-Kbyte Block 55	6FFFFF		17FFFF	64-Kword/128-Kbyte Block 23	2FFFFF
370000		6E0000		170000		2E0000
36FFFF	64-Kword/128-Kbyte Block 54	6DFFFF		16FFFF	64-Kword/128-Kbyte Block 22	2DFFFF
360000		6C0000		160000		2C0000
35FFFF	64-Kword/128-Kbyte Block 53	6BFFFF		15FFFF	64-Kword/128-Kbyte Block 21	2BFFFF
350000		6A0000		150000		2A0000
34FFFF	64-Kword/128-Kbyte Block 52	69FFFF		14FFFF	64-Kword/128-Kbyte Block 20	29FFFF
340000		680000		140000		280000
33FFFF	64-Kword/128-Kbyte Block 51	67FFFF		13FFFF	64-Kword/128-Kbyte Block 19	27FFFF
330000		660000		130000		260000
32FFFF	64-Kword/128-Kbyte Block 50	65FFFF		12FFFF	64-Kword/128-Kbyte Block 18	25FFFF
320000		640000		120000		240000
31FFFF	64-Kword/128-Kbyte Block 49	63FFFF		11FFFF	64-Kword/128-Kbyte Block 17	23FFFF
310000		620000		110000		220000
30FFFF	64-Kword/128-Kbyte Block 48	61FFFF		10FFFF	64-Kword/128-Kbyte Block 16	21FFFF
300000		600000		100000		200000
2FFFFF	64-Kword/128-Kbyte Block 47	5FFFFF		0FFFFF	64-Kword/128-Kbyte Block 15	1FFFFF
2F0000		5E0000		0F0000		1E0000
2EFFFF	64-Kword/128-Kbyte Block 46	5DFFFF		0EFFFF	64-Kword/128-Kbyte Block 14	1DFFFF
2E0000		5C0000		0E0000		1C0000
2DFFFF	64-Kword/128-Kbyte Block 45	5BFFFF		0DFFFF	64-Kword/128-Kbyte Block 13	1BFFFF
2D0000		5A0000		0D0000		1A0000
2CFFFF	64-Kword/128-Kbyte Block 44	59FFFF		0CFFFF	64-Kword/128-Kbyte Block 12	19FFFF
2C0000		580000		0C0000		180000
2BFFFF	64-Kword/128-Kbyte Block 43	57FFFF		0BFFFF	64-Kword/128-Kbyte Block 11	17FFFF
2B0000		560000		0B0000		160000
2AFFFF	64-Kword/128-Kbyte Block 42	55FFFF		0AFFFF	64-Kword/128-Kbyte Block 10	15FFFF
2A0000		540000		0A0000		140000
29FFFF	64-Kword/128-Kbyte Block 41	53FFFF		09FFFF	64-Kword/128-Kbyte Block 9	13FFFF
290000		520000		090000		120000
28FFFF	64-Kword/128-Kbyte Block 40	51FFFF		08FFFF	64-Kword/128-Kbyte Block 8	11FFFF
280000		500000		080000		100000
27FFFF	64-Kword/128-Kbyte Block 39	4FFFFF		07FFFF	64-Kword/128-Kbyte Block 7	0FFFFF
270000		4E0000		070000		0E0000
26FFFF	64-Kword/128-Kbyte Block 38	4DFFFF		06FFFF	64-Kword/128-Kbyte Block 6	0DFFFF
260000		4C0000		060000		0C0000
25FFFF	64-Kword/128-Kbyte Block 37	4BFFFF		05FFFF	64-Kword/128-Kbyte Block 5	0BFFFF
250000		4A0000		050000		0A0000
24FFFF	64-Kword/128-Kbyte Block 36	49FFFF		04FFFF	64-Kword/128-Kbyte Block 4	09FFFF
240000		480000		040000		080000
23FFFF	64-Kword/128-Kbyte Block 35	47FFFF		03FFFF	64-Kword/128-Kbyte Block 3	07FFFF
230000		460000		030000		060000
22FFFF	64-Kword/128-Kbyte Block 34	45FFFF		02FFFF	64-Kword/128-Kbyte Block 2	05FFFF
220000		440000		020000		040000
21FFFF	64-Kword/128-Kbyte Block 33	43FFFF		01FFFF	64-Kword/128-Kbyte Block 1	03FFFF
210000		420000		010000		020000
20FFFF	64-Kword/128-Kbyte Block 32	41FFFF		00FFFF	64-Kword/128-Kbyte Block 0	01FFFF
200000		400000		000000		000000

Figure 2.2. Memory Map (Memory Area selected by BS=V_{IH})

Table 3. Identifier Codes Address

	Code	Address [A ₂₂ -A ₁] ⁽¹⁾	Data [DQ ₇ -DQ ₀]	Notes
Manufacturer Code	Manufacturer Code	000000H	B0H	2
Device Code	Device Code	000001H	18H	2
Block Lock Configuration Code	Block is Unlocked	Block Address + 2	DQ ₀ = 0	3
	Block is Locked		DQ ₀ = 1	3

NOTES:

1. The address A₀ and BS don't care.
2. "00H" is presented on DQ₁₅-DQ₈ in word mode (BYTE#=V_{IH} : ×16 bit).
3. Block Address = The beginning location of a block address. DQ₁₅-DQ₁ are reserved for future implementation.

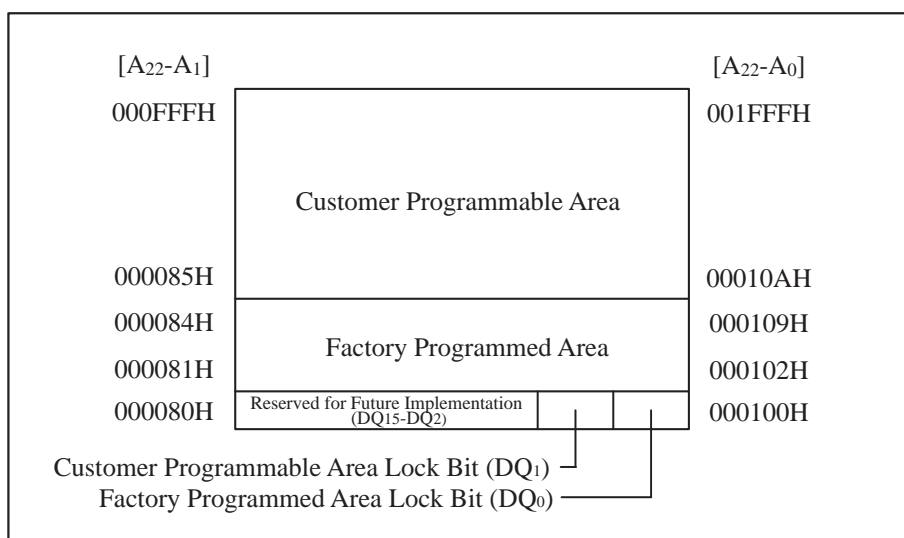


Figure 3. OTP Block Address Map
(The area not specified in the above figure cannot be used.)

NOTE:

1. BS must be V_{IL} , when using OTP block.

Table 4. Bus Operation^(1, 2)

Mode	Notes	RP#	CE _{0,1} ⁽³⁾	OE#	WE#	Address	V _{PEN}	DQ ⁽⁴⁾	STS ⁽¹⁰⁾
Read Array	8	V _{IH}	Enabled	V _{IL}	V _{IH}	X	X	D _{OUT}	X
Output Disable		V _{IH}	Enabled	V _{IH}	V _{IH}	X	X	High Z	X
Standby		V _{IH}	Disabled	X	X	X	X	High Z	X
Reset	5	V _{IL}	X	X	X	X	X	High Z	High Z
Read Identifier Codes/OTP	8	V _{IH}	Enabled	V _{IL}	V _{IH}	Refer to Table 3	X	Refer to Table 3	X
Read Query	8,9	V _{IH}	Enabled	V _{IL}	V _{IH}	See Appendix	X	See Appendix	X
Write	6,7,8	V _{IH}	Enabled	V _{IH}	V _{IL}	X	X	D _{IN}	X

NOTES:

1. Refer to DC Characteristics. When $V_{PEN} \leq V_{PENLK}$, memory contents can be read, but cannot be altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PENLK} or V_{PENH} for V_{PEN}.
Refer to DC Characteristics for V_{PENLK} and V_{PENH} voltages.
3. Refer to Table 2 to determine whether the device is selected or de-selected depending on the state of CE₀, CE₁ and BS.
4. DQ refers to DQ₁₅-DQ₀ in word mode (BYTE#=V_{IH} : ×16 bit) and DQ₇-DQ₀ in byte mode (BYTE#=V_{IL} : ×8 bit).
5. RP# at GND±0.2V ensures the lowest power consumption.
6. Command writes involving block erase, (page buffer) program, block lock configuration or OTP program are reliably executed when V_{PEN}=V_{PENH} and V_{CC}=2.7V-3.6V.
7. Refer to Table 5 for valid D_{IN} during a write operation. BS transitions must not occur when CE₀=CE₁=V_{IL} and WE#=V_{IL}.
8. Never hold OE# low and WE# low at the same timing.
9. Refer to Appendix of LH28F640SP series for more information about query code.
10. STS is V_{OL} when the WSM (Write State Machine) is executing internal block erase, (page buffer) program or OTP program algorithms. It is High Z during when the WSM is not busy, in block erase suspend mode (with program and page buffer program inactive), (page buffer) program suspend mode, or reset mode.

Table 5. Command Definitions ⁽¹⁰⁾

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Oper ⁽¹⁾	Addr ⁽²⁾	Data ⁽³⁾	Oper ⁽¹⁾	Addr ⁽²⁾	Data ⁽³⁾
Read Array	1		Write	Bnk	FFH			
Read Identifier Codes/OTP	≥ 2	4	Write	Bnk	90H	Read	IA or OA	ID or OD
Read Query	≥ 2	4	Write	Bnk	98H	Read	QA	QD
Read Status Register	2		Write	Bnk	70H	Read	Bnk	SRD
Clear Status Register	1		Write	Bnk	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Program	2	5,6	Write	WA	40H or 10H	Write	WA	WD
Page Buffer Program	≥ 4	5,7	Write	BA	E8H	Write	BA	N-1
Block Erase and (Page Buffer) Program Suspend	1	8	Write	Bnk	B0H			
Block Erase and (Page Buffer) Program Resume	1	8	Write	Bnk	D0H			
STS Configuration	2		Write	Bnk	B8H	Write	Bnk	CC
Set Block Lock Bit	2		Write	BA	60H	Write	BA	01H
Clear Block Lock Bits	2	9	Write	Bnk	60H	Write	Bnk	D0H
OTP Program	2		Write	OA	C0H	Write	OA	OD

NOTES:

- Bus operations are defined in Table 4. Each command is valid for the bank to which the command is written. BS transitions must not occur when $CE_0=CE_1=V_{IL}$ and $WE\#=V_{IL}$.
- Bnk=Any valid address within the bank selected by BS.
IA=Identifier codes address (Refer to Table 3).
QA=Query codes address. Refer to Appendix of LH28F640SP series for details.
BA=Address within the block for block erase, page buffer program or set block lock bit.
WA=Address of memory location for the Program command.
OA=Address of OTP block to be read or programmed (Refer to Figure 3).
- The upper byte of the data bus (DQ₁₅-DQ₈) during command writes is ignored in word mode (BYTE#=V_{IH}: ×16 bit).
ID=Data to be read from identifier codes. (Refer to Table 3).
QD=Data to be read from query database. Refer to Appendix of LH28F640SP series for details.
SRD=Data to be read from status register. Refer to Table 7 for a description of the status register bits.
WD=Data to be programmed at location WA. Data is latched on the first edge of CE₀ or CE₁ that disables the device or the rising edge of WE# (whichever occurs first) during command write cycles.
N-1=N is the number of the words /bytes to be loaded into a page buffer.
OD=Data within OTP block. Data is latched on the first edge of CE₀ or CE₁ that disables the device or the rising edge of WE# (whichever occurs first) during command write cycles.
CC= STS configuration code (Refer to Table 9). STS configuration must be set for every bank.
- Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock configuration code and the data within OTP block (Refer to Table 3).
The Read Query command is available for reading CFI (Common Flash Interface) information.
- Block erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when RP# is V_{IH}.
- Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.
- Following the third bus cycle, write the program sequential address and data of "N" times. Finally, write the any valid address within the block to be programmed and the confirm command (D0H).
Refer to Appendix of LH28F640SP series for details.

8. If both block erase operation and (page buffer) program operation are suspended, the suspended (page buffer) program operation is resumed when writing the Block Erase and (Page Buffer) Program Resume (D0H) command.
9. Following the Clear Block Lock Bits command, all the blocks within the bank to which the command is written are unlocked at a time.
10. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

Table 6. Functions of Block Lock ^{(1), (2)}

DQ ₀ ⁽³⁾	State Name	Erase/Program Allowed ⁽⁴⁾
0	Unlocked	Yes
1	Locked	No

NOTES:

1. Selected block is locked by the Set Block Lock Bit command. Following the Clear Block Lock Bits command, all the blocks within the bank to which the command is written are unlocked at a time.
2. Locked and unlocked states remain unchanged even after power-up/down and device reset.
3. After writing the Read Identifier Codes/OTP command, read operation outputs the block lock bit status on DQ₀ (refer to Table 3).
4. Erase and program are general terms, respectively, to express: block erase and (page buffer) program operations.

Table 7. Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
WSMS	BESS	BECBLS	PBPOPSBLS	VPENS	PBPSS	DPS	R
7	6	5	4	3	2	1	0
<p>SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p> <p>SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy</p> <p>SR.6 = BLOCK ERASE SUSPEND STATUS (BESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed</p> <p>SR.5 = BLOCK ERASE AND CLEAR BLOCK LOCK BITS STATUS (BECBLS) 1 = Error in Block Erase or Clear Block Lock Bits 0 = Successful Block Erase or Clear Block Lock Bits</p> <p>SR.4 = (PAGE BUFFER) PROGRAM, OTP PROGRAM AND SET BLOCK LOCK BIT STATUS (PBPOPSBLS) 1 = Error in (Page Buffer) Program, OTP Program or Set Block Lock Bit 0 = Successful (Page Buffer) Program, OTP Program or Set Block Lock Bit</p> <p>SR.3 = V_{PEN} STATUS (VPENS) 1 = V_{PEN} LOW Detect, Operation Abort 0 = V_{PEN} OK</p> <p>SR.2 = (PAGE BUFFER) PROGRAM SUSPEND STATUS (PBPSS) 1 = (Page Buffer) Program Suspended 0 = (Page Buffer) Program in Progress/Completed</p> <p>SR.1 = DEVICE PROTECT STATUS (DPS) 1 = Erase or Program Attempted on a Locked Block, Operation Abort 0 = Unlocked</p> <p>SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p>				<p>NOTES:</p> <p>Check SR.7 or STS to determine block erase, (page buffer) program, block lock configuration or OTP program completion. SR.6 - SR.1 are invalid while SR.7="0".</p> <p>If both SR.5 and SR.4 are "1"s after a block erase, page buffer program, block lock configuration, STS configuration attempt, an improper command sequence was entered.</p> <p>SR.3 does not provide a continuous indication of V_{PEN} level. The WSM interrogates and indicates the V_{PEN} level only after Block Erase, (Page Buffer) Program, Set Block Lock Bit, Clear Block Lock Bits or OTP Program command sequences. SR.3 is not guaranteed to report accurate feedback when $V_{PEN} \neq V_{PENH}$ or V_{PENLK}.</p> <p>SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, (Page Buffer) Program or OTP Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/OTP command indicates block lock bit status.</p> <p>SR.15 - SR.8 and SR.0 are reserved for future use and should be masked out when polling the status register.</p>			

Table 8. Extended Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R) XSR.7 = STATE MACHINE STATUS (SMS) 1 = Page Buffer Program available 0 = Page Buffer Program not available XSR.6-0 =RESERVED FOR FUTURE ENHANCEMENTS (R)				NOTES: After issue a Page Buffer Program command (E8H), XSR.7="1" indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not. XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register.			

Table 9. STS Configuration Definition ^{(1), (2)}

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
R	R	R	R	R	R	CC	CC
7	6	5	4	3	2	1	0

DQ₁₅-DQ₂ = RESERVED FOR FUTURE
ENHANCEMENTS (R)

DQ₁-DQ₀ = STS CONFIGURATION CODE (CC)
00 = level mode: RY/BY# indication. (Default)
01 = pulse mode on erase complete.
10 = pulse mode on program complete.
11 = pulse mode on erase or program complete.

In STS configuration = "00", STS is V_{OL} when the WSM is executing internal erase or program algorithms.

STS configuration codes "01", "10" and "11" are all pulse modes such that the STS pin pulses low then high when the operation indicated by the configuration code is completed.

NOTES:

After power-up or device reset, STS configuration is set to "00".

STS configuration 00

The output of the STS pin is the control signal to prevent accessing a flash memory while the internal WSM is busy (SR.7="0").

STS configuration 01

The output of the STS pin is the control signal to indicate that the erase operation is completed and the flash memory is available for the next operation.

STS configuration 10

The output of the STS pin is the control signal to indicate that the program operation is completed and the flash memory is available for the next operation.

STS configuration 11

The output of the STS pin is the control signal to indicate that the erase or program operation is completed and the flash memory is available for the next operation.

NOTE:

1. When the device is configured in one of the pulse modes, the STS pin pulses low with a typical pulse width of 250ns.
2. STS configuration must be set for every bank.

1 Electrical Specifications

1.1 Absolute Maximum Ratings *

Operating Temperature

During Read, Erase and Program ... -40°C to +85°C ⁽¹⁾

Storage Temperature

During under Bias..... -40°C to +85°C

During non Bias..... -65°C to +125°C

Voltage On Any Pin (except V_{CC}, V_{CCQ} and V_{PEN})

..... -0.5V to V_{CCQ}+0.5V ⁽²⁾

V_{CC} and V_{CCQ} Supply Voltage -0.2V to +3.9V ⁽²⁾

V_{PEN} Supply Voltage..... -0.2V to +3.9V ⁽²⁾

Output Short Circuit Current 100mA ⁽³⁾

***WARNING:** Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTES:

1. Operating temperature is for extended temperature product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC}, V_{CCQ} and V_{PEN} pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is V_{CC}+0.5V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

1.2 Operating Conditions

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
T _A	Operating Temperature		-40	+25	+85	°C	Ambient Temperature
V _{CC}	V _{CC} Supply Voltage	1, 2	2.7	3.0	3.6	V	
V _{CCQ}	I/O Supply Voltage	1, 2	2.7	3.0	3.6	V	
V _{PENH}	V _{PEN} Voltage	1	2.7	3.0	3.6	V	
	Block Erase Cycling: V _{PEN} =V _{PENH}		100,000			Cycles	

NOTES:

1. Refer to DC Characteristics tables for voltage range-specific specification.
2. V_{CC} and V_{CCQ} should be the same voltage.

1.2.1 Capacitance ⁽¹⁾ (T_A=+25°C, f=1MHz)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
C _{IN}	Input Capacitance		12	16	pF	V _{IN} =0.0V
C _{OUT}	Output Capacitance		16	24	pF	V _{OUT} =0.0V

NOTE:
1. Sampled, not 100% tested.

1.2.2 AC Input/Output Test Conditions

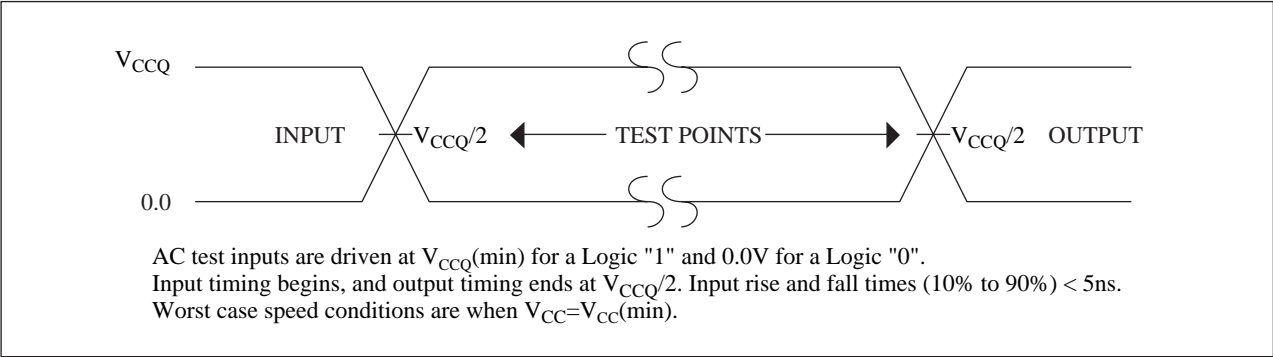


Figure 4. Transient Input/Output Reference Waveform for V_{CC}=2.7V-3.6V

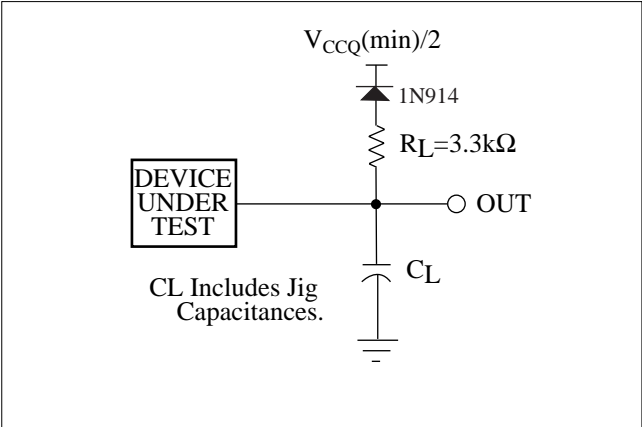


Figure 5. Transient Equivalent Testing Load Circuit

Table 10. Configuration Capacitance Loading Value

Test Configuration	C _L (pF)
V _{CC} =2.7V-3.6V	30

1.2.3 DC Characteristics

 $V_{CC}=2.7V-3.6V$

Symbol	Parameter		Notes	Min.	Typ.	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	-2		+2	μA	$V_{CC}=V_{CCMax.}$, $V_{CCQ}=V_{CCQMax.}$, $V_{IN}/V_{OUT}=V_{CCQ}$ or GND
I_{LO}	Output Leakage Current		1	-10		+10	μA	
I_{CCS}	V_{CC} Standby Current		1, 2, 8		50	120	μA	CMOS Inputs, $V_{CC}=V_{CCMax.}$, $V_{CCQ}=V_{CCQMax.}$, Device is disabled (refer to Table 2), $RP\#=V_{CCQ}\pm 0.2V$
					0.71	2	mA	TTL Inputs, $V_{CC}=V_{CCMax.}$, $V_{CCQ}=V_{CCQMax.}$, Device is disabled (refer to Table 2), $RP\#=V_{IH}$
I_{CCAS}	V_{CC} Automatic Power Savings Current		1, 2, 5		50	120	μA	CMOS Inputs, $V_{CC}=V_{CCMax.}$, $V_{CCQ}=V_{CCQMax.}$, Device is enabled (refer to Table 2)
I_{CCD}	V_{CC} Reset Current		1		50	120	μA	$RP\#=GND\pm 0.2V$ $I_{OUT}(STS)=0mA$
I_{CCR}	Average V_{CC} Page Mode Read Current	4 word/ 8 byte read	1, 2		15	20	mA	CMOS Inputs, $V_{CC}=V_{CCMax.}$, $V_{CCQ}=V_{CCQMax.}$, Device is enabled (refer to Table 2), $f=5MHz$, $I_{OUT}=0mA$
			1, 2		24	29	mA	CMOS Inputs, $V_{CC}=V_{CCMax.}$, $V_{CCQ}=V_{CCQMax.}$, Device is enabled (refer to Table 2), $f=33MHz$, $I_{OUT}=0mA$
	Average V_{CC} Read Current	1 word/ 1 byte read	1, 2		40	50	mA	CMOS Inputs, $V_{CC}=V_{CCMax.}$, $V_{CCQ}=V_{CCQMax.}$, Device is enabled (refer to Table 2), $f=5MHz$, $I_{OUT}=0mA$
I_{CCW}	V_{CC} (Page Buffer) Program, Set Block Lock Bit Current		1, 2, 6		35	60	mA	CMOS Inputs, $V_{PEN}=V_{PENH}$
			1, 2, 6		40	70	mA	TTL Inputs, $V_{PEN}=V_{PENH}$

DC Characteristics (Continued)

$V_{CC}=2.7V-3.6V$

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
I_{CCE}	V_{CC} Block Erase, Clear Block Lock Bits Current	1, 2, 6		35	70	mA	CMOS Inputs, $V_{PEN}=V_{PENH}$
		1, 2, 6		40	80	mA	TTL Inputs, $V_{PEN}=V_{PENH}$
I_{CCWS} I_{CCES}	V_{CC} (Page Buffer) Program or Block Erase Suspend Current	1, 3			10	mA	Device is disabled (refer to Table 2).
V_{IL}	Input Low Voltage	6	-0.5		0.8	V	
V_{IH}	Input High Voltage	6	2.0		$V_{CCQ} + 0.5$	V	
V_{OL}	Output Low Voltage	6, 8			0.4	V	$V_{CC}=V_{CCMin.}$, $V_{CCQ}=V_{CCQMin.}$, $I_{OL}=2mA$
					0.2	V	$V_{CC}=V_{CCMin.}$, $V_{CCQ}=V_{CCQMin.}$, $I_{OL}=100\mu A$
V_{OH}	Output High Voltage	6, 8	$0.85 \times V_{CCQ}$			V	$V_{CC}=V_{CCMin.}$, $V_{CCQ}=V_{CCQMin.}$, $I_{OH}=-1.5mA$
			$V_{CCQ} - 0.2$			V	$V_{CC}=V_{CCMin.}$, $V_{CCQ}=V_{CCQMin.}$, $I_{OH}=-100\mu A$
V_{PENLK}	V_{PEN} Lockout Voltage during Normal Operations	4, 6, 7			1.0	V	
V_{PENH}	V_{PEN} Voltage during Block Erase, (Page Buffer) Program, Set Block Lock Bit, Clear Block Lock Bits or OTP Program Operations	4, 7	2.7	3.0	3.6	V	
V_{LKO}	V_{CC} Lockout Voltage	4	2.0			V	

NOTES:

- All currents are in RMS unless otherwise noted. Typical values are the reference values at $V_{CC}=3.0V$, $V_{CCQ}=3.0V$ and $T_A=+25^\circ C$ unless V_{CC} is specified.
- CMOS inputs are either $V_{CCQ} \pm 0.2V$ or $GND \pm 0.2V$. TTL inputs are either V_{IL} or V_{IH} .
- I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or (page buffer) program is executed while in block erase suspend mode, the device's current draw is the sum of I_{CCES} and I_{CCR} or I_{CCW} . If read is executed while in (page buffer) program suspend mode, the device's current draw is the sum of I_{CCWS} and I_{CCR} .
- Block erase, (page buffer) program, block lock configuration and OTP program operations are inhibited when $V_{PEN} \leq V_{PENLK}$ or $V_{CC} \leq V_{LKO}$. These operations are not guaranteed outside the specified voltage ($V_{CC}=2.7V-3.6V$ and $V_{PEN}=2.7V-3.6V$).
- The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings (t_{AVQV}) provide new data when addresses are changed.
- Sampled, not 100% tested.
- V_{PEN} is not used for power supply pin. With $V_{PEN} \leq V_{PENLK}$, block erase, (page buffer) program, block lock configuration and OTP program operations are inhibited.
- Includes STS.

1.2.4 AC Characteristics - Read-Only Operations ⁽¹⁾

 $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$

Symbol	Parameter	Notes	V_{CC}		V_{CCQ}		Unit
			3.0V-3.6V	2.7V-3.6V	3.0V-3.6V	2.7V-3.6V	
t_{AVAV}	Read Cycle Time		120		120		ns
t_{AVQV}	Address to Output Delay			120		120	ns
t_{ELQV}	CE_X to Output Delay	3, 4		120		120	ns
t_{APA}	Page Address Access Time			25		30	ns
t_{GLQV}	$OE\#$ to Output Delay	3		25		30	ns
t_{PHQV}	$RP\#$ High to Output Delay			180		180	ns
t_{ELQX}	CE_X to Output in Low Z	2, 4	0		0		ns
t_{GLQX}	$OE\#$ to Output in Low Z	2	0		0		ns
t_{EHQZ}	CE_X to Output in High Z	2, 5		35		35	ns
t_{GHQZ}	$OE\#$ to Output in High Z	2		15		15	ns
t_{OH}	Output Hold from First Occurring Address, CE_X or $OE\#$ change	2, 5	0		0		ns
t_{ELFL}/t_{ELFH}	CE_X Setup to $BYTE\#$ Going Low or High	2, 4		10		10	ns
t_{FLQV}/t_{FHQV}	$BYTE\#$ to Output Delay			1000		1000	ns
t_{FLQZ}/t_{FHQZ}	$BYTE\#$ to Output in High Z	2		1000		1000	ns

NOTES:

1. Refer to AC input/output reference waveform for timing measurements and maximum allowable input slew rate.
2. Sampled, not 100% tested.
3. $OE\#$ may be delayed up to $t_{ELQV} - t_{GLQV}$ after the first edge of CE_0 , CE_1 or BS that enables the device (refer to Table 2) without impact to t_{ELQV} .
4. The timing is defined from the first edge of CE_0 , CE_1 or BS that enables the device.
5. The timing is defined from the first edge of CE_0 , CE_1 or BS that disables the device.

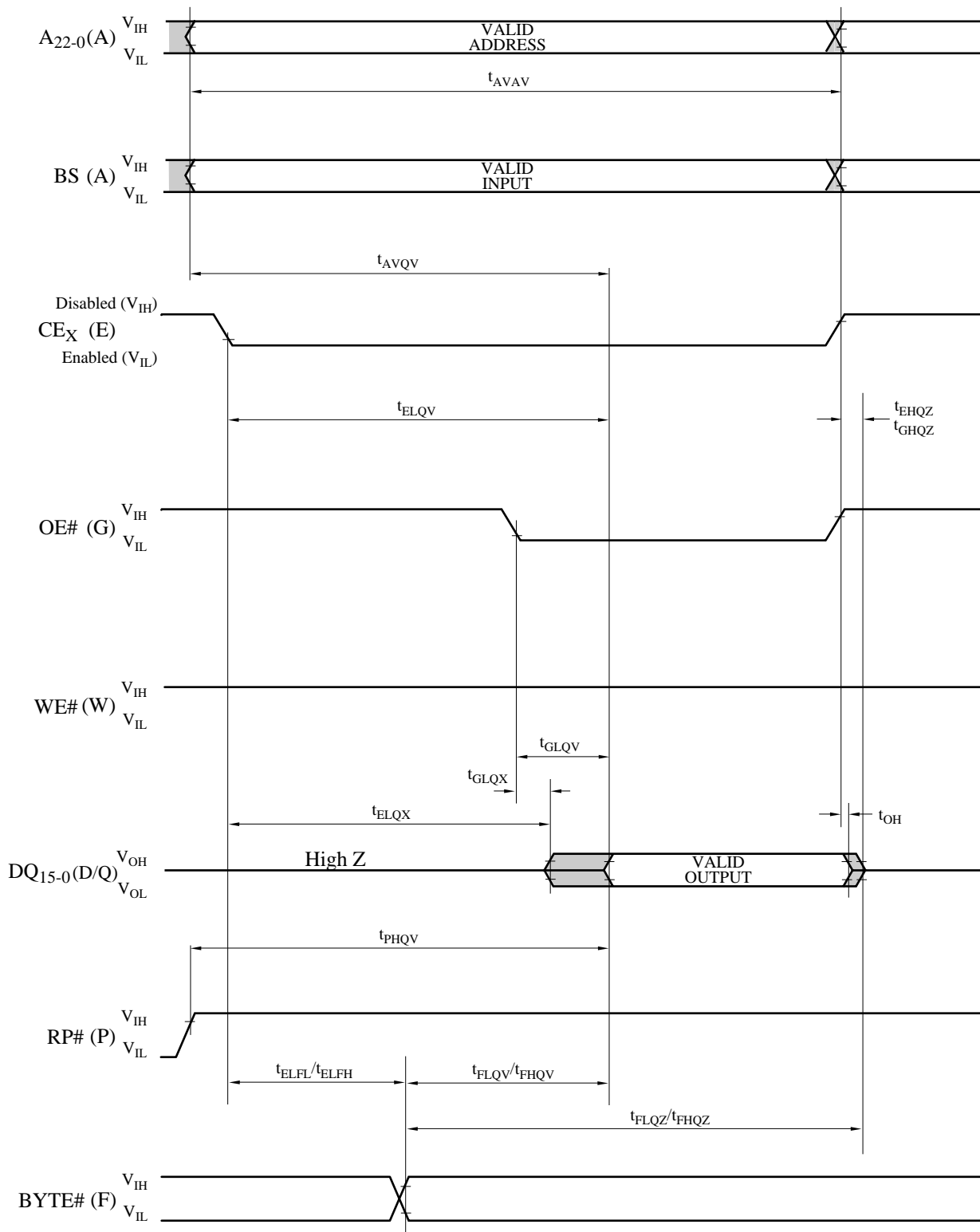


Figure 6. AC Waveform for 1-Word/ 1-Byte Read Operations
(Status Register, Identifier Codes, OTP Block or Query Code)

NOTE:

1. Status register, identifier codes, OTP block and query code can only be read in 1 word/ 1 byte read operations.

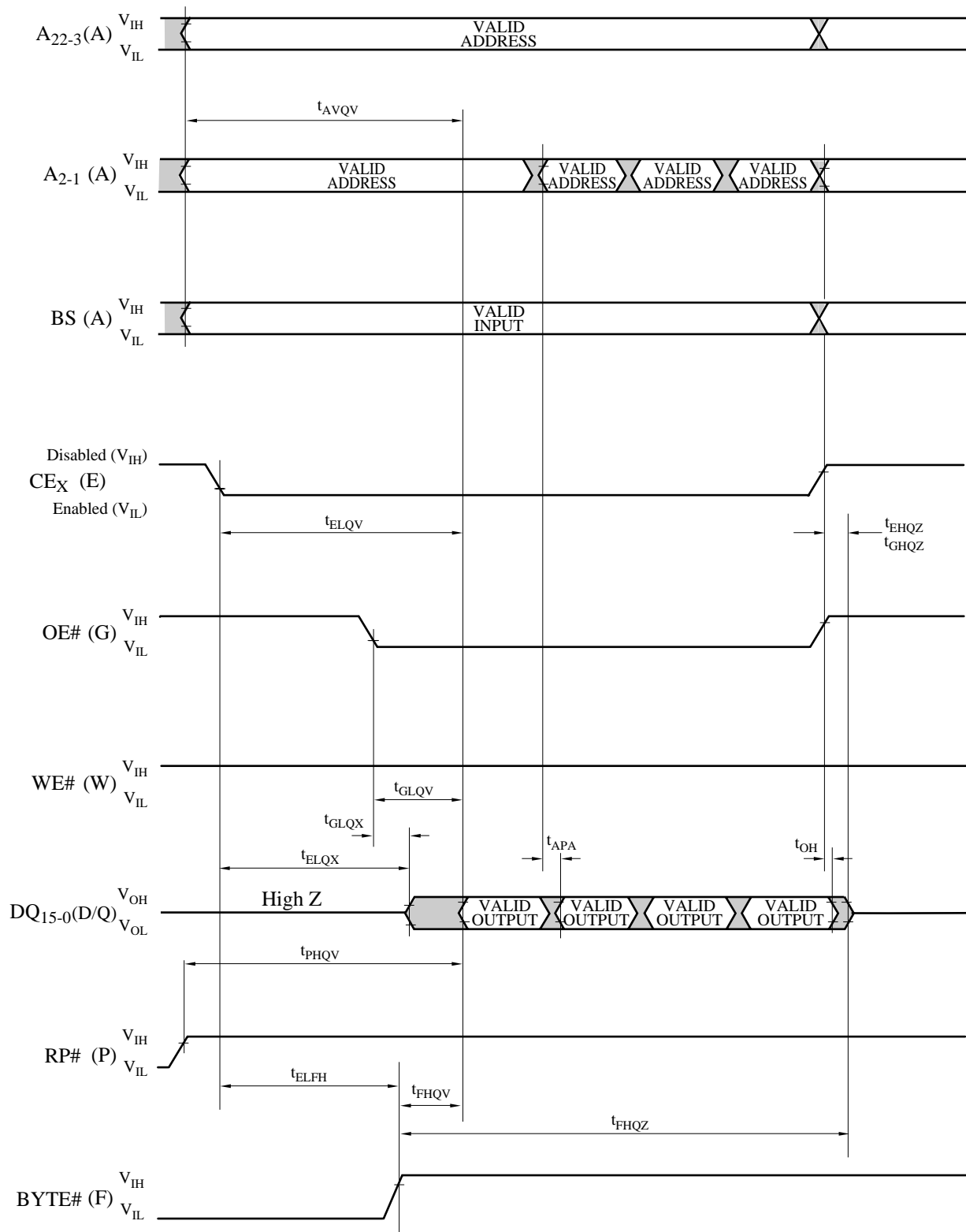


Figure 7. AC Waveform for 4-Word Page Mode Read Operations (Memory Array)

NOTE:

1. Memory array supports page mode read operations.

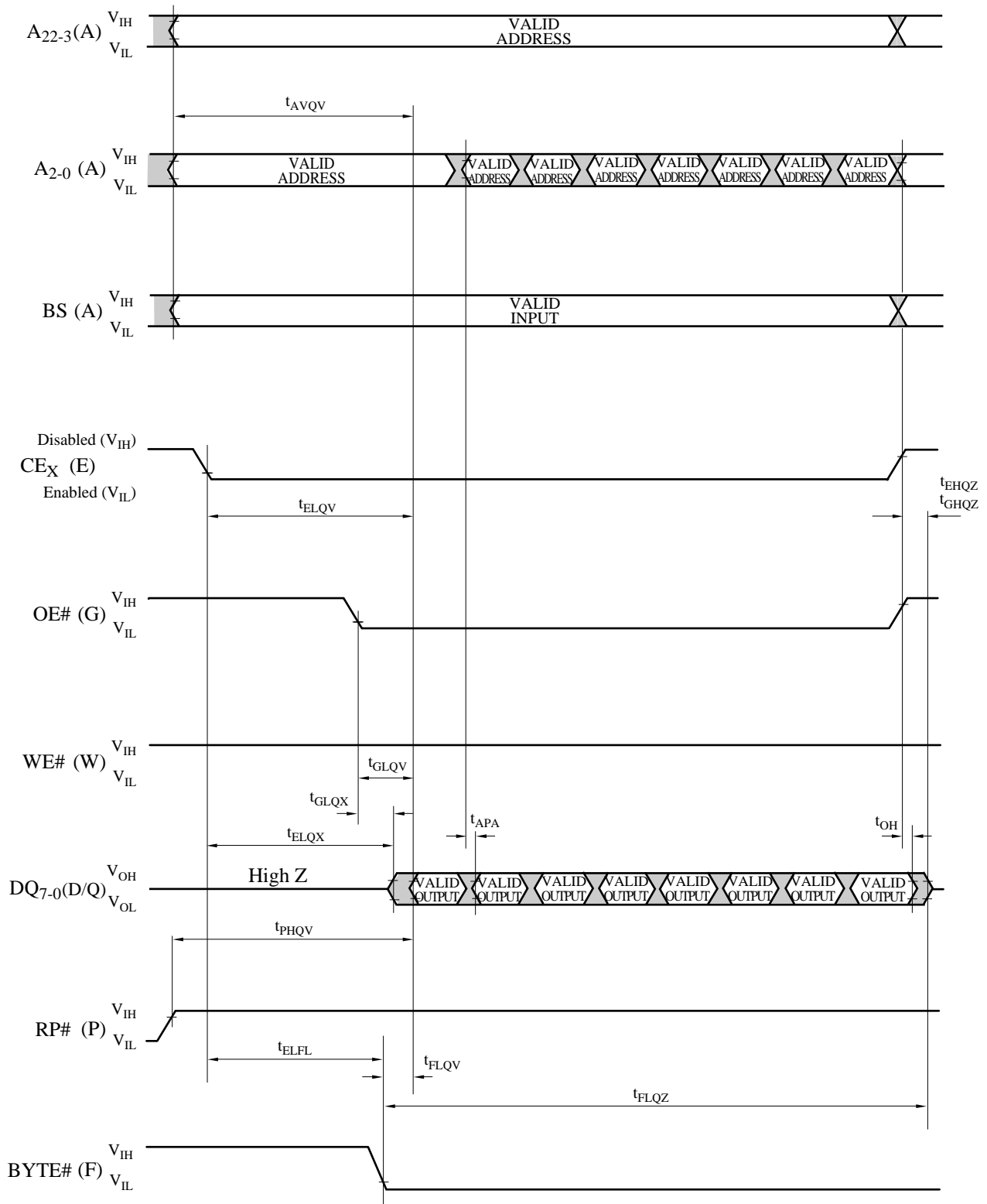


Figure 8. AC Waveform for 8-Byte Page Mode Read Operations (Memory Array)

NOTE:

1. Memory array supports page mode read operations.

1.2.5 AC Characteristics - Write Operations ^{(1), (2)}

 $V_{CC}=2.7V-3.6V, T_A=-40^{\circ}C \text{ to } +85^{\circ}C$

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		120		ns
$t_{PHWL} (t_{PHEL})$	RP# High Recovery to WE# (CE _X) Going Low	3, 9	1		μs
$t_{ELWL} (t_{WLEL})$	CE _X (WE#) Setup to WE# (CE _X) Going Low	9	0		ns
$t_{WLWH} (t_{ELEH})$	WE# (CE _X) Pulse Width Low	4, 9, 10	70		ns
$t_{DVWH} (t_{DVEH})$	Data Setup to WE# (CE _X) Going High	7, 10	50		ns
$t_{AVWH} (t_{AVEH})$	Address Setup to WE# (CE _X) Going High	7, 10	55		ns
$t_{WHEH} (t_{EHWH})$	CE _X (WE#) Hold from WE# (CE _X) High	10	0		ns
$t_{WHDX} (t_{EHDX})$	Data Hold from WE# (CE _X) High	10	0		ns
$t_{WHAX} (t_{EHAX})$	Address Hold from WE# (CE _X) High	10	0		ns
$t_{WHWL} (t_{EHEL})$	WE# (CE _X) Pulse Width High	5, 9, 10	30		ns
$t_{VVWH} (t_{VVEH})$	V _{PEN} Setup to WE# (CE _X) Going High	3, 10	0		ns
$t_{WHGL} (t_{EHGL})$	Write Recovery before Read	8	35		ns
$t_{WHR0} (t_{EHR0})$ $t_{WHRL} (t_{EHL})$	WE# (CE _X) High to SR.7 Going "0", STS Going Low	10, 11		500	ns
t_{QVVL}	V _{PEN} Hold from Valid SRD, STS High Z	3, 6, 11	0		ns
t_{FLWH}/t_{FHWL} (t_{FLEH}/t_{FHEH})	BYTE# Setup to WE# (CE _X) Going High	10	50		ns
t_{WHFL}/t_{WHFH} (t_{EHFL}/t_{EHFH})	BYTE# Hold from WE# (CE _X) High	10	90		ns

NOTES:

- The timing characteristics for reading the status register during block erase, (page buffer) program, block lock configuration and OTP program operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
- A write operation can be initiated and terminated with either CE₀, CE₁ or WE#.
BS transitions must not occur when CE₀=CE₁=V_{IL} and WE#=V_{IL}.
- Sampled, not 100% tested.
- Write pulse width low (t_{WP}) is defined from the first edge of CE₀ or CE₁ that enables the device or the falling edge of WE# (whichever occurs last) to the first edge of CE₀ or CE₁ that disables the device or the rising edge of WE# (whichever occurs first). Hence, t_{WP}=t_{WLWH}=t_{ELEH}=t_{WLEH}=t_{ELWH}.
- Write pulse width high (t_{WPH}) is defined from the first edge of CE₀ or CE₁ that disables the device or the rising edge of WE# (whichever occurs first) to the first edge of CE₀ or CE₁ that enables the device or the falling edge of WE# (whichever occurs last). Hence, t_{WPH}=t_{WHWL}=t_{EHEL}=t_{WHEL}=t_{EHWL}.
- V_{PEN} should be held at V_{PEN}=V_{PENH} until determination of block erase, (page buffer) program, block lock configuration or OTP program success (SR.1/3/4/5=0).
- Refer to Table 5 for valid address and data for block erase, (page buffer) program, block lock configuration and OTP program.
- The output delay time t_{AVQV} or t_{ELQV} is required in addition to t_{WHGL} (t_{EHGL}) for read operations after command writes.
- The timing is defined from the first edge of CE₀ or CE₁ that enables the device.
- The timing is defined from the first edge of CE₀ or CE₁ that disables the device.
- STS timings depend on STS configuration.

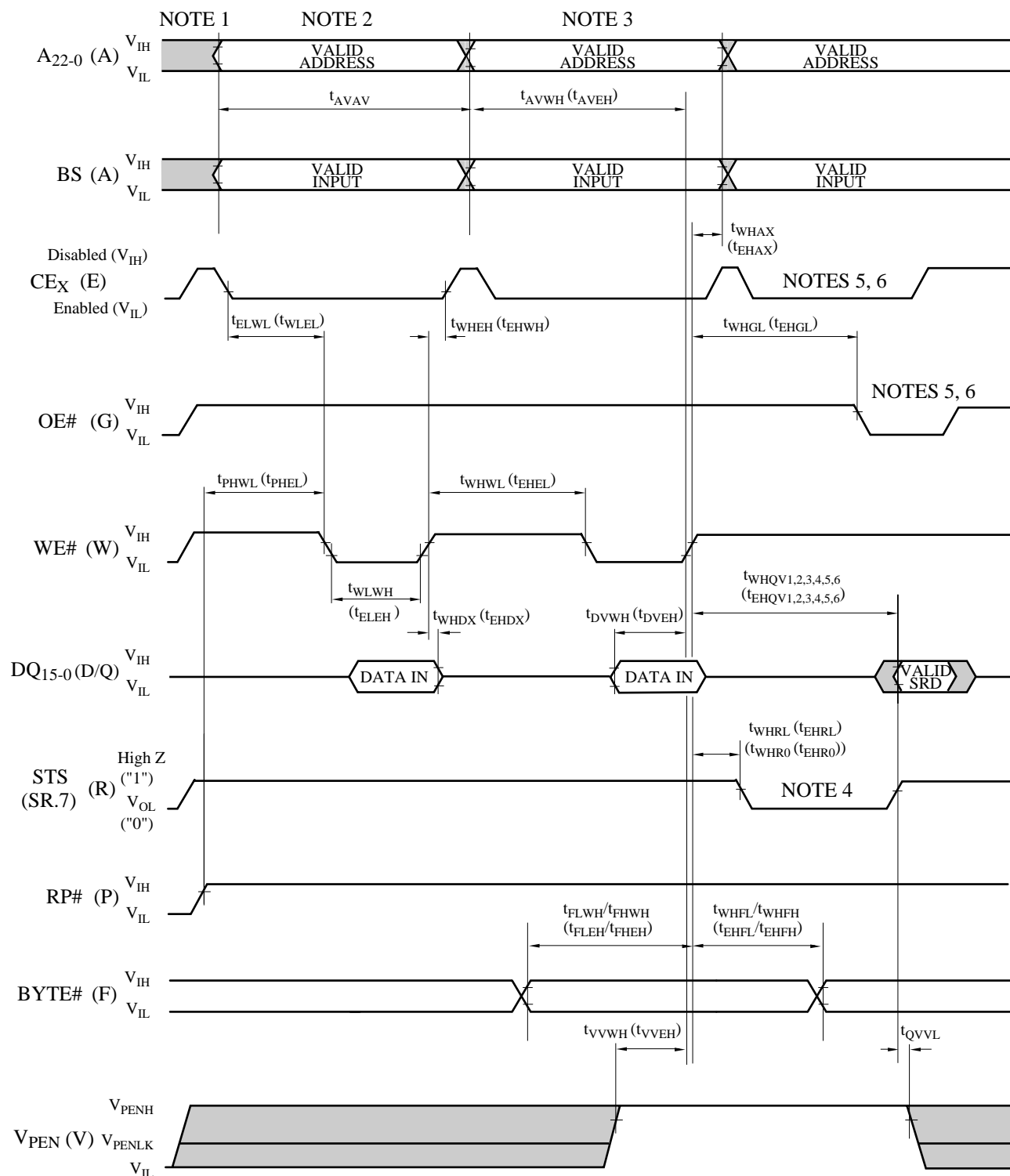


Figure 9. AC Waveform for Write Operations

1.2.6 Reset Operations

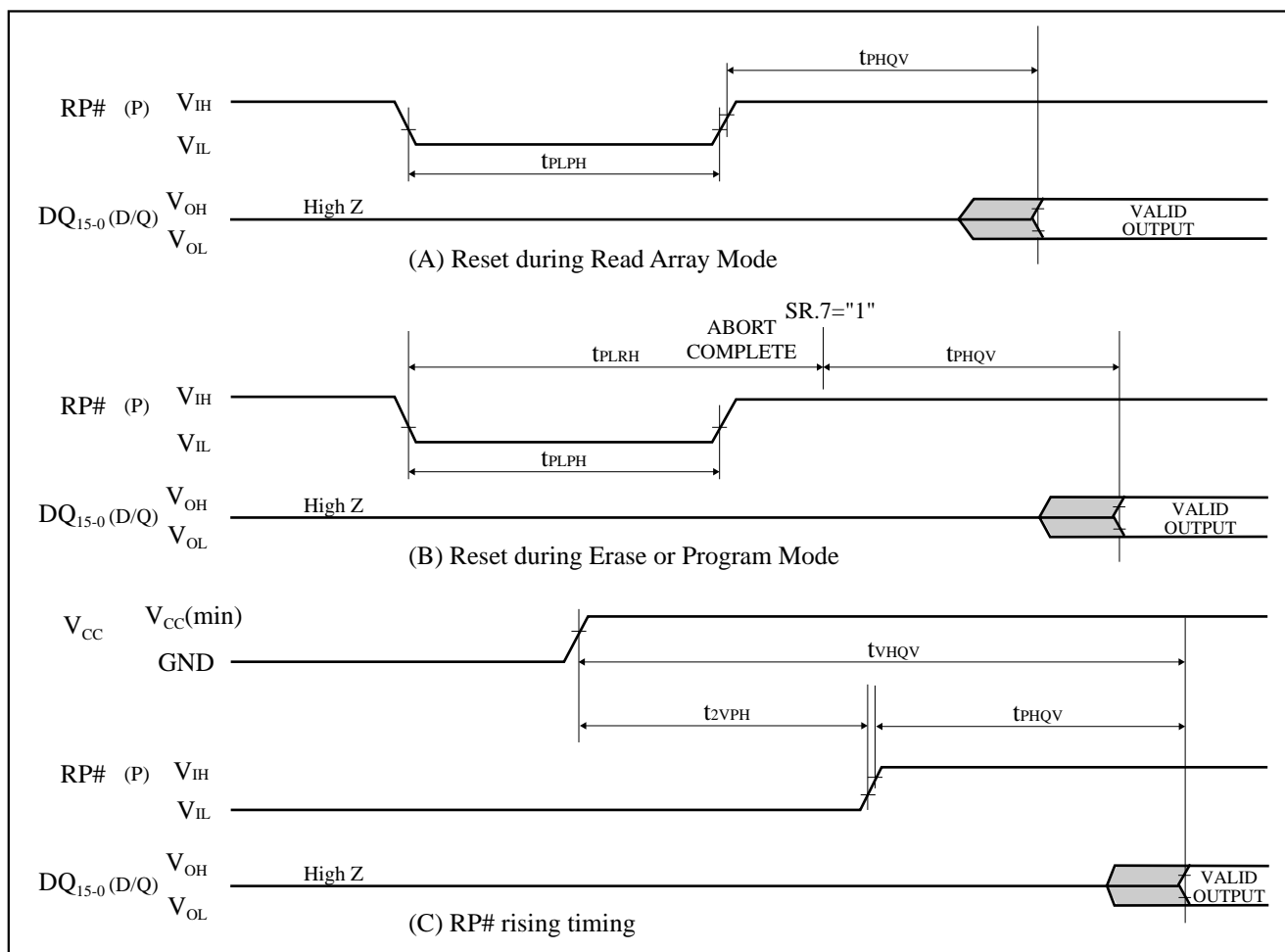


Figure 10. AC Waveform for Reset Operations

Reset AC Specifications ($V_{CC}=2.7V-3.6V$, $T_A=-40^{\circ}C$ to $+85^{\circ}C$)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{PLPH}	RP# Low to Reset during Read (RP# must be low during power-up.)	1, 2, 3	100		ns
t_{PLRH}	RP# Low to Reset during Erase or Program	1, 3, 4		30	μs
t_{2VPH}	V_{CC} 2.7V to RP# High	1, 3, 5	100		ns
t_{VHQP}	V_{CC} 2.7V to Output Delay	3		1	ms

NOTES:

1. A reset time, t_{PHQV} , is required from the later of SR.7 (STS) going "1" (High Z) or RP# going high until outputs are valid. Refer to AC Characteristics - Read-Only Operations for t_{PHQV} .
2. The device may reset if t_{PLPH} is $<100ns$, but this is not guaranteed.
3. Sampled, not 100% tested.
4. If RP# asserted while a block erase, (page buffer) program, block lock configuration or OTP program operation is not executing, the reset will complete within 100ns.
5. When the device power-up, holding RP# low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

1.2.7 Block Erase, (Page Buffer) Program and Block Lock Configuration Performance⁽³⁾

$V_{CC}=2.7V-3.6V$, $T_A=-40^{\circ}C$ to $+85^{\circ}C$

Symbol	Parameter	Notes	$V_{PEN}=V_{PENH}$			Unit
			Min.	Typ. ⁽¹⁾	Max.	
	Page Buffer Program Time (Time to Program 16 words/ 32 bytes)	2, 6, 7		400	1200	μs
$t_{WHQV3}/$ t_{EHQV3}	Program Time	2		210	630	μs
	Block Program Time (Using Page Buffer Program Command)	2		1.6	4.8	s
$t_{WHQV4}/$ t_{EHQV4}	Block Erase Time	2		1	5	s
$t_{WHQV5}/$ t_{EHQV5}	Set Block Lock Bit Time	2		64	85	μs
$t_{WHQV6}/$ t_{EHQV6}	Clear Block Lock Bits Time	2		0.5	0.7	s
$t_{WHRH1}/$ t_{EHRH1}	(Page Buffer) Program Suspend Latency Time to Read	4		25	90	μs
$t_{WHRH2}/$ t_{EHRH2}	Block Erase Suspend Latency Time to Read	4		26	40	μs
t_{ERES}	Latency Time from Block Erase Resume Command to Block Erase Suspend Command	5	600			μs

NOTES:

1. Typical values measured at $V_{CC}=3.0V$, $V_{PEN}=3.0V$ and $T_A=+25^{\circ}C$. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.
4. A latency time is required from writing suspend command (the first edge of CE_0 or CE_1 that disables the device or the rising edge of $WE\#$) until $SR.7$ going "1" or STS going High Z.
5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t_{ERES} and its sequence is repeated, the block erase operation may not be finished.
6. These values are valid when the page buffer is full, and the start address is aligned on a 16-word/ 32-byte boundary.
7. Program time per byte (t_{WHQV1}/t_{EHQV1}) is 12.5 μs /byte (typical).
Program time per word (t_{WHQV2}/t_{EHQV2}) is 25.0 μs /word (typical).

2 Related Document Information⁽¹⁾

Document No.	Document Name
FUM03201	LH28F640SP series Appendix

NOTE:

1. International customers should contact their local SHARP or distribution sales offices.

3 Package and packing specification

[Applicability]

This specification applies to IC package of the LEAD-FREE delivered as a standard specification.

1.Storage Conditions.

1-1.Storage conditions required before opening the dry packing.

- Normal temperature : 5~40°C
- Normal humidity : 80%(Relative humidity) max.
- "Humidity" means "Relative humidity"

1-2.Storage conditions required after opening the dry packing.

In order to prevent moisture absorption after opening, ensure the following storage conditions apply:

- (1) Storage conditions for one-time soldering. (Convection reflow^{*1}, IR/Convection reflow.^{*1}, or Manual soldering.)
 - Temperature : 5~25°C
 - Humidity : 60% max.
 - Period : 96 hours max. after opening.
- (2) Storage conditions for two-time soldering. (Convection reflow^{*1}, IR/Convection reflow.^{*1})
 - a. Storage conditions following opening and prior to performing the 1st reflow.
 - Temperature : 5~25°C
 - Humidity : 60% max.
 - Period : 96 hours max. after opening.
 - b. Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow.
 - Temperature : 5~25°C
 - Humidity : 60% max.
 - Period : 96 hours max. after completion of the 1st reflow.

^{*1}:Air or nitrogen environment.

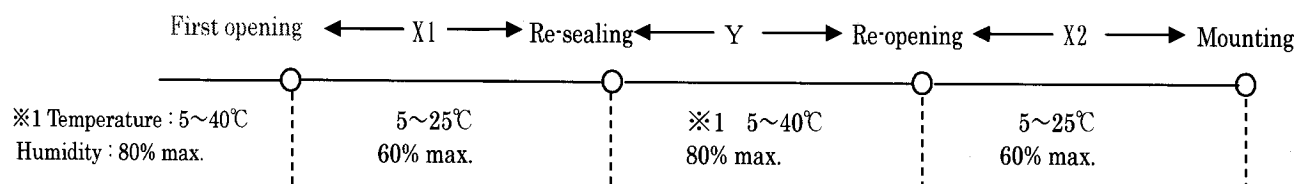
1-3.Temporary storage after opening.

To re-store the devices before soldering, do so only once and use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using heat-sealing.

The storage period, temperature and humidity must be as follows :

(1) Storage temperature and humidity.

※1 : External atmosphere temperature and humidity of the dry packing.



(2) Storage period.

- X1 + X2 : Refer to Section 1-2(1) and (2)a , depending on the mounting method.
- Y : Two weeks max.

2. Baking Condition.

(1) Situations requiring baking before mounting.

- Storage conditions exceed the limits specified in Section 1-2 or 1-3.
- Humidity indicator in the desiccant was already red (pink) when opened.
(Also for re-opening.)

(2) Recommended baking conditions.

- Baking temperature and period :
120°C for 16~24 hours.
- The above baking conditions apply since the trays are heat-resistant.

(3) Storage after baking.

- After baking, store the devices in the environment specified in Section 1-2 and mount immediately.

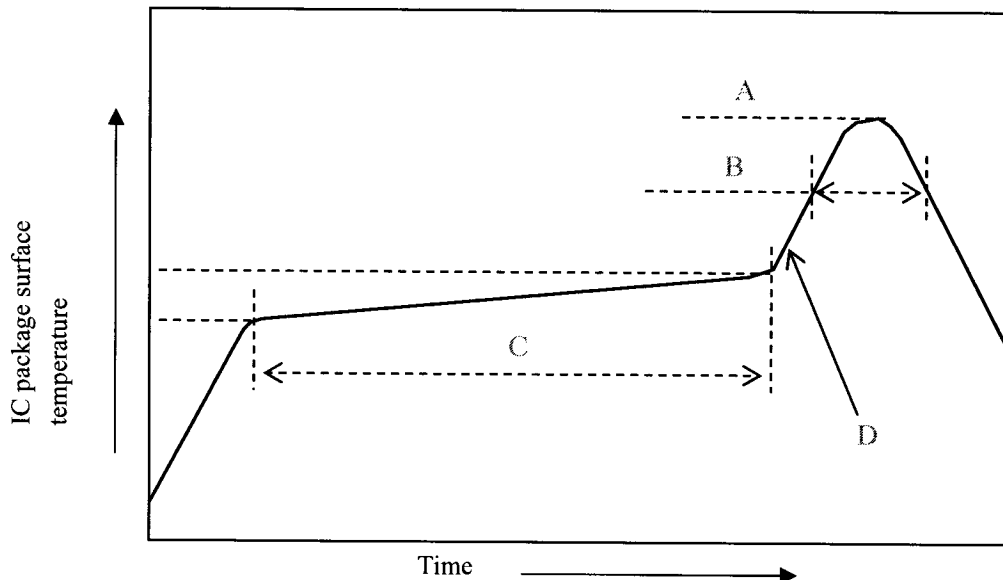
3. Surface mount conditions.

The following soldering condition are recommended to ensure device quality.

3-1.Soldering.

(1) Convection reflow or IR/Convection. (one-time soldering or two-time soldering in air or nitrogen environment)

- Temperature and period :
 - A) Peak temperature. 250°C max.
 - B) Heating temperature. 40 to 60 seconds as 220°C
 - C) Preheat temperature. It is 150 to 200°C, and is 120±30 seconds
 - D) Temperature increase rate. It is 1 to 3°C/seconds
- Measuring point : IC package surface.
- Temperature profile:



(2) Manual soldering (soldering iron) (one-time soldering only)

Soldering iron should only touch the IC's outer leads.

- Temperature and period :

380°C max. for 3 seconds / pin max.

(Soldering iron should only touch the IC's outer leads.)

- Measuring point : Soldering iron tip.

4. Condition for removal of residual flux.

- (1) Ultrasonic washing power : 25 watts / liter max.
- (2) Washing time : Total 1 minute max.
- (3) Solvent temperature : 15~40°C

5. Package outline specification.

Refer to the attached drawing.

(Plastic body dimensions do not include burr of resin.)

The contents of LEAD-FREE TYPE application of the specifications. (*2)

6. Markings.

6-1. Marking details. (The information on the package should be given as follows.)

- (1) Product name : LH28F128SPHTD-PTLZ5
- (2) Company name : SHARP
- (3) Date code : (Example) YYWW XXX
 - YY → Denotes the production year. (Last two digits of the year.)
 - WW → Denotes the production week. (01 · 02 · ~ · 52 · 53)
 - XXX → Denotes the production ref. code (1~3 digits).
- (4) "JAPAN" indicates the country of origin.

6-2. Marking layout.

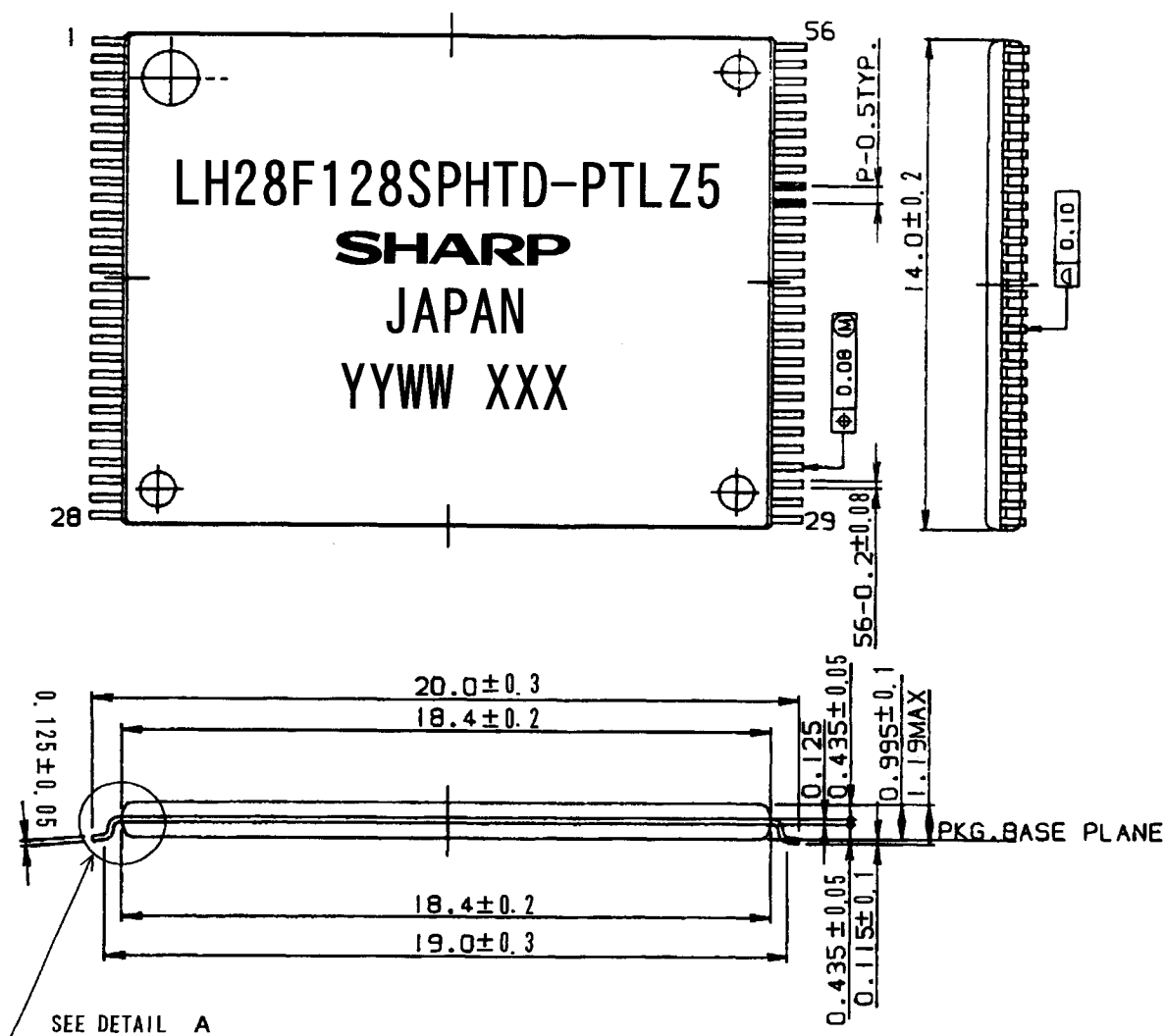
The layout is shown in the attached drawing.

(However, this layout does not specify the size of the marking character and marking position.)

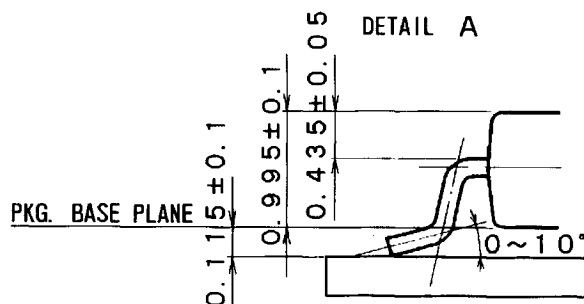
*2 The contents of LEAD-FREE TYPE application of the specifications.

LEAD FINISH or BALL TYPE	LEAD-FREE TYPE (Sn-Bi)
DATE CODE	They are those with an underline.
The word of " LEAD FREE" is printed on the packing label	Printed

(Note) It is those with an underline printing in a date code because of a LEAD-FREE type.



TSOP056-P-1420-AA1115



LEAD TYPE	LEAD FINISH		LEAD MATERIAL	
	Sn-Bi PLATING		42Alloy	
NAME	TSOP056-P-1420			NOTE : Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA1115	UNIT	mm	

7. Packing Specifications (Dry packing for surface mount packages.)

7-1. Packing materials.

Material name	Material specifications	Purpose
Inner carton	Cardboard (910 devices / inner carton max.)	Packing the devices. (10 trays / inner carton)
Tray	Conductive plastic (91 devices / tray)	Securing the devices.
Upper cover tray	Conductive plastic (1 tray / inner carton)	Securing the devices.
Laminated aluminum bag	Aluminum polyethylene	Keeping the devices dry.
Desiccant	Silica gel	Keeping the devices dry.
Label	Paper	Indicates part number, quantity, and packed date.
PP band	Polypropylene (3 pcs. / inner carton)	Securing the devices.
Outer carton	Cardboard (3640 devices / outer carton max.)	Outer packing.

(Devices must be placed on the tray in the same direction.)

7-2. Outline dimension of tray.

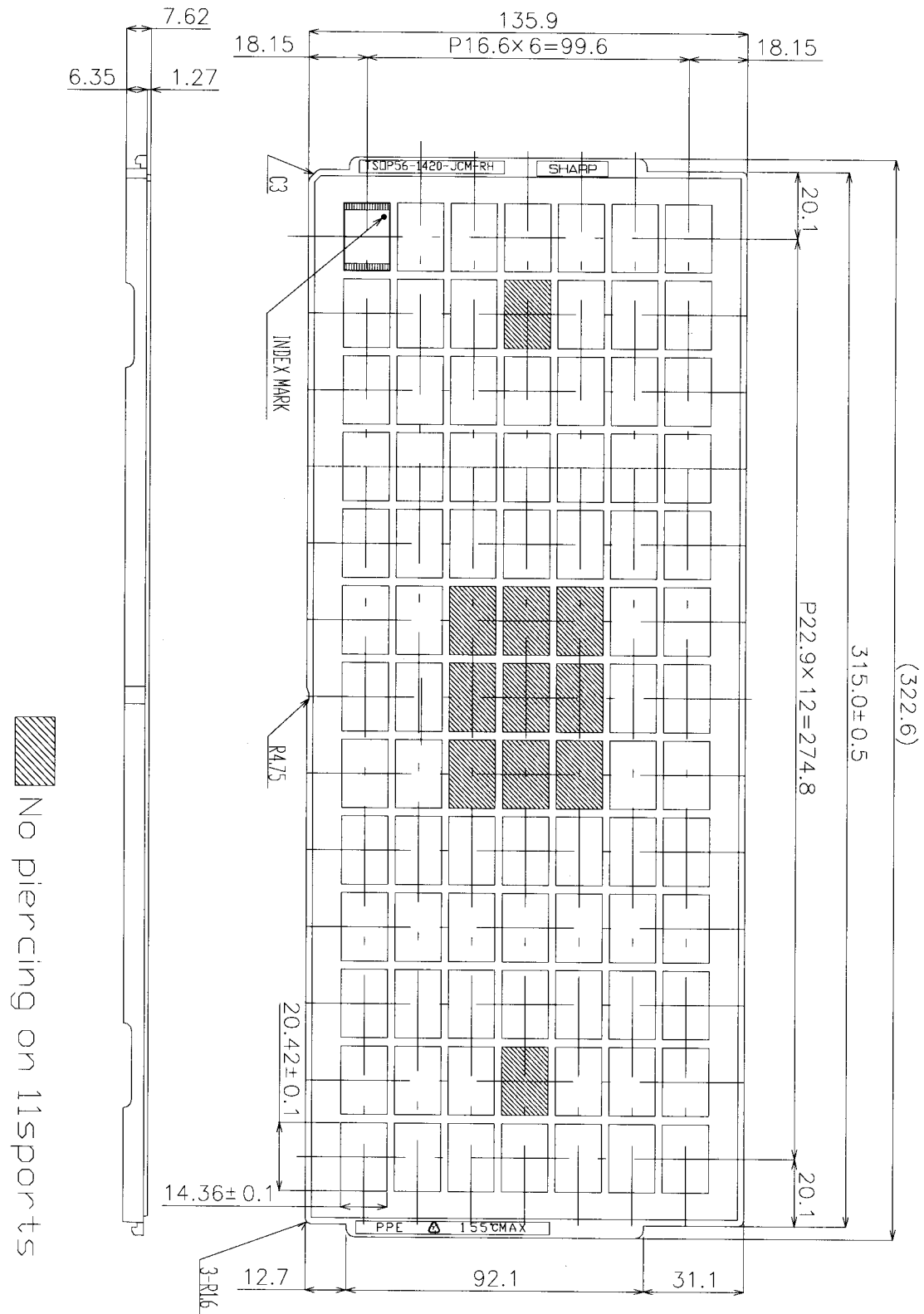
Refer to the attached drawing.

7-3. Outline dimension of carton.

Refer to the attached drawing.

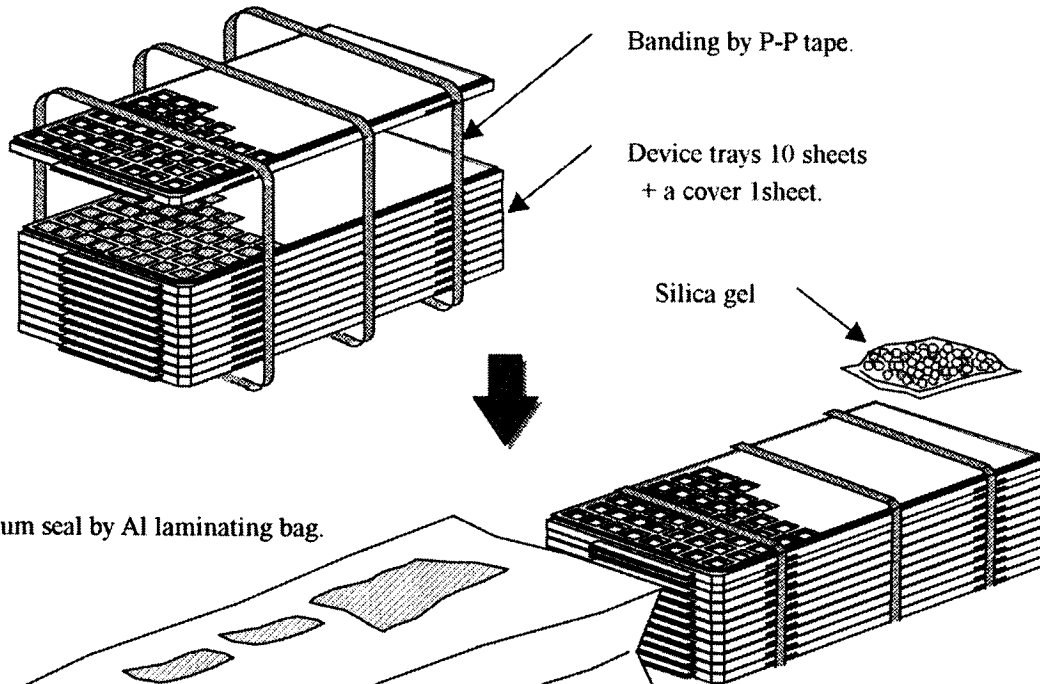
8. Precautions for use.

- (1) Opening must be done on an anti-ESD treated workbench.
All workers must also have undergone anti-ESD treatment.
- (2) The trays have undergone either conductive or anti-ESD treatment.
If another tray is used, make sure it has also undergone conductive or anti-ESD treatment.
- (3) The devices should be mounted within one year of the date of delivery.

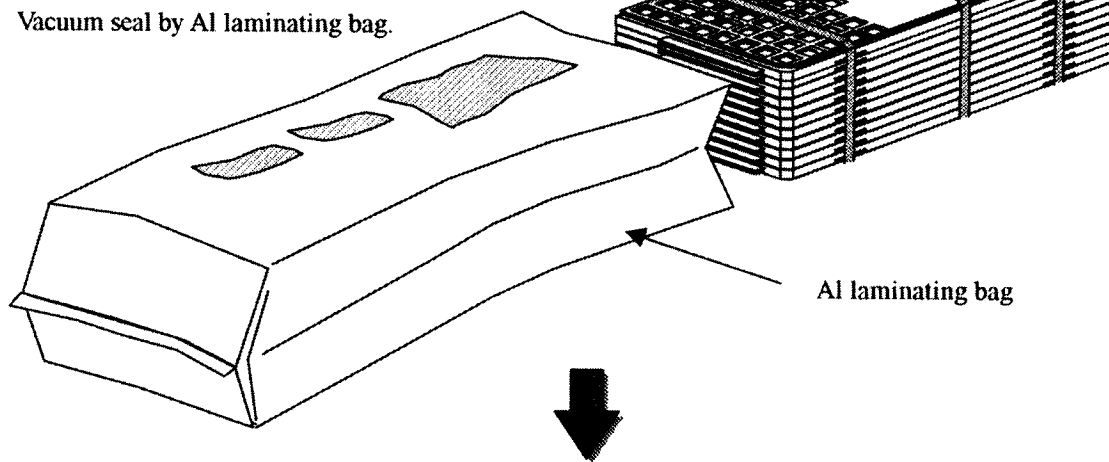


名称 NAME	TSOP56-1420-JCM-RH-N			備考 NOTE
DRAWING NO.	CV912	単位 UNIT	mm	

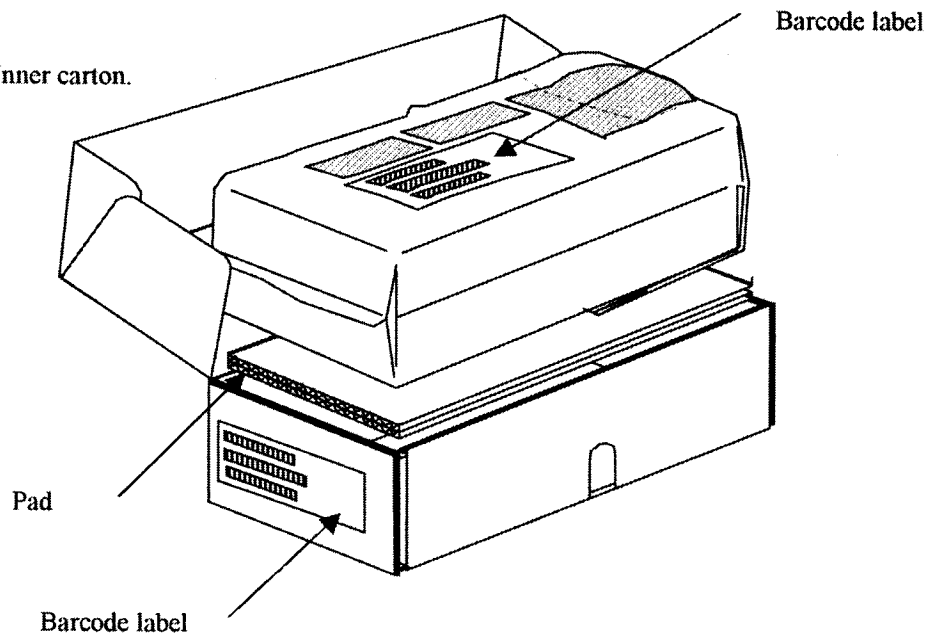
(1) Banding device tray together.



(2) Vacuum seal by Al laminating bag.

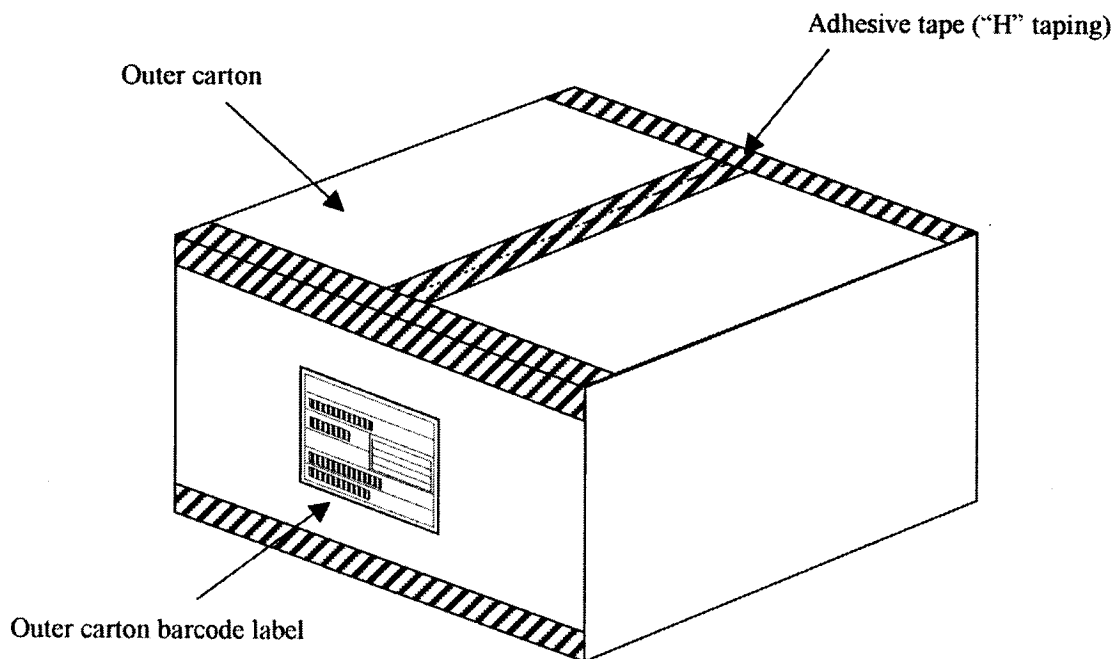
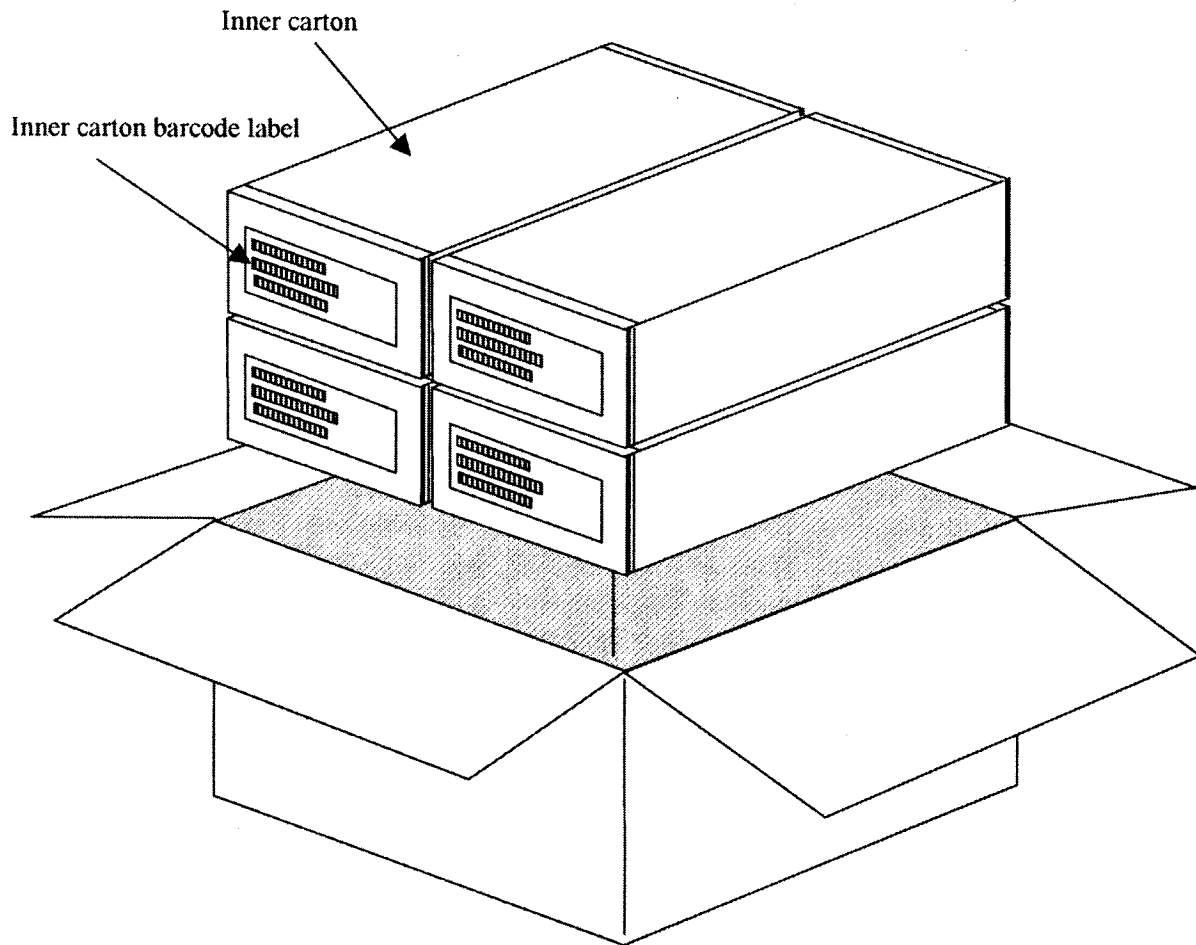


(3) Packing by Inner carton.



NAME	Packing specifications		
DRAWING NO.	BJ433c	UNIT	mm

NOTE There is a possibility different from this specification when the number of shipments is fractions.


 $L \times W \times H$

Inner carton - Outer dimensions : 360×150×95




Outer carton - Outer dimensions : 390×335×230

NOTE There is a possibility different from this specification when the number of shipments is fractions.





NAME	Packing specifications		
DRAWING NO.	BJ433d	UNIT	mm

(Note) The <LEAD-FREE> display shows a lead-free article.

Inner carton label

Product name	LH28F128SPHTD-PTLZ5 (3N) 1 LH28F128SPHTD-PTLZ5	< LEAD-FREE >	
Quantity		< QUANTITY >	910
PD lot	(3N) 2 910 XXXXXXXXXXXX 103120		
Company code			
Part No. (SHARP)	LHF12PZ5 		
Packed date	YYYY. MM. DD	TYPE : A	
	SHARP MADE IN JAPAN	EIAJ C-3 <RMK> XXXXXXXXXXXXXXXXXXXX	
	The country of origin (It displays, when the country of origin is Japan.)	Assembly management No.	

Outer carton label

Part No. (SHARP)	(4S) PKG ID : LHF12PZ5 	< LEAD-FREE >
Quantity	(Q) QUANTITY : 3640 	MADE IN JAPAN
Product name	(P) CUST PROD ID : LH28F128SPHTD-PTLZ5 	YYYY. MM. DD
Shipment lot	XXXXXXXXXXXX 	SHARP
		Packed date

The country of origin
(It displays, when the country of origin is Japan.)

(Former) EIAJ B Standard conforming

A-1 RECOMMENDED OPERATING CONDITIONS

A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

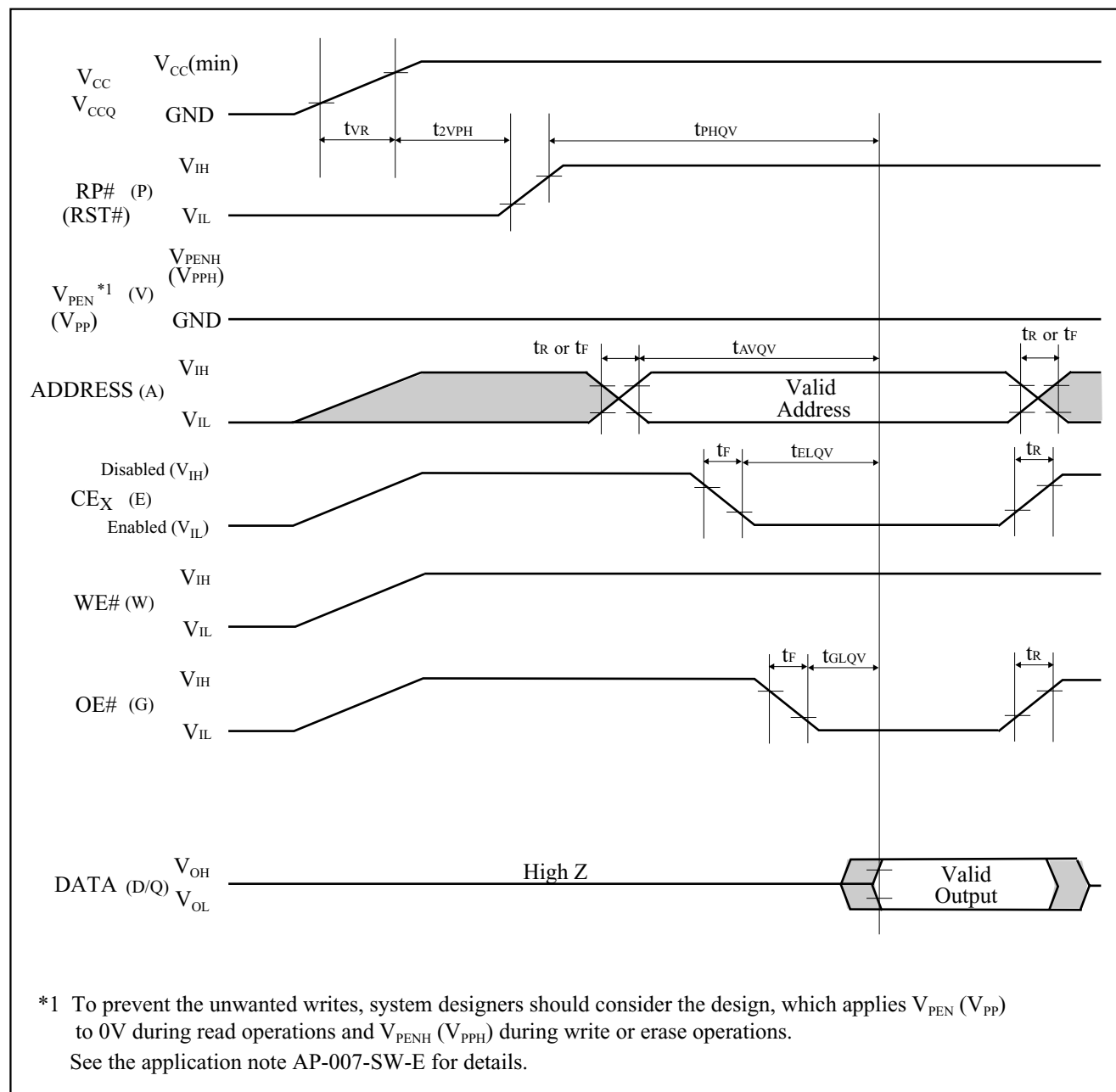


Figure A-1. AC Timing at Device Power-Up

For the AC specifications **t_{VR}**, **t_R**, **t_F** in the figure, refer to the next page. See the “ELECTRICAL SPECIFICATIONS” described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

A-1.1.1 Rise and Fall Time

Symbol	Parameter	Notes	Min.	Max.	Unit
t _{VR}	V _{CC} Rise Time	1	0.5	30000	μs/V
t _R	Input Signal Rise Time	1, 2		1	μs/V
t _F	Input Signal Fall Time	1, 2		1	μs/V

- NOTES:
- 1. Sampled, not 100% tested.
 - 2. This specification is applied for not only the device power-up but also the normal operations.

A-1.2 Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

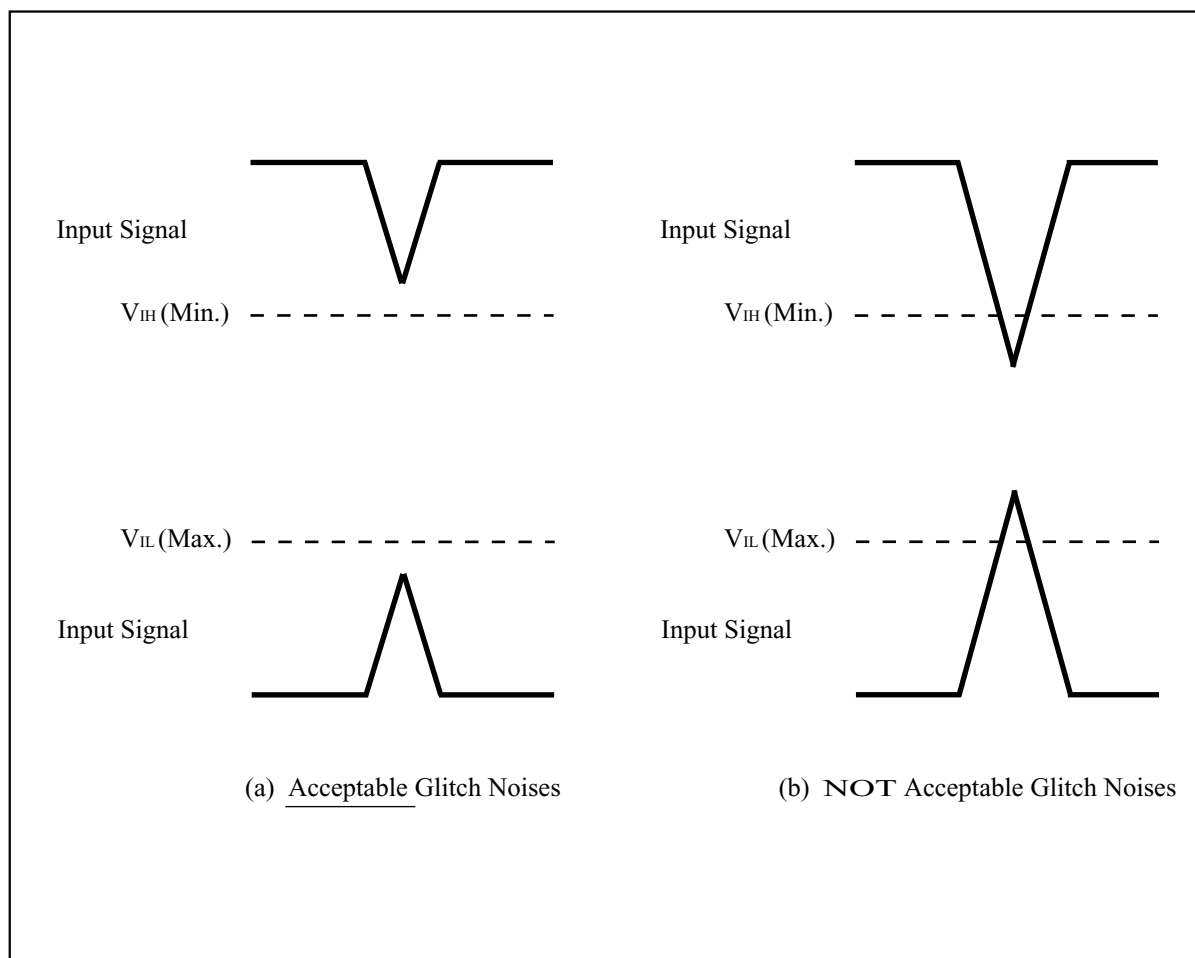


Figure A-2. Waveform for Glitch Noises

See the "DC CHARACTERISTICS" described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

A-2 RELATED DOCUMENT INFORMATION⁽¹⁾

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, V_{PP} Electric Potential Switching Circuit

NOTE:

1. International customers should contact their local SHARP or distribution sales office.

SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.

Suggested applications (if any) are for standard use; See Important Restrictions for limitations on special applications. See Limited Warranty for SHARP's product warranty. The Limited Warranty is in lieu, and exclusive of, all other warranties, express or implied. ALL EXPRESS AND IMPLIED WARRANTIES, INCLUDING THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR USE AND FITNESS FOR A PARTICULAR PURPOSE, ARE SPECIFICALLY EXCLUDED. In no event will SHARP be liable, or in any way responsible, for any incidental or consequential economic or property damage.

**NORTH AMERICA**

SHARP Microelectronics of the Americas
5700 NW Pacific Rim Blvd.
Camas, WA 98607, U.S.A.
Phone: (1) 360-834-2500
Fax: (1) 360-834-8903
Fast Info: (1) 800-833-9437
www.sharpsma.com

EUROPE

SHARP Microelectronics Europe
Division of Sharp Electronics (Europe) GmbH
Sonninstrasse 3
20097 Hamburg, Germany
Phone: (49) 40-2376-2286
Fax: (49) 40-2376-2232
www.sharpsme.com

JAPAN

SHARP Corporation
Electronic Components & Devices
22-22 Nagaike-cho, Abeno-Ku
Osaka 545-8522, Japan
Phone: (81) 6-6621-1221
Fax: (81) 6117-725300/6117-725301
www.sharp-world.com

TAIWAN

SHARP Electronic Components
(Taiwan) Corporation
8F-A, No. 16, Sec. 4, Nanking E. Rd.
Taipei, Taiwan, Republic of China
Phone: (886) 2-2577-7341
Fax: (886) 2-2577-7326/2-2577-7328

SINGAPORE

SHARP Electronics (Singapore) PTE., Ltd.
438A, Alexandra Road, #05-01/02
Alexandra Technopark,
Singapore 119967
Phone: (65) 271-3566
Fax: (65) 271-3855

KOREA

SHARP Electronic Components
(Korea) Corporation
RM 501 Geosung B/D, 541
Dohwa-dong, Mapo-ku
Seoul 121-701, Korea
Phone: (82) 2-711-5813 ~ 8
Fax: (82) 2-711-5819

CHINA

SHARP Microelectronics of China
(Shanghai) Co., Ltd.
28 Xin Jin Qiao Road King Tower 16F
Pudong Shanghai, 201206 P.R. China
Phone: (86) 21-5854-7710/21-5834-6056
Fax: (86) 21-5854-4340/21-5834-6057

Head Office:

No. 360, Bashen Road,
Xin Development Bldg. 22
Waigaoqiao Free Trade Zone Shanghai
200131 P.R. China
Email: smc@china.global.sharp.co.jp

HONG KONG

SHARP-ROXY (Hong Kong) Ltd.
3rd Business Division,
17/F, Admiralty Centre, Tower 1
18 Harcourt Road, Hong Kong
Phone: (852) 28229311
Fax: (852) 28660779
www.sharp.com.hk

Shenzhen Representative Office:

Room 13B1, Tower C,
Electronics Science & Technology Building
Shen Nan Zhong Road
Shenzhen, P.R. China
Phone: (86) 755-3273731
Fax: (86) 755-3273735