CMOS IC

LC65F1306A

4-Bit Single-Chip CMOS Microcontroller for Small-Scale Control Applications

Preliminary

Overview

The LC65F1306A belongs to our 4-bit single-chip microcontroller LC6500 series fabricated using CMOS process technology. They are ideally suited for use in small-scale control applications. Their basic architecture and instruction set are the same. These microcontrollers include an 8-input 8-bit A/D converter and are appropriate for use in a wide range of applications. That range includes applications with a small number of control circuits that were previously implemented in standard logic, and applications with a larger scale such as home appliances, automotive equipment, communications equipment, office equipment, and audio equipment such as decks and players. This microcontroller, with some exceptions, has identical functions to the LC651306A, 1304A, 1302A and 1301A mask ROM version microcontrollers. It can also be used as an OTP version microcontroller. Further, through a rewrite operation on the FLASH memory, the LC65F1306A can be used in applications where previously microcontrollers of this type could not have been implemented.

Features

1) CMOS technology for a low-power consumption operation (A standby function that can be invoked under program control is also provided.)

2) Flash ROM/RAM
   LC65F1306A Flash ROM : 6K × 8 bits, RAM : 256 × 4 bits

3) Instruction set : 81 instructions common to all microcontrollers of the LC6500 series

4) Wide operating voltage range : 3.0 V to 5.5 V

5) Instruction cycle time : 0.92 μs

6) On-chip serial I/O port

7) Flexible I/O port
- Number of ports : 5 ports / 18 pins (max.)
- All ports : Input / output common
  Input / output capacity voltage 15V max. (open-drain specification C and D only)
  Output current 20 mA max. sink current (Can drive an LED directly)
- Support option for system specification
  Output level in the reset mode : high/low level for port C and D specified in 4-bit unit

8) Interrupt function
  Interrupt by timer overflow (can be tested under program control)
  Interrupt by the state of the $\overline{INT}$ pin or completion of transmission/reception at serial I/O port (can be tested under program control)

9) Stack level : 8 levels (common use with interrupt)

10) Timer : 4-bit variable prescaler + 8-bit programmable counter

11) Clock oscillation options for user's intended system
- Oscillator circuit options : two-pin RC oscillator
  two-pin ceramic oscillator
- Divider circuit options : No divider
  built-in divide by 3
  built-in divide by 4

12) Continuous square wave output (64 times of the cycle time)

13) AD converter (successive approximation)
- Precise conversion (expressed in 8 bits), 8 input channels

14) Watchdog timer
- RC circuit time constant
- Watchdog timer reset function can be assigned to an external pin by the option.

15) Low voltage detection circuit
- Can be implemented by the option.

16) Factory shipment
- DIP24S, MFP24S

17) Flash Memory
- Rewrite block size : 128 bytes / page
- Erase / write voltage : 3.0 to 5.5V
- Rewritable limit : 10000 times (target number, to be decided after evaluation)
- Operating temperature : 0 to +85°C (when writing to the flash memory)
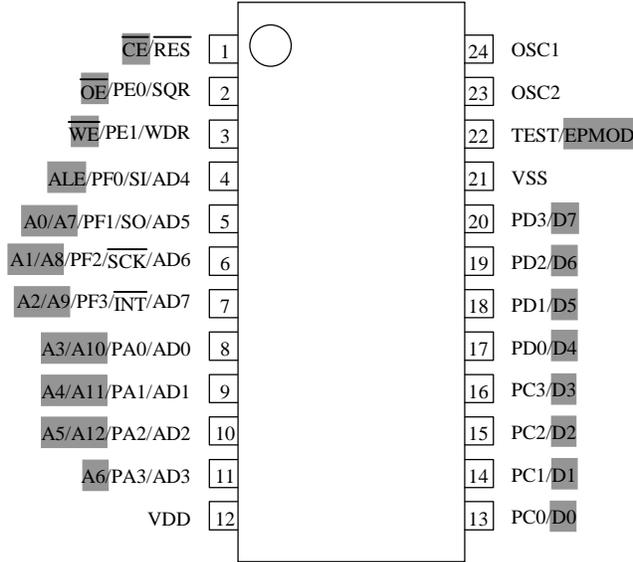 -20 to +85°C (when reading from the flash memory)

Function Table

Parameter		LC651306A/04A/02A/01A	LC65F1306A
Memory	ROM	6144 × 8 bits (1306A) 4096 × 8 bits (1304A) 2048 × 8 bits (1302A) 1024 × 8 bits (1301A)	6144 × 8 bits
	RAM	256 × 4 bits (1306A/04A/02A/01A)	256 × 4 bits
Instructions	Instruction set	81	81
	Table reference	Supported	Supported
On-chip functions	Interrupt	1 external, 1 internal	1 external, 1 internal
	Timer	4-bit variable prescaler + 8-bit timers	4-bit variable prescaler + 8-bit timers
	Stack level	8	8
	Standby function	Standby mode by the HALT instruction supported	Standby mode by the HALT instruction supported
I/O ports	Port number	18 I/O port pins	22 I/O port pins
	Serial port	Input and output in 4 or 8 bit units	Input and output in 4 or 8 bit units
	I/O voltage capacity	15 V max.	15 V max.
	Output current	10 mA typ. 20 mA max.	10 mA typ. 20 mA max.
	I/O circuit type	Open drain (N-channel) or pull-up resistor output option can be specified in 1- bit unit.	Open drain (N-channel)
	Output level at reset	High or low level output can be selected in port unit (ports C and D only)	
	Square wave output	Supported	Supported
Characteristics	Minimum cycle time	0.92 μs (VDD ≥ 2.5 V)	0.92 μs (VDD ≥ 3.0 V)
	Operating temperature	-40°C to +85°C	0°C to +85°C (when writing) -20°C to +85°C (when reading)
	Supply voltage	2.5 to 6 V	3.0 to 5.5 V
	Supply current	1.5 mA typ.	3 mA typ.
Oscillator	Oscillator	RC (800 kHz typ.) Ceramic (400k, 800k,1MHz, 4MHz)	RC (800 kHz typ.) Ceramic (400k, 800k,1MHz, 4MHz)
	Divider circuit option	1/1, 1/3, 1/4	1/1, 1/3, 1/4
Other items	Package	DIP24S MFP24S SSOP24	DIP24S MFP24S
	Watchdog timer	Supported	Supported
	OTP	Only DIP24S MFP24S	-

Note: The above oscillator and oscillator circuit constants are tentative. They will be announced as the recommended circuits for these microcontrollers are determined. Please confirm the progress of these developments periodically.

Pin Assignment

DIP24S, MFP24S

$\overline{CE}$/$\overline{RES}$	1	24 OSC1
$\overline{OE}$/PE0/SQR	2	23 OSC2
$\overline{WE}$/PE1/WDR	3	22 TEST/EPMOD
ALE/PF0/SI/AD4	4	21 VSS
A0/A7/PF1/SO/AD5	5	20 PD3/D7
A1/A8/PF2/$\overline{SCK}$/AD6	6	19 PD2/D6
A2/A9/PF3/$\overline{INT}$/AD7	7	18 PD1/D5
A3/A10/PA0/AD0	8	17 PD0/D4
A4/A11/PA1/AD1	9	16 PC3/D3
A5/A12/PA2/AD2	10	15 PC2/D2
A6/PA3/AD3	11	14 PC1/D1
VDD	12	13 PC0/D0

▓▓▓▓ : Pin function names used when writing data to on-chip Flash ROM with the PROM writer

Pin Functions

OSC1, OSC2	:	Ceramic Oscillator for OSC, RC	TEST	:	Test
$\overline{RES}$	:	Reset	AD0-AD7	:	AD converter analog input
PA0-3	:	Common I/O port A0-3	SQR	:	Square wave output
PC0-3	:	Common I/O port C0-3	WDR	:	Watch Dog Reset pin
PD0-3	:	Common I/O port D0-3	$\overline{INT}$	:	Interrupt Request pin
PE0-1	:	Common I/O port E0-1	SI	:	Serial Input pin
PF0-3	:	Common I/O port F0-3	SO	:	Serial Output pin
			$\overline{SCK}$	:	Serial Clock input/output pin

Notes: • SQR and WDR are common with PE0 and PE1 respectively.
  • SI, SO, $\overline{SCK}$, and $\overline{INT}$ are common with PF0 to PF3 respectively.

Package Dimension

(unit : mm)

3067A
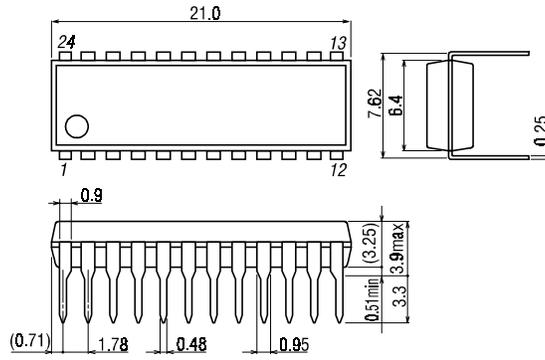
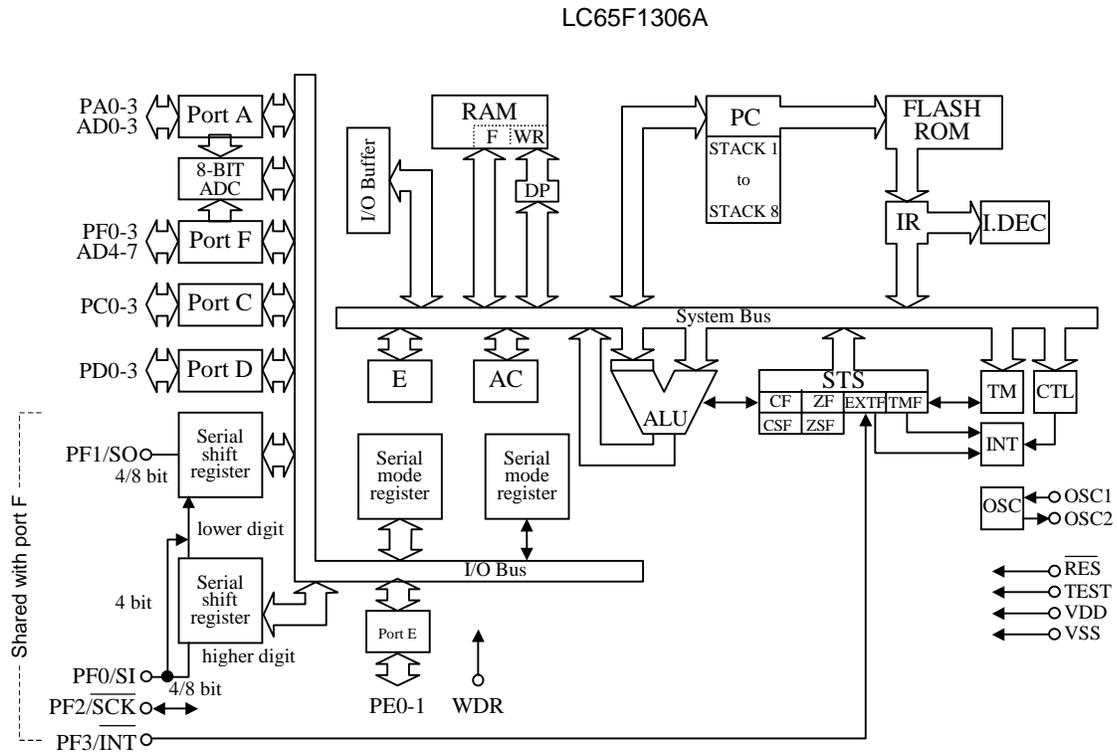

SANYO : DIP24S(300mil)

Package Dimension

(unit : mm)

3112A
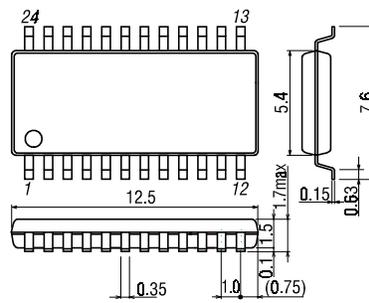
SANYO : MFP24S(300mil)

System Block Diagram

LC65F1306A

RAM	:	Data Memory	FLASH ROM	:	Program Memory
F	:	Flag	PC	:	Program Counter
WR	:	Working Register	INT	:	Interrupt control
AC	:	Accumulator	IR	:	Instruction Register
ALU	:	Arithmetic and Logic Unit	I.DEC	:	Instruction Decoder
DP	:	Data Pointer	CF, CSF	:	Carry Flag, Carry Save Flag
E	:	E register	ZF, ZSF	:	Zero Flag, Zero Save Flag
CTL	:	Control register	EXTF	:	External Interrupt Request Flag
OSC	:	Oscillation Circuit	TMF	:	Internal Interrupt Request Flag
TM	:	Timer			
STS	:	Status register			

Development Support

The following are currently in the development stage and will soon be available to the user for the development of the LC65F1306A.

1. User's manual
   Refer to the "LC65F1306A/LC651300 series user's manual."
2. Development tool manual
   Refer to the "EVA86000 Development Tool Manual for 4-bit microcontrollers."
3. Software manual
   "LC65/66 Series Software Manual"
4. Development tool
   a. For program development (EVA86000 system)
   b. For program evaluation
      Microcontroller with Flash ROM (LC65F1306)

Pin Functions

Symbol	Number of pins	I/O	Function	Option	At reset	Handling when unused
VDD VSS	1 1	- -	Power supply	-	-	-
OSC1 OSC2	1 1	Input Output	• Pins for connecting system clock oscillation RC or ceramic resonator. • Leave OSC2 open when OSC1 is used for an external clock input	(1) Two-pin RC oscillator, external clock (2) Two-pin ceramic oscillator (3) Divider option 　1. No divider 　2. Divide by 3 　3. Divide by 4	-	-
PA0-PA3/ AD0-AD3	4	I/O	• I/O port A0 to A3 　Input in 4-bit unit (IP instruction) 　Output in 4-bit unit 　(OP instruction) 　Testing in 1-bit unit 　(BP, BNP instructions) 　Set and reset in 1-bit unit 　(SPB, RPB instructions) • PA3 is used for standby mode control. • Chattering should not be occurred on the PA3 during HALT instruction execution. • All four pins have shared function. PA0/AD0:AD converter input AD0 PA1/AD1:AD converter input AD1 PA2/AD2:AD converter input AD2 PA3/AD3: converter input AD3	Open-drain output only	High-level output (The output N-channel transistors in the off state.)	Select the open-drain output option and connect to VSS.
PC0-PC3	4	I/O	•I/O port C0 to C3 The port functions are identical to those of PA0 to PA3 (See note). • The output during a reset can be selected to be either high or low as an option. Note: This port has no standby mode control function.	Open-drain output only (1) High level output during reset. (2) Low level output during reset. • (1) and (2) are specified 4 bits at a time	• High-level output. • Low-level output. (Depending on options selected)	Same as PA0 to PA3.
PD0-PD3	4	I/O	•I/O port D0 to D3 The port functions and options are identical to those of PC0 to PC3.	Same as PC0 to PC3.	Same as PC0 to PC3.	Same as PA0 to PA3.

Symbol	Number of pins	I/O	Function	Option	At reset	Handling when unused

PE0-PE1 /WDR	2	I/O	• I/O port E0 to E1
			  Input in 4-bit unit (IP instruction)
			  Output in 4-bit unit (OP instruction)
			  Set and reset in 1-bit unit
			  (SPB and PRB instructions)
			  Testing in 1-bit unit
			  (BP and BNP instructions)
			• PE0 also has a continuous pulse (64 Tcyc) output function.
			• PE1 becomes the watchdog reset pin WDR when selected as an option.
				Open -drain output only
				(1) Normal port PE1
				(2) Watchdog reset WDR
				  • Either options (1) or (2) can be selected.
					High level output (The output N-channel transistors in the off state)	Identical to those for PA0 to PA3.

PF0/SI/AD4
PF1/SO/AD5
PF2/$\overline{\text{SCK}}$/AD6
PF3/$\overline{\text{INT}}$/AD7
	4	I/O	• I/O port F0 to F3
			  The port functions and options are identical to those of PE0 to PE1 (See note).
			• PF0 to PF3 have shared functions with the serial interface pins and the $\overline{\text{INT}}$ input.
			  The function can be selected under program control.
			    SI... Serial input pin
			    $\overline{\text{SO}}$...Serial output pin
			    $\overline{\text{SCK}}$...Input and output of the serial clock signal.
			    $\overline{\text{INT}}$...Interrupt request signal
			  The serial I/O function can be switched between 4-bit and 8-bit transfers under program control.
			Note: There is no continuous pulse output function.
			• All four pins have shared function.
			  PF0/AD4: AD converter input AD4
			  PF1/AD5: AD converter input AD5
			  PF2/AD6: AD converter input AD6
			  PF3/AD7: AD converter input AD7
				Identical to those for PA0 to PA3.	Identical to those for PA0 to PA3.
					
					The serial port functions are disabled.
					
					The interrupt source is set to $\overline{\text{INT}}$.
						Identical to those for PA0 to PA3.

$\overline{\text{RES}}$	1	Input	• System reset input • Provide an external capacitor for the power-on reset. • Apply low level to this pin for 4 or more clock cycles to reset and restart the program.	-	-	-
TEST	1	Input	• Test pin for LSI. This pin must be connected to VSS during normal operation.	-	-	This pin must be connected to VSS.

User Option

User option is selected according to the information written to the user option area on the on-chip Flash ROM.

Oscillator Circuit Options

Option	Circuit	Conditions and notes
External clock		The OSC2 pin should be left open.
Two-pin RC oscillator		
Ceramic oscillator		

Divider Circuit Options

Option	Circuit	Conditions and notes
No divider (1/1)		• The oscillator frequency or external clock frequency should not exceed 4330 kHz.
Built-in divide-by-three circuit		• This option can only be used with the external clock and the ceramic oscillator options. • The oscillator frequency or external clock frequency should not exceed 4330 kHz.
Built-in divide-by-four circuit		• This option can only be used with the external clock and the ceramic oscillator options. • The oscillator frequency or external clock frequency should not exceed 4330 kHz.

Note: The following table summarizes the oscillator and divider circuit options. When selecting the divider option, the relationship between frequency and cycle time must be taken into account.

LC65F1306A Oscillator Options

Circuit type	Frequency	Divider option (Cycle time)	VDD range	Notes
Ceramic resonator	400 kHz	1/1 (10μs)	3 to 5.5V	Can not be used with the divide-by-three and divide-by-four options.
	800 kHz	1/1 (5μs)	3 to 5.5V	
	1 MHz	1/1 (4μs)	3 to 5.5V	
	4 MHz	1/1 (1μs)	3 to 5.5V	
		1/3 (3μs)	3 to 5.5V	
		1/4 (4μs)	3 to 5.5V	
External clock (used with the 2-pin RC oscillator circuit)	384 k to 4330 kHz	1/1 (10.4 to 0.92μs)	3 to 5.5V	
	1152 k to 4330 kHz	1/3 (10.4 to 2.77μs)	3 to 5.5V	
	1536 k to 4330 kHz	1/4 (10.4 to 3.70μs)	3 to 5.5V	
Two-pin RC	Use the no divider circuit option and the recommended circuit constants. When using other constants by necessity, use the frequency and VDD range identical to the external clock written above.		3 to 5.5V	
External clock used with the ceramic oscillator option	External clock drive is not possible. To use external clock drive, select the 2-pin RC oscillator option.			

Port C and D Output level Option During Reset

The Output level of the C and D ports at reset can be selected from the following two options in 4-bit unit.

Option	Conditions and notes
High level output at reset	Ports C and D in 4-bit unit
Low level output at reset	Ports C and D in 4-bit unit

Port Output Type

The I/O port type is open-drain output.

Option	Circuit	Ports
Open-drain output		Ports A, C, D, E and F

Watchdog Reset Option

This option allows the user to select how the PE1/WDR pin is to be used. It can be used as the normal port PE1, or used as the watchdog reset pin WDR.

1. Absolute Maximum Ratings at Ta=25°C, VSS=0V

Parameter	Symbol	Conditions	Applicable pins and notes	Ratings	unit
Maximum supply voltage	VDD max		VDD	-0.3 to +6.5	V
Output voltage	VO		OSC2	Output voltage generated can be over the maximum limit of the VDD.	
Input voltage	VI (1)		OSC1 (Note 1)	-0.3 to VDD+0.3	
	VI (2)		TEST, $\overline{\text{RES}}$ AV$_+$, AV$_-$	-0.3 to VDD+0.3	
I/O voltage	VIO (1)	PC0 to 3, PD0 to 3	Open-drain specification ports	-0.3 to +15	
	VIO (2)	PC0 to 3, PD0 to 3	Pull-up resistor specification ports	-0.3 to VDD+0.3	
	VIO (3)	PA0 to 3, PE0, 1, PF0 to 3		-0.3 to VDD+0.3	
Peak output current	IOP		I/O Port	-2 to +20	mA
Average output current	IOA	Average current applied to a pin for 100 ms	I/O Port	-2 to +20	
	ΣIOA(1)	The total current of PC0 to 3, PD0 to 3 and PE0 to 1. (Note 2)	PC0 to 3 PD0 to 3 PE0 to 1	-15 to +100	
	ΣIOA(2)	The total current of PF0 to 3 and PA0 to 3. (Note 2)	PF0 to 3 PA0 to 3	-15 to +100	
Maximum power consumption	Pd max (1)	Ta=-20 to +85°C (DIP package)		310	mW
	Pd max (2)	Ta=-20 to +85°C (MFP package)		220	
Operating temperature	Topr			-20 to +85	°C
Storage temperature	Tstg			-55 to +125	

2. Recommended Operating Range at Ta=-20 to +85°C, VSS=0V, VDD=3.0 to 5.5V (Unless otherwise specified)

Parameter	Symbol	Conditions		Applicable pins and notes	Ratings			unit
					min.	typ.	max.	
Operating supply voltage	VDD			VDD	3.0		5.5	V
Standby supply voltage	VST	RAM and register values retained. (Note 3)		VDD	1.8		5.5	
High level input voltage	VIH(1)	Output Nch Tr. off		Port C, D with open-drain specifications.	0.7VDD		13.5	
	VIH(2)	Output Nch Tr. off		Port A, E, F	0.7VDD		VDD	
	VIH(3)	Output Nch Tr. off		The $\overline{\text{INT}}$, $\overline{\text{SCK}}$, and SI pin with open-drain specifications.	0.8VDD		VDD	
	VIH(4)	VDD=1.8 to 5.5 V		$\overline{\text{RES}}$	0.8VDD		VDD	
	VIH(5)	External clock specifications		OSC1	0.8VDD		VDD	
Low level input voltage	VIL(1)	Output Nch Tr. off	VDD=4 to 5.5V	Port	VSS		0.3VDD	
	VIL(2)	Output Nch Tr. off	3 to 5.5V	Port	VSS		0.25VDD	
	VIL(3)	Output Nch Tr. off	VDD=4 to 5.5V	$\overline{\text{INT}}$, $\overline{\text{SCK}}$, SI	VSS		0.25VDD	
	VIL(4)	Output Nch Tr. off	3 to 5.5V	$\overline{\text{INT}}$, $\overline{\text{SCK}}$, SI	VSS		0.2VDD	
	VIL(5)	External clock specification	VDD=4 to 5.5V	OSC1	VSS		0.25VDD	
	VIL(6)	External clock specification	3 to 5.5V	OSC1	VSS		0.2VDD	
	VIL(7)		VDD=4 to 5.5V	TEST	VSS		0.3VDD	
	VIL(8)		3 to 5.5V	TEST	VSS		0.25VDD	
	VIL(9)		VDD=4 to 5.5V	$\overline{\text{RES}}$	VSS		0.25VDD	
	VIL(10)		3 to 5.5V	$\overline{\text{RES}}$	VSS		0.2VDD	
Operating frequency (cycle time)	fop (Tcyc)		VDD=3 to 5.5V		384 (10.4)		4330 (0.92)	kHz (μs)
External clock conditions Frequency	text	Fig. 1	VDD=3 to 5.5V	OSC1	384		4330	kHz
Pulse width	textH, textL		VDD=3 to 5.5V	OSC1	69			ns
Rising/falling time	textR, textF		VDD=3 to 5.5V	OSC1			50	
Recommended oscillation constants Two-pin RC oscillator	Cext Rext	Fig. 2	VDD=3 to 5.5V	OSC1, OSC2		270±5% 5.6±1%		pF kΩ
Ceramic oscillator (Note 4)		Fig. 3			See Table 1			

3. Electrical Characteristics at Ta=-20 to +85°C, VSS=0V, VDD=3.0 to 5.5V (Unless otherwise specified)

Parameter		Symbol	Conditions	Applicable pins and notes	Ratings min.	Ratings typ.	Ratings max.	unit
Input High level current		IIH(1)	Output Nch Tr. OFF (including OFF leak current of Nch Tr.) VIN=+13.5V	Port C and D with the open-drain specifications			5.0	μA
		IIH (2)	Output Nch Tr. OFF (including OFF leak current of Nch Tr.) VIN=VDD	Port A, E and G with the open-drain specifications			1.0	
		IIH (3)	When external clock is used, VIN=VDD	OSC1			1.0	
Input Low level current		IIL(1)	Output Nch Tr. OFF VIN=VSS	Ports with the open-drain specifications	-1.0			
		IIL(2)	Output Nch Tr. OFF VIN=VSS	Ports with the pull-up resistor specifications	-1.3	-0.35		mA
		IIL(3)	VIN=VSS	$\overline{RES}$	-45	-10		μA
		IIL(4)	When external clock is used, VIN=VSS	OSC1	-1.0			
Output High level voltage		VOH (1)	IOH=-50 μA VDD=4.0 to 6.0V	Ports with the pull-up resistor specifications	VDD-1.2			V
		VOH (2)	IOH=-10 μA	Ports with the pull-up resistor specifications	VDD-0.5			
Output Low level voltage		VOL(1)	IOL=10 mA VDD=4.0 to 6.0 V	Port			1.5	
		VOL(2)	IOL=1 mA, IOL of each Port : 1 mA or less	Port			0.5	
Schmitt characteristics	Hysteresis Voltage	VHIS		$\overline{RES}$, $\overline{INT}$, $\overline{SCK}$, SI, and schmitt specification		0.1VDD		
	High level threshold voltage	VtH		OSC1 (Note 5)	0.4VDD		0.8VDD	
	Low level threshold voltage	VtL			0.2VDD		0.6VDD	
Current consumption Two-pin RC oscillator		IDDOP (1)	• Output N-channel transistors are off when operating • Port = VDD • Fig. 2, fosc=800 kHz (typical)	VDD		3.0	6	mA
Ceramic oscillator		IDDOP (2)	• Fig. 3, 4 MHz, no divider	VDD		4.0	10	
		IDDOP (3)	• Fig. 3, 4 MHz, divide-by-three circuit	VDD		3.0	8	
		IDDOP (4)	• Fig. 3, 4 MHz, divide-by-four circuit	VDD		3.0	6	
		IDDOP (5)	• Fig. 3, 400 kHz	VDD		2.0	5	
		IDDOP (6)	• Fig. 3, 800 kHz	VDD		3.0	6	
External clock		IDDOP (7)	• 384 kHz to 4330 kHz, no divider	VDD		4.0	10	
		IDDOP (8)	• 1152 kHz to 4330 kHz, divide-by-three circuit • 1536 kHz to 4330 kHz, divide-by-four circuit	VDD		3.0	8	
Standby mode		IDDst	Output N-channel, VDD=6V transistor off	VDD		0.05	10	μA
			Ports=VDD VDD=2.5V	VDD		0.025	5	

Parameter	Symbol	Conditions	Pin	Ratings			unit
				min.	typ.	max.	
Oscillation characteristics Ceramic resonator Frequency	fCFOSC (Note 7)	• Fig. 3 fo=400kHz • Fig. 3 fo=800kHz • Fig. 3 fo=1MHz • Fig. 3 fo=4MHz, with no divider, divide-by-three, or divide-by-four circuit	OSC1,OSC2 OSC1,OSC2 OSC1,OSC2 OSC1,OSC2	392 784 980 3920	400 800 1000 4000	408 816 1020 4080	kHz
Oscillation stabilizing time (Note 8)	tCFS	• Fig. 4 fo=400kHz • Fig. 4 fo=800kHz, 1MHz, or 4MHz, with no divider, divide-by-three, or divide-by-four circuit				10 10	ms
Two-pin RC oscillator frequency	fMOSC	• Fig. 2 Cext=270pF±5% • Fig. 2 Rext=5.6kΩ±1%	OSC1, OSC2	587	800	1298	kHz
Pull-up resistance $\overline{RES}$	Ru	VIN=VSS VDD=5V	$\overline{RES}$	200	500	800	kΩ
External reset characteristics Reset time	tRST				See Fig.5		
Pin capacitance	Cp	f=1MHz, Pins except for tested pins, VIN=VSS			10		pF
Serial clock Input clock Cycle time	tCKCY(1)	Fig. 6	$\overline{SCK}$	2.0			µs
Output clock Cycle time	tCKCY(2)	Fig. 6	$\overline{SCK}$		64×tCYC (Note 9)		
Input clock low level pulse width	tCKL(1)	Fig. 6	$\overline{SCK}$	0.6			
Output clock low level pulse width	tCKL(2)	Fig. 6	$\overline{SCK}$		32×tCYC		
Input clock high level pulse width	tCKH(1)	Fig. 6	$\overline{SCK}$	0.6			
Output clock high level pulse width	tCKH(2)	Fig. 6	$\overline{SCK}$		32×tCYC		
Serial input Data setup time	tICK	Specified for the rising edge of $\overline{SCK}$ Fig. 6	SI	0.2			
Data hold time	tCKI		SI	0.2			
Serial output Output delay time	tCKO	• Specified for the falling edge of $\overline{SCK}$ • Select only Nch OD option, and add external 1kΩ resistor and external 50pF capacitor. • Fig. 6	SO			0.4	

Parameter		Symbol	Conditions	VDD[V]	Applicable pins and notes	Ratings min.	Ratings typ.	Ratings max.	unit
Pulse output Period		tPCY	• Fig.7		PE0		64×TCYC		μs
High level pulse width		tPH	• TCYC=4 × system clock		PE0		32×TCYC ±10%		
Low level pulse width		tPL	• Select only Nch OD option, and add external 1kΩ resistor and external 50pF capacitor.		PE0		32×TCYC ±10%		
A/D converter characteristics	Resolution			3 to 5.5				8	bit
	Absolute precision		AV$_+$=VDD AV$_-$=VSS				±1	±2	LSB
	Conversion time	TCAD	When AD speed is 1/1=26*TCYC			24 (TCYC= 0.92μs)		260 (TCYC= 10μs)	μs
			When AD speed is 1/2=51*TCYC			47 (TCYC= 0.92μs)		510 (TCYC= 10μs)	
	Analog input voltage range	VAIN			AD0 to AD7	VSS		VDD	V
	Analog port input current	IAIN	Including the output off leakage current. VAIN=VDD		AD0 to AD7 (The shared I/O function ports have open-drain specification)			1	μA
			VAIN=VSS			-1			
Watch dog timer	Recommended constants (Note 10)	Cw	When PE1 is using open-drain	3 to 5.5	WDR		0.1±5%		μF
		Rw	When PE1 is using open-drain		WDR		680±1%		kΩ
		Rl	When PE1 is using open-drain		WDR		100±1%		Ω
	Clear time (discharge)	tWCT	Fig.8		WDR	100			μs
	Clear period (charge)	tWCCY	Fig.8		WDR	36			ms
	Recommended constants (Note 10)	Cw	When PE1 is using open-drain	3 to 5.5	WDR		0.01±5%		μF
		Rw	When PE1 is using open-drain		WDR		680±1%		kΩ
		Rl	When PE1 is using open-drain		WDR		100±1%		Ω
	Clear time (discharge)	tWCT	Fig.8		WDR	10			μs
	Clear period (charge)	tWCCY	Fig.8		WDR	4.2			ms

Notes:

(1) When oscillated internally under the oscillating conditions in Fig.3, generated voltage can be over the maximum limit of the VDD.

(2) Average for 100 ms period.

(3) Operating supply voltage VDD must be held until the microcontroller enters in the standby mode after the execution of the HALT instruction. Any chattering should not be generated at the PA3 pin during the HALT instruction execution cycle.

(4) Recommended circuit constants that are verified by the oscillator manufacturer, using oscillator characteristic evaluation board selected by SANYO.

(5) The OSC1 pin will have schmitt characteristics when external clock oscillator or the two-pin RC oscillator is selected as an oscillation option.

(6) These are the results of testing using the value at each part on the Fig.3 circuit which is recommended by SANYO. These results do not include the current applied to the output transistor, nor the current applied to the transistor with a pull-up resistor on the LSI.

(7) fCFOSC is the frequency when the values in table 1 are used.

(8) This indicates the elapsed time that is required before the oscillation becomes stable after the VDD exceeds the minimum limit of the operation supply voltage.

(9) TCYC=4×system clock period

(10) When used in an environment that may result in condensation, note that a current leakage between PE1 and adjacent pins

or a current leakage at external integration circuit using R and C could occur.

OSC1   (OSC2)

External Clock   OPEN
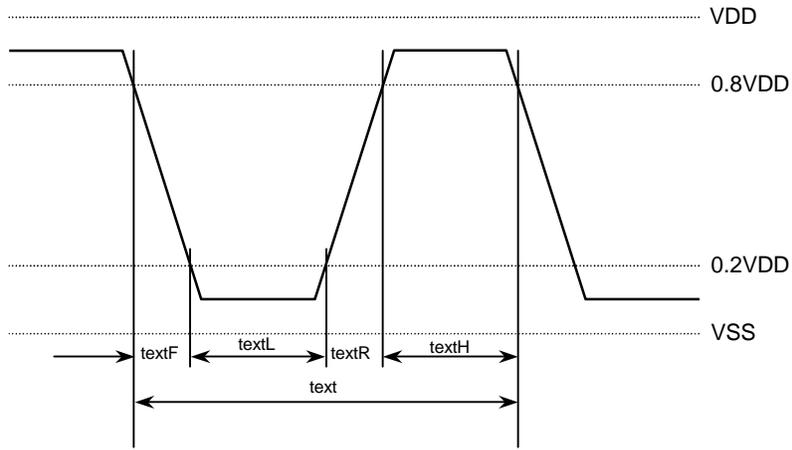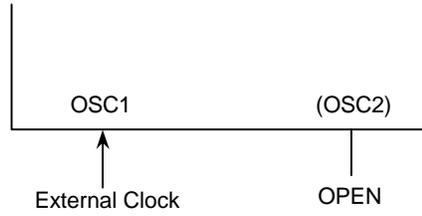
Figure 1 External Clock Input Waveform
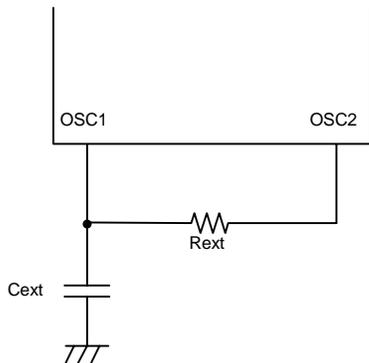
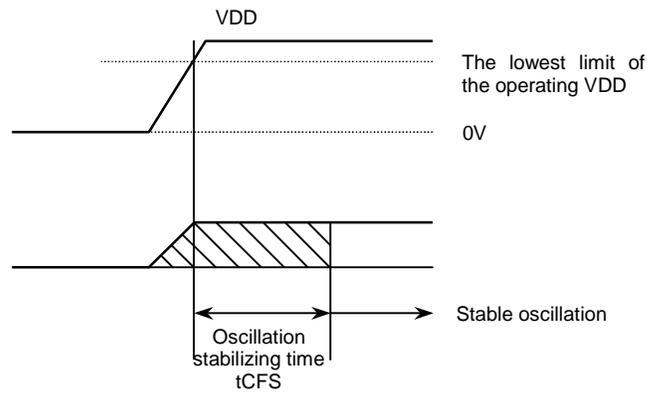Figure 2 Two-pin RC Oscillator Circuit   Figure 3 Ceramic Resonator Circuit
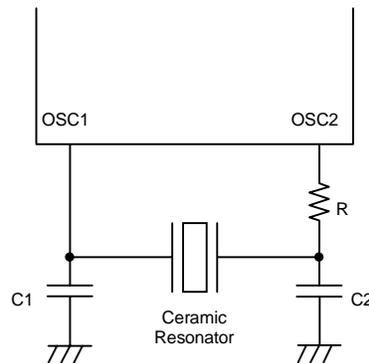
Figure 4 Oscillation Stabilizing Time

Table 1 Recommended Ceramic Resonator constants
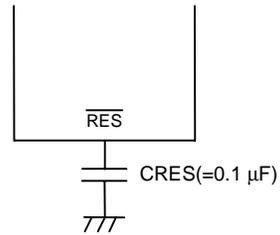
Data will be added once evaluation has been completed.

Figure 5 Reset Circuit

(Note) If measured from the instant the voltage level reaches the lowest limit of the operating VDD (i.e. not including the rising time), the reset time when CRES=0.1 μF is used should be between 10 ms to 100 ms.
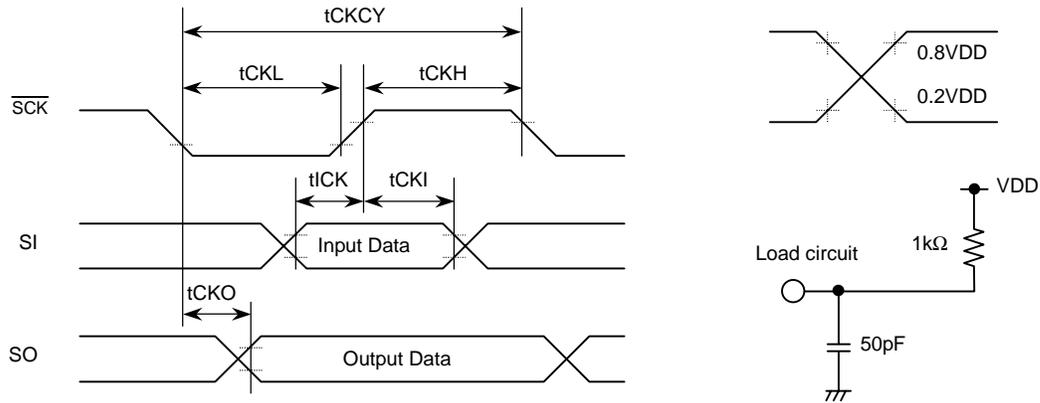
Figure 6 Serial I/O Timing

Figure 7 Port PE0 Pulse Output Timing
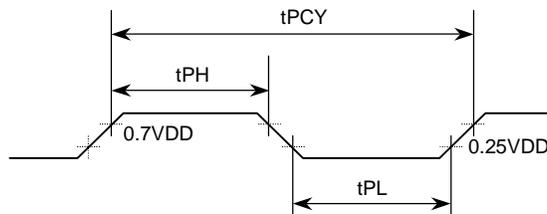
The load conditions are the same as those in Figure 5.
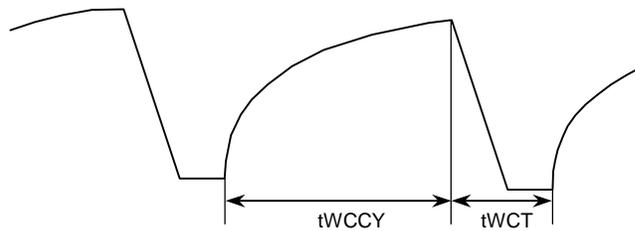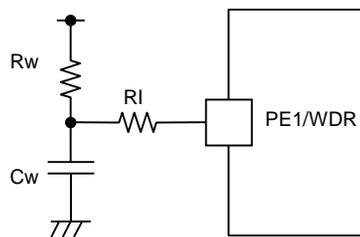
tWCCY : Charge time made by the external Cw, Rw, and Rl time constants
tWCT   : Discharge time made by program control

Figure 8 Watchdog Timer Waveform

RC Oscillator Characteristic of LC65F1306A

Data will be added once evaluation has been completed.

Notes on Circuit Board Design

This section provides hints and countermeasure for noise problem in terms of microcontroller when designing circuit boards using these microcontrollers for a mass production. These design techniques are effective to prevent and avoid the defects (e.g. malfunctions of the microcontroller or a runaway program) caused by noise.

1. VDD, VSS : Power Supply Pins

Add capacitors between the VDD and VSS pins so that they meet the following conditions.
- The length of the line from the VDD to the two capacitors and the length of the line from the VSS to the two capacitors should be as equal as possible (L1=L1', L2=L2'), and should be as short as possible.
- Add the larger capacitor to 'C1' position and smaller capacitor to 'C2' position.

The VDD and VSS lines on the circuit board should be thicker than any other lines.
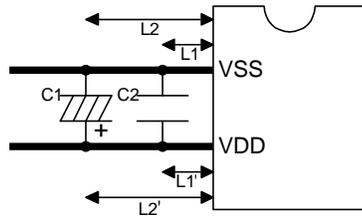
2. OSC1, OSC2 : Clock I/O Pins
- When the ceramic resonator option is selected : (Figure 2-1)
  - The length of the lines (Losc in Fig.2-1) between the clock I/O pins (input: OSC1, output: OSC2) and the external components should be as short as possible.
  - The length of the lines (Lvss+L1 or L2) between each capacitor and the VSS pin should be as short as possible.
  - The VSS line for the oscillation circuit and the VSS line for other functions should be branched as close as possible to the microcontroller's VSS pin.
  - Oscillation constants written in this specification sheet (such as the capacitor C1, C2 and the damping resistor Rd) may have to be changed and the frequency should be adjusted, depending on the pattern capacity of the circuit board. In this case, contact the oscillator manufacturer about it.
- When two-pin RC oscillator option is selected: (Figure 2-2)
  - The length of the lines (Losc) between the clock I/O pins (input: OSC1, output: OSC2) and the external components (capacitor Cext, resistor Rext) should be as short as possible.
  - The length of the line (Lvss+Lc) between the capacitor and the VSS pin should be as short as possible.
  - The VSS line for the oscillation circuit and the VSS line for other functions should be branched as close as possible to the microcontroller's VSS pin.
- When the external oscillation option is selected: (Figure 2-3)
  - The length of the line (Losc) between the clock input pin (OSC1) and the external oscillator should be as short as possible.
  - The clock output pin (OSC2) should be opened.
  - The length of the line between the VSS and the external oscillator, and the length of the line between the VDD and the external oscillator should be as short as possible.
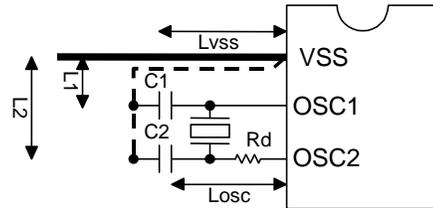
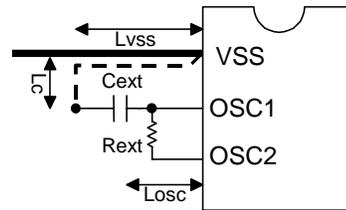Figure 2-1. Sample Oscillation Circuit 1
(Ceramic resonator)

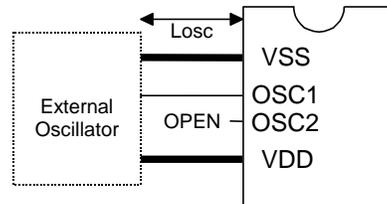Figure 2-2. Sample Oscillation Circuit 2
(Two-pin RC Oscillator)

Figure 2-3. Sample Oscillation Circuit 3
(External Oscillator)

• Other note on all oscillator circuit:

   • Place the lines for signals that can easily change suddenly, high amplitude signals connected to the higher capacity voltage (+15 V) ports, and powerful current supplies as far as possible from the oscillation circuit, and do not cross these lines with lines concerned to the clock.

3. $\overline{\text{RES}}$: Reset Pin

   • The length of line (Lres) between the $\overline{\text{RES}}$ pin and the external circuit should be as short as possible.

   • The length of lines (L1 and L2) between the $\overline{\text{RES}}$ pin and the capacitor (Cres), and the VSS and the capacitor should be as short as possible.
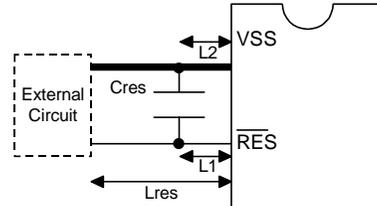
Figure 3. $\overline{\text{RES}}$ Pin Patterns

4. TEST : Test Pin

   • The length of line (L) between the VSS and the TEST pin should be as short as possible.

   • The TEST pin and the VSS pin should be connected as close as possible to the VSS pin.
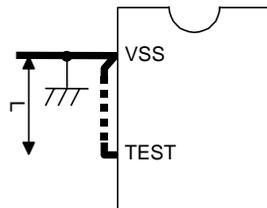
Figure 4. Test Pin Patterns

5. AD0 to AD7 : Analog Input Pins

The connection for the analog input pins, such as A/D converter input pins and comparator input pin, should meet the following conditions.

   • The length of the line (L1) between the damping resistor (R1) and each analog pins should be as short as possible.

   • The capacitor added between each analog pins and AV- pin (base voltage input pin for A/D converter) should be located as close as possible to the AV- input pin.
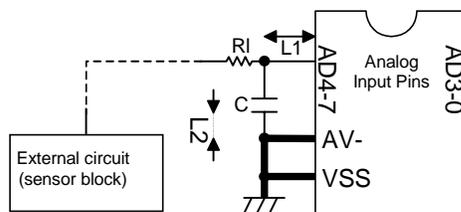
Figure 5. Analog Input Pins Patterns

6. I/O Pins

All I/O pins on these microcontrollers have function of both input and output.

   • When used as an input pin, add a damping resistor and keep the length of the line to that pin as short as possible.

[Supplement]

In addition to the techniques for designing a circuit board, the following options and programming are effective to prevent and avoid the defects (the malfunction or a runaway program).

- If signals are input from external sources when the microcontroller power supply is unstable, select the higher capacity voltage (N-channel open drain) output type for the input pin, and add a damping resistor close to the pin.
- When the external signals are input to pins, the chattering of the key must be removed.
- The data should be output periodically from the pins using the output instruction (OP or SPB).
- To read the data input to the I/O common pins, the output value should be set to '1' using the output instruction (OP or SPB).

7. Unused Pins

- See the user's manual for each microcontrollers or the final edition of the specification sheet.