

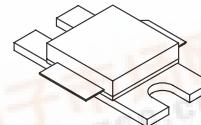
The RF MOSFET Line**RF Power Field Effect Transistors****N-Channel Enhancement-Mode Lateral MOSFETs**

Designed for class AB PCN and PCS base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications.

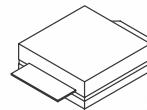
- CDMA Performance @ 1990 MHz, 26 Volts
IS-97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Thru 13
885 kHz — -47 dBc @ 30 kHz BW
1.25 MHz — -55 dBc @ 12.5 kHz BW
2.25 MHz — -55 dBc @ 1 MHz BW
Output Power — 4.5 Watts Avg.
Power Gain — 13.5 dB
Efficiency — 17%
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1.93 GHz, 30 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.

MRF19030R3
MRF19030SR3

2.0 GHz, 30 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465E-03, STYLE 1
NI-400
MRF19030R3



CASE 465F-03, STYLE 1
NI-400S
MRF19030SR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	65	Vdc
Gate-Source Voltage	V _{GS}	-0.5, +15	Vdc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	83.3 0.48	Watts W/°C
Storage Temperature Range	T _{stg}	-65 to +200	°C
Operating Junction Temperature	T _J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	2.1	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage ($V_{GS} = 0 \text{ Vdc}$, $I_D = 20 \mu\text{A}$)	$V_{(\text{BR})\text{DSS}}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 28 \text{ Vdc}$, $V_{GS} = 0 \text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current ($V_{GS} = 5 \text{ Vdc}$, $V_{DS} = 0 \text{ Vdc}$)	I_{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage ($V_{DS} = 10 \text{ Vdc}$, $I_D = 100 \mu\text{Adc}$)	$V_{GS(\text{th})}$	2	3	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 28 \text{ Vdc}$, $I_D = 300 \text{ mA}$)	$V_{GS(\text{Q})}$	2	3.3	4.5	Vdc
Drain–Source On–Voltage ($V_{GS} = 10 \text{ Vdc}$, $I_D = 1 \text{ Adc}$)	$V_{DS(\text{on})}$	—	0.29	0.4	Vdc
Forward Transconductance ($V_{DS} = 10 \text{ Vdc}$, $I_D = 1 \text{ Adc}$)	g_{fs}	—	2	—	S

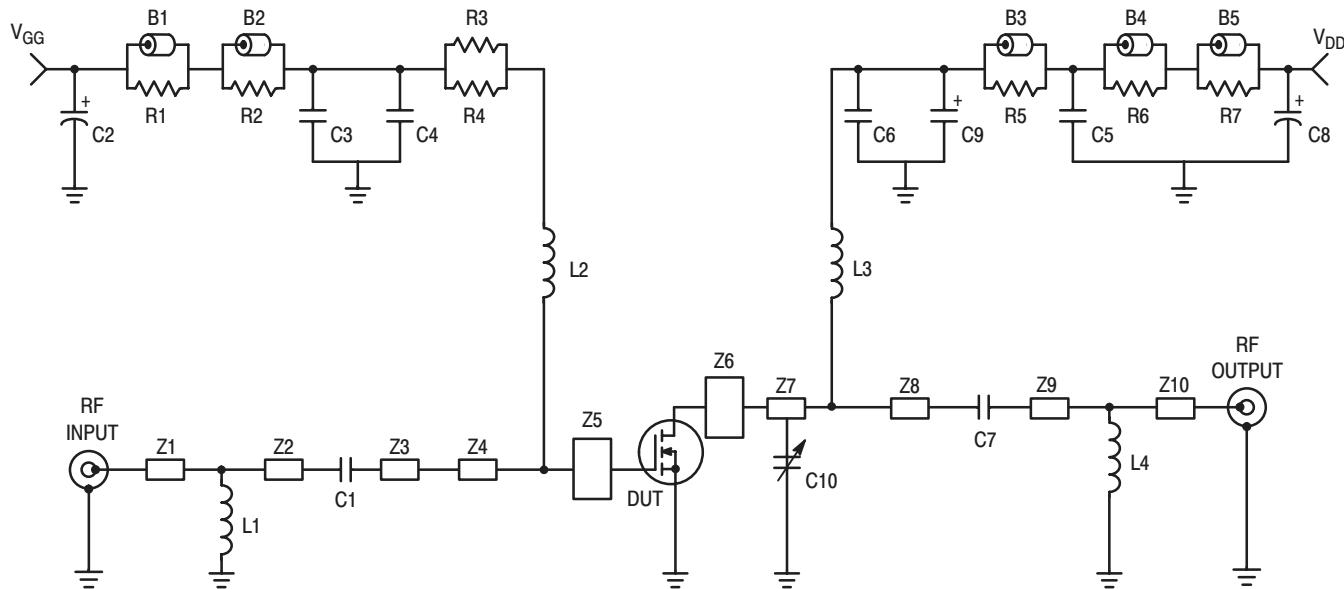
DYNAMIC CHARACTERISTICS

Input Capacitance (Including Input Matching Capacitor in Package) (1) ($V_{DS} = 26 \text{ Vdc}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$)	C_{iss}	—	98.5	—	pF
Output Capacitance (1) ($V_{DS} = 26 \text{ Vdc}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$)	C_{oss}	—	37	—	pF
Reverse Transfer Capacitance ($V_{DS} = 26 \text{ Vdc}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$)	C_{rss}	—	1.3	—	pF

FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)

Two-Tone Common–Source Amplifier Power Gain ($V_{DD} = 26 \text{ Vdc}$, $P_{\text{out}} = 30 \text{ W PEP}$, $I_{DQ} = 300 \text{ mA}$, $f_1 = 1960.0 \text{ MHz}$, $f_2 = 1960.1 \text{ MHz}$)	G _{ps}	—	13	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26 \text{ Vdc}$, $P_{\text{out}} = 30 \text{ W PEP}$, $I_{DQ} = 300 \text{ mA}$, $f_1 = 1960.0 \text{ MHz}$, $f_2 = 1960.1 \text{ MHz}$)	η	—	36	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26 \text{ Vdc}$, $P_{\text{out}} = 30 \text{ W PEP}$, $I_{DQ} = 300 \text{ mA}$, $f_1 = 1960.0 \text{ MHz}$, $f_2 = 1960.1 \text{ MHz}$)	IMD	—	-31	—	dBc
Input Return Loss ($V_{DD} = 26 \text{ Vdc}$, $P_{\text{out}} = 30 \text{ W PEP}$, $I_{DQ} = 300 \text{ mA}$, $f_1 = 1960.0 \text{ MHz}$, $f_2 = 1960.1 \text{ MHz}$)	IRL	—	-13	—	dB
Two-Tone Common–Source Amplifier Power Gain ($V_{DD} = 26 \text{ Vdc}$, $P_{\text{out}} = 30 \text{ W PEP}$, $I_{DQ} = 300 \text{ mA}$, $f_1 = 1930.0 \text{ MHz}$, $f_2 = 1930.1 \text{ MHz}$ and $f_1 = 1990.0 \text{ MHz}$, $f_2 = 1990.1 \text{ MHz}$)	G _{ps}	12	13	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26 \text{ Vdc}$, $P_{\text{out}} = 30 \text{ W PEP}$, $I_{DQ} = 300 \text{ mA}$, $f_1 = 1930.0 \text{ MHz}$, $f_2 = 1930.1 \text{ MHz}$ and $f_1 = 1990.0 \text{ MHz}$, $f_2 = 1990.1 \text{ MHz}$)	η	33	36	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26 \text{ Vdc}$, $P_{\text{out}} = 30 \text{ W PEP}$, $I_{DQ} = 300 \text{ mA}$, $f_1 = 1930.0 \text{ MHz}$, $f_2 = 1930.1 \text{ MHz}$ and $f_1 = 1990.0 \text{ MHz}$, $f_2 = 1990.1 \text{ MHz}$)	IMD	—	-31	-28	dBc
Input Return Loss ($V_{DD} = 26 \text{ Vdc}$, $P_{\text{out}} = 30 \text{ W PEP}$, $I_{DQ} = 300 \text{ mA}$, $f_1 = 1930.0 \text{ MHz}$, $f_2 = 1930.1 \text{ MHz}$ and $f_1 = 1990.0 \text{ MHz}$, $f_2 = 1990.1 \text{ MHz}$)	IRL	—	-13	-9	dB
Output Mismatch Stress ($V_{DD} = 26 \text{ Vdc}$, $P_{\text{out}} = 30 \text{ W CW}$, $I_{DQ} = 300 \text{ mA}$, $f = 1930 \text{ MHz}$, $\text{VSWR} = 10:1$, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B1 – B5
 C1, C7
 C2, C8
 C3, C5
 C4, C6
 C9
 C10
 L1 – L4
 R1 – R7
 Z1
 Z2

Short Ferrite Beads
 10 pF Chip Capacitors, B Case
 470 μ F, 35 V Electrolytic Capacitors
 0.1 μ F Chip Capacitors, B Case
 5.1 pF Chip Capacitors, B Case
 22 μ F Tantalum Chip Capacitor
 0.4 – 2.5 pF Variable Capacitor, Johanson Gigatrim
 12.5 nH Inductors
 12 Ω Chip Resistors (0805)
 0.080" x 0.595" Microstrip
 0.080" x 0.600" Microstrip

Z3
 Z4
 Z5
 Z6
 Z7
 Z8
 Z9
 Z10
 Substrate

0.080" x 0.480" Microstrip
 0.325" x 0.280" Microstrip
 0.510" x 0.200" Microstrip
 0.510" x 0.200" Microstrip
 0.325" x 0.280" Microstrip
 0.080" x 0.480" Microstrip
 0.080" x 0.530" Microstrip
 0.080" x 0.671" Microstrip
 0.030" x 3.00" x 5.00" Glass Teflon[®], Arlon

Figure 1. MRF19030 Test Circuit Schematic

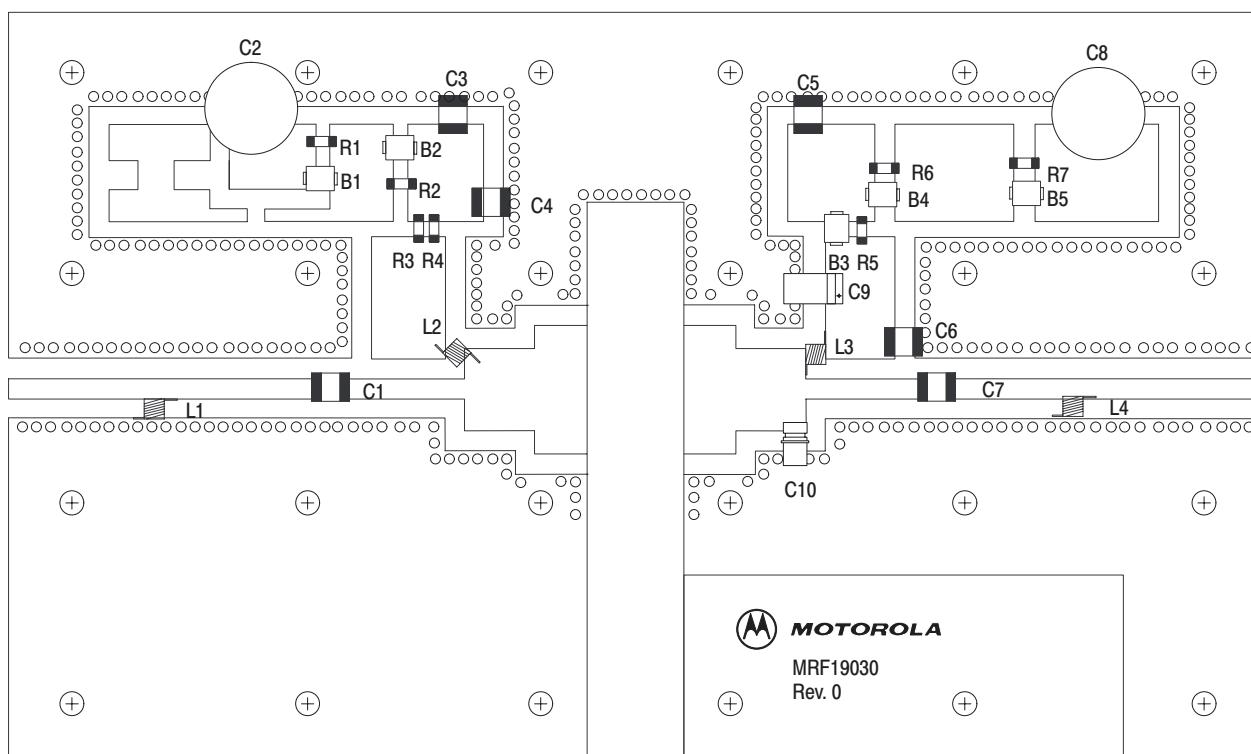
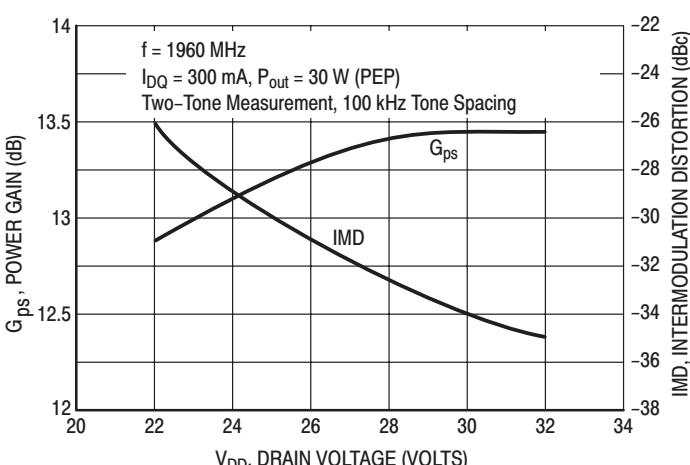
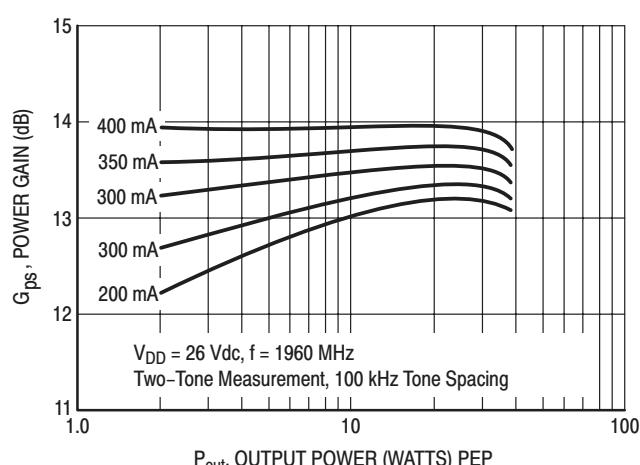
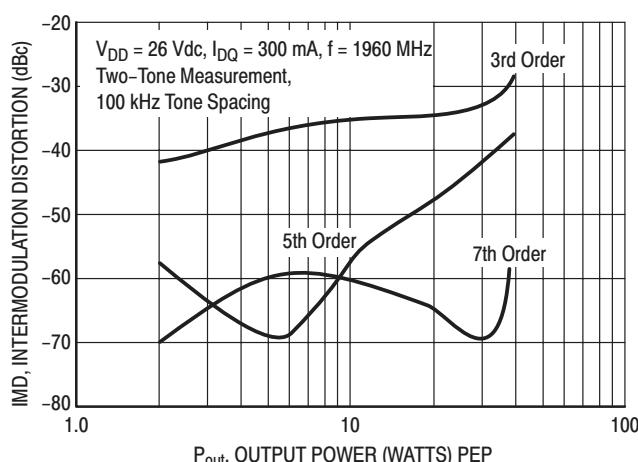
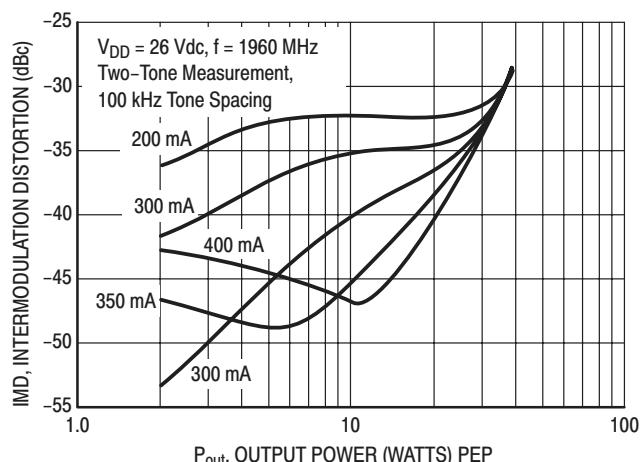
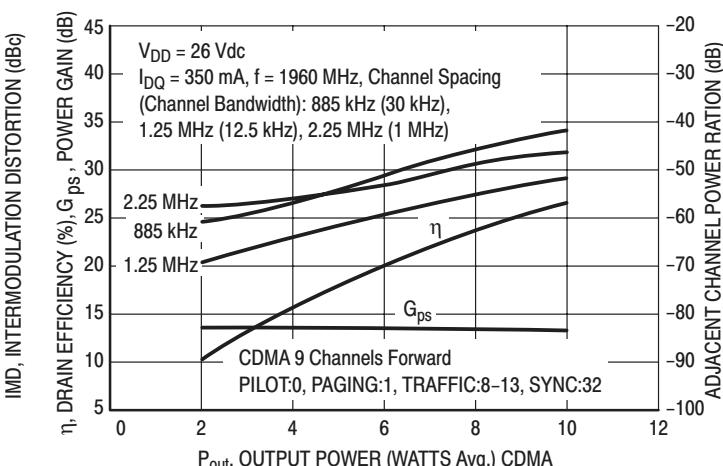
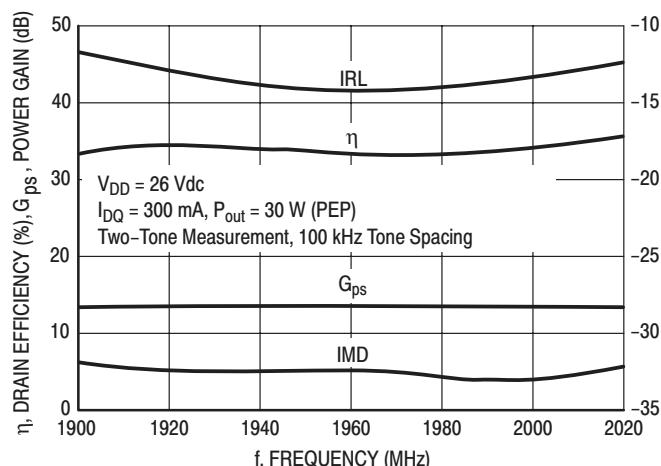
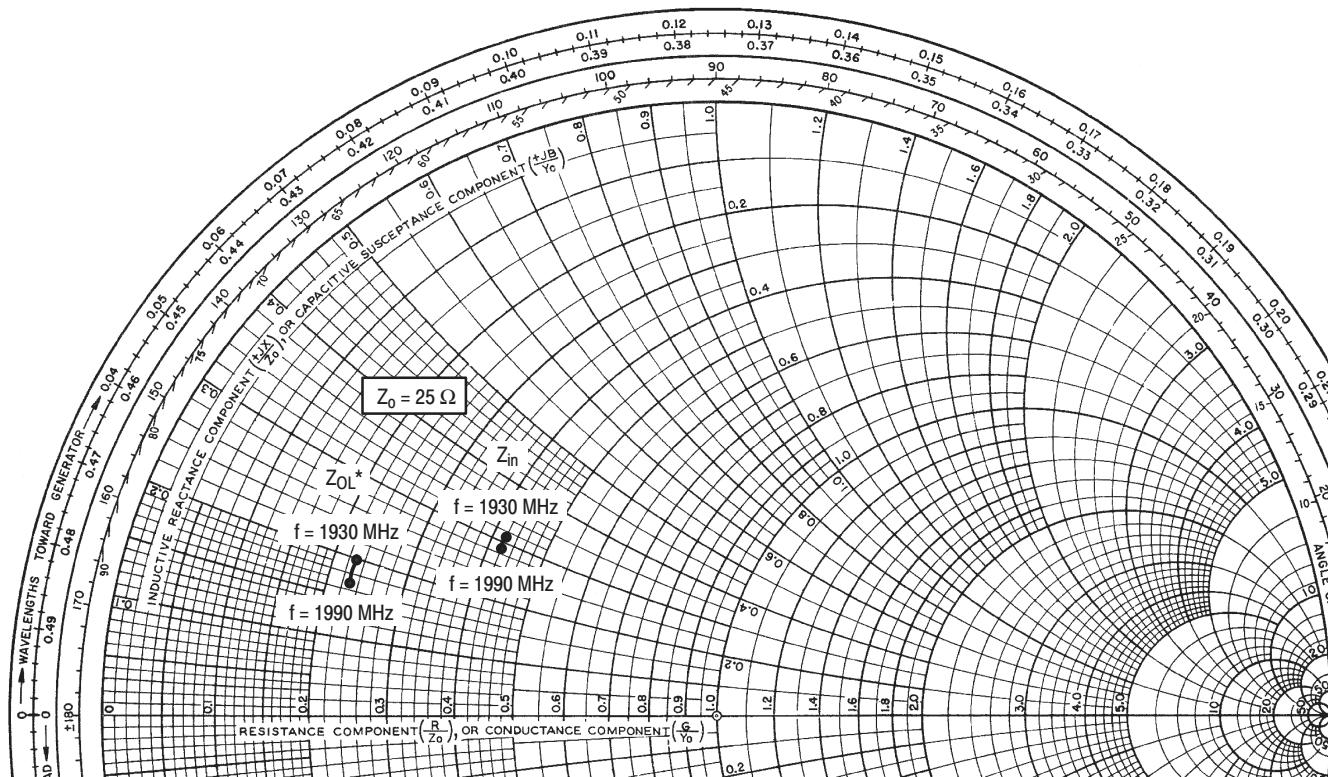


Figure 2. MRF19030 Test Circuit Component Layout

TYPICAL CHARACTERISTICS





$V_{DD} = 26 \text{ V}$, $I_{DQ} = 300 \text{ mA}$, $P_{out} = 30 \text{ W PEP}$

f MHz	Z_{in} Ω	Z_{OL^*} Ω
1930	$10.57 + j7.69$	$5.81 + j5.01$
1960	$10.54 + j7.43$	$5.84 + j4.67$
1990	$10.47 + j7.21$	$5.84 + j4.35$

Z_{in} = Complex conjugate of source impedance.

Z_{OL^*} = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL^*} was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

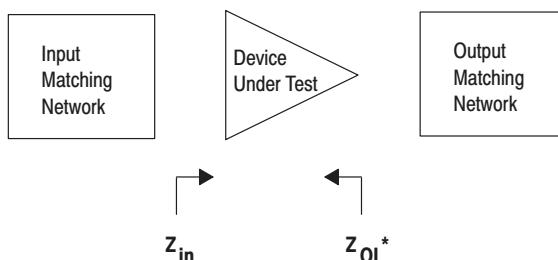
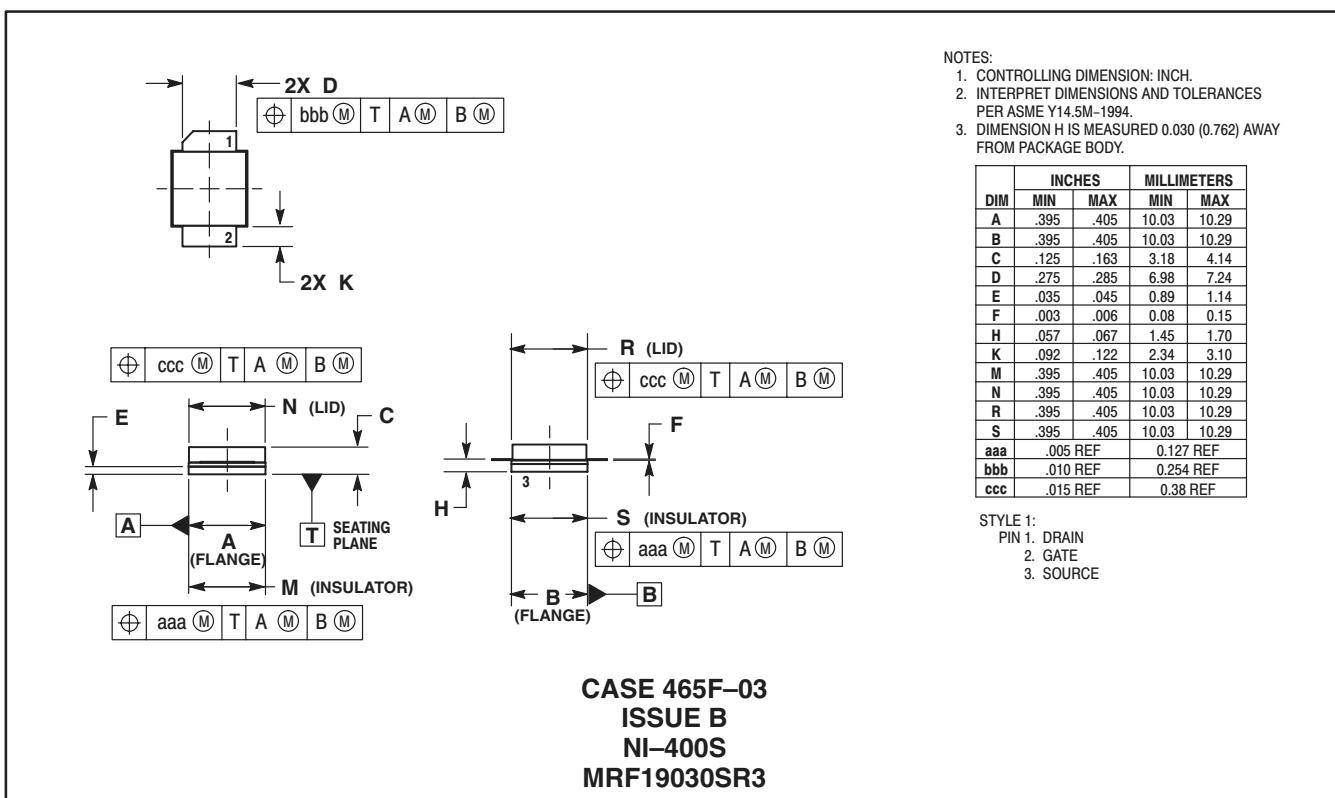
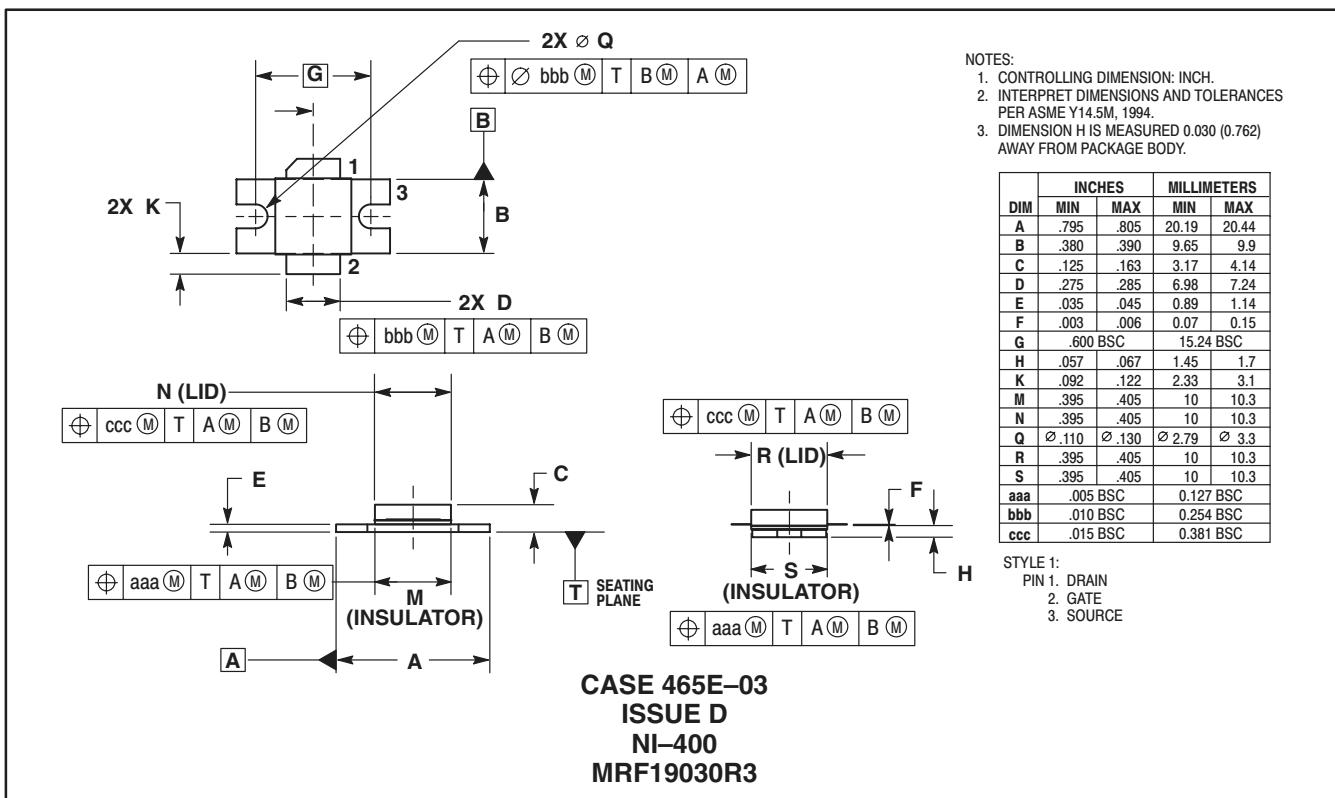


Figure 9. Series Equivalent Input and Output Impedance

NOTES

PACKAGE DIMENSIONS



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How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 1-303-675-2140 or 1-800-441-2447

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3-20-1, Minami-Azabu. Minato-ku, Tokyo 106-8573 Japan. 81-3-3440-3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852-26668334

Technical Information Center: 1-800-521-6274

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