

**FAIRCHILD**  
SEMICONDUCTOR™

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## 74F269 8-Bit Bidirectional Binary Counter

### General Description

The 74F269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

### Features

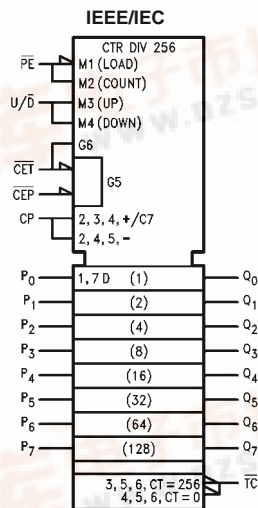
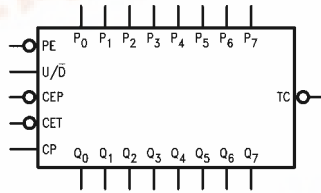
- Synchronous counting and loading
- Built-in lookahead carry capability
- Count frequency 100 MHz
- Supply current 113 mA typ
- 300 mil slimline package

### Ordering Code:

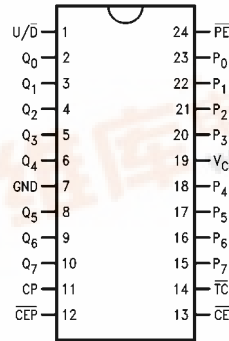
Order Number	Package Number	Package Description
74F269SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F269SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



### Function Table

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$\overline{U/D}$	CP	Function
L	X	X	X	↗	Parallel Load All Flip-Flops
H	H	X	X	↗	Hold
H	X	H	X	↗	Hold ( $\overline{TC}$ Held HIGH)
H	L	L	H	↗	Count Up
H	L	L	L	↗	Count Down

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
↗ = Transition LOW-to-HIGH

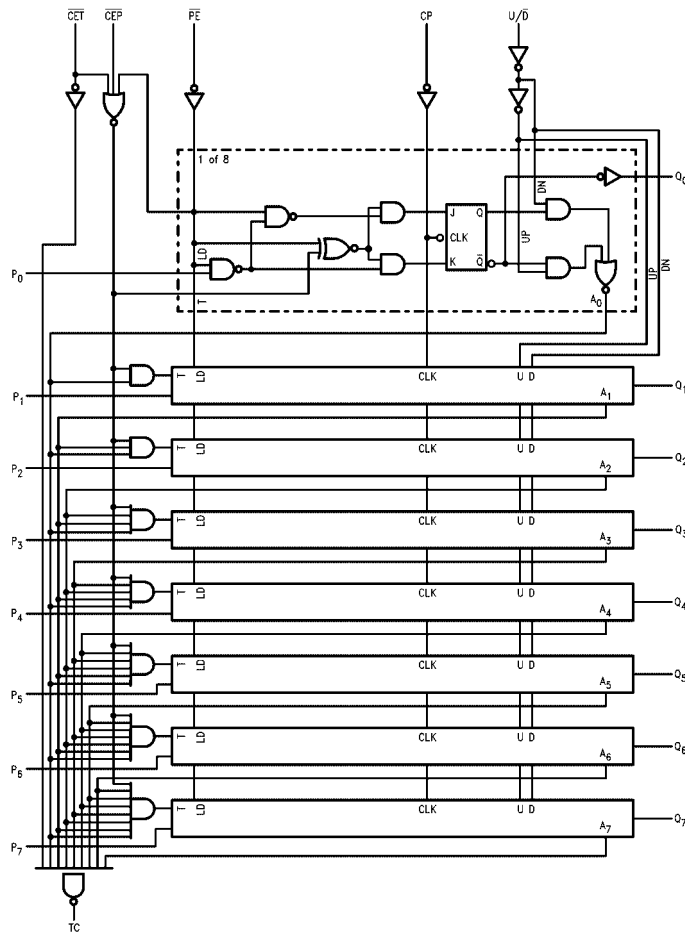
74F269 8-Bit Bidirectional Binary Counter



### Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
P <sub>0</sub> –P <sub>7</sub>	Parallel Data Inputs	1.0/1.0	20 $\mu$ A/–0.6 mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/–0.6 mA
U/ $\overline{D}$	Up-Down Count Control Input	1.0/1.0	20 $\mu$ A/–0.6 mA
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	1.0/1.0	20 $\mu$ A/–0.6 mA
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	1.0/1.0	20 $\mu$ A/–0.6 mA
CP	Clock Input	1.0/1.0	20 $\mu$ A/–0.6 mA
$\overline{TC}$	Terminal Count Output (Active LOW)	5.0/33.3	–1 mA/20 mA
Q <sub>0</sub> –Q <sub>7</sub>	Flip-Flop Outputs	50/33.3	–1 mA/20 mA

### Logic Diagram



**Absolute Maximum Ratings**(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

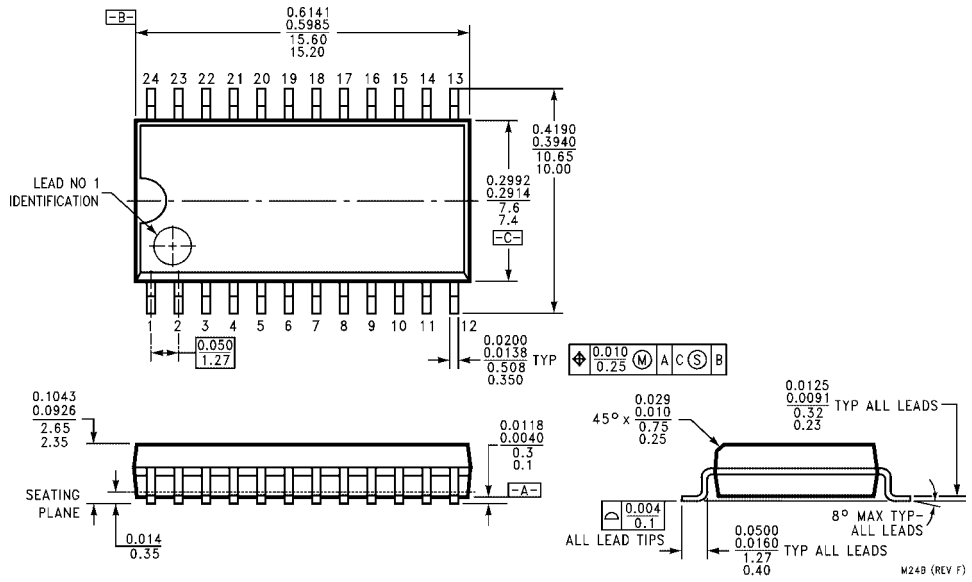
Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub> 5% V <sub>CC</sub>	2.5 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA, All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		104	125	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		113	135	mA	Max	V <sub>O</sub> = LOW

AC Electrical Characteristics							
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	
$f_{MAX}$	Maximum Clock Frequency	100			85		MHz
$t_{PLH}$	Propagation Delay	3.5		8.0	3.5	7.0	ns
$t_{PHL}$	CP to $Q_n$ (Count-Up)	4.5		10.5	4.5	11.0	
$t_{PLH}$	Propagation Delay	3.5		7.5	3.5	10.0	ns
$t_{PHL}$	$U/\bar{D}$ to TC	4.5		7.5	4.5	11.0	
$t_{PLH}$	Propagation Delay	3.5		7.0	3.5	10.5	ns
$t_{PHL}$	$\overline{CET}$ to $\overline{TC}$	3.0		10.5	3.0	11.5	
$t_{PLH}$	Propagation Delay	4.5		10.0	4.5	10.5	ns
$t_{PHL}$	CP to $\overline{TC}$	5.0		10.0	4.5	10.5	
$t_{PLH}$	Propagation Delay	3.5		10.5	3.5	11.0	ns
$t_{PHL}$	CP to $Q_n$ (Count-Down)	4.5		10.5	4.5	11.0	
$t_{PLH}$	Propagation Delay	3.5		7.0	3.5	10.0	ns
$t_{PHL}$	CP to $Q_n$ (Load)	4.0		7.0	4.0	7.0	

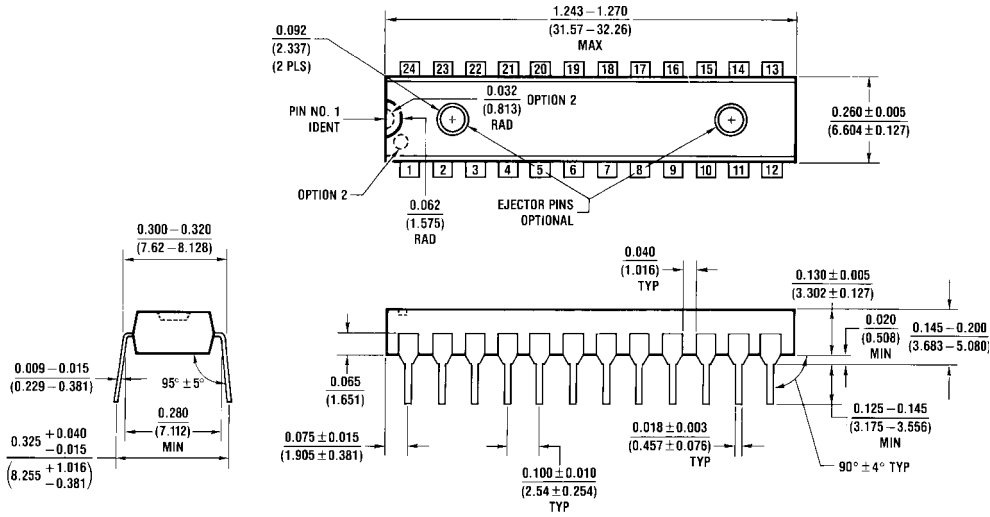
AC Operating Requirements						
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		Units
		Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	3.5		4.0		ns
$t_S(L)$	Data to CP	3.0		3.0		
$t_H(H)$	Hold Time, HIGH or LOW	1.0		2.0		ns
$t_H(L)$	Data to CP	1.0		1.0		
$t_S(H)$	Setup Time, HIGH or LOW	5.5		6.5		ns
$t_S(L)$	$\overline{PE}$ to CP	5.5		6.5		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		ns
$t_H(L)$	$\overline{PE}$ to CP	0		0		
$t_S(H)$	Setup Time, HIGH or LOW	6.0		6.5		ns
$t_S(L)$	$\overline{CET}$ or $\overline{CEP}$ to CP	8.0		9.0		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		ns
$t_H(L)$	$\overline{CET}$ or $\overline{CEP}$ to CP	0		0		
$t_W(H)$	Clock Pulse Width, HIGH or LOW	3.5		3.5		ns
$t_W(L)$		3.5		4.0		
$t_S(H)$	Setup Time, HIGH or LOW	8.0		9.5		ns
$t_S(L)$	$U/\bar{D}$ to CP	6.0		7.0		
$t_H(H)$	Hold Time, HIGH or LOW	0.0		0.0		ns
$t_H(L)$	$U/\bar{D}$ to CP	0.0		0.0		

**Physical Dimensions** inches (millimeters) unless otherwise noted



**28-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide  
Package Number M24B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N24C**

N24C (REV F)

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