MOTOROLA

MC74F269

8-BIT BIDIRECTIONAL BINARY COUNTER

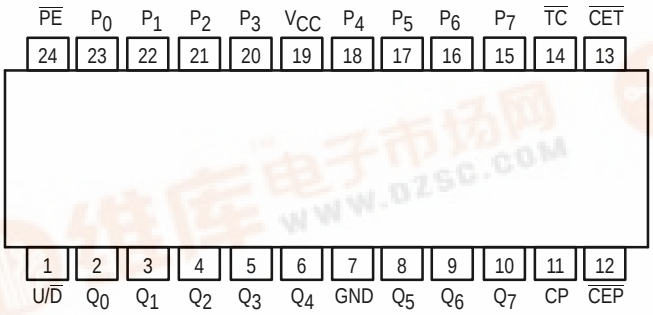
The MC74F269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

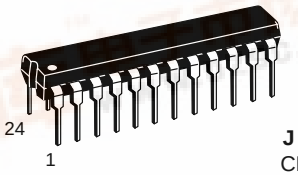
- Synchronous Counting and Loading
- Built-In Lookahead Carry Capability
- Count Frequency 115 MHz Typical
- Supply Current 95 mA Typical

8-BIT BIDIRECTIONAL BINARY COUNTER

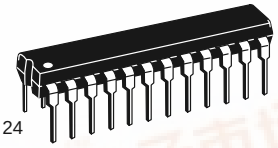
FAST™ SCHOTTKY TTL

PIN ASSIGNMENT

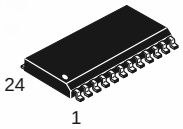




J SUFFIX
CERAMIC
CASE 758-01



N SUFFIX
PLASTIC
CASE 724-03



DW SUFFIX
SOIC
CASE 751E-03

ORDERING INFORMATION

MC74FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXDW	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	74	0	25	70	°C
I_{OH}	Output Current — High	74			–1.0	mA
I_{OL}	Output Current — Low	74			20	mA

FUNCTION TABLE

Operating Mode	Inputs						Outputs	
	CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	P_n	Q_n	$\overline{TC}$
Parallel Load	↑	X	X	X	l	l	L	(a)
	↑	X	X	X	l	h	H	(a)
Count Up	↑	h	l	l	h	X	Count Up	(a)
Count Down	↑	l	l	l	h	X	Count Down	(a)
Hold	↑	X	h	X	h	X	q_n	(a)
Do Nothing	↑	X	X	h	h	X	q_n	H

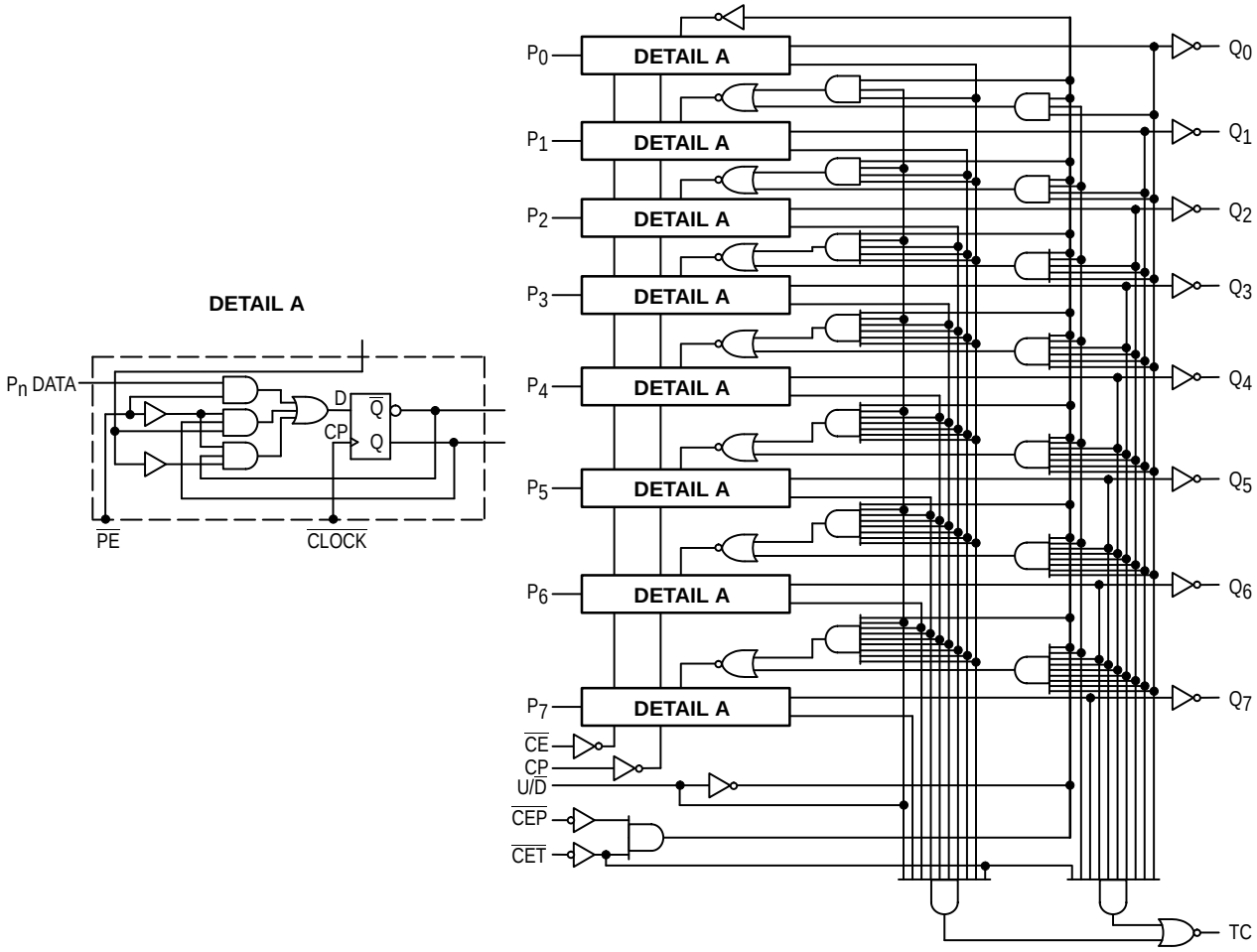
H = HIGH voltage level steady state
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level steady state
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition
↑ = LOW-to-HIGH clock transition
(a) = The TC is LOW when CET is LOW and the counter is at Terminal Count. Terminal Count Up is with all Q_n outputs HIGH and Terminal Count Down is with all Q_n outputs LOW.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{OH}	Output HIGH Voltage	74	2.5			V	I_{OH} = –1.0 mA	V_{CC} = 4.5 V
			2.7	3.4				V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage	74		0.35	0.5	V	I_{OL} = 20 mA, V_{CC} = 4.5 V	
V_{IK}	Input Clamp Diode Voltage				–1.2	V	V_{CC} = MIN, I_{IN} = –18 mA	
I_{IH}	Input HIGH Current				100	μA	V_{CC} = MAX	V_{IN} = 7.0 V
					20			V_{IN} = 2.7 V
I_{IL}	Input LOW Current				–0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		–60		–150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Total Supply Current (total)	I_{CCH}		93	120	mA	V_{CC} = MAX	(Note 3)
		I_{CCL}		98	125			(Note 4)

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.
3. PE = CET = CEP = U/D = GND: P_n = 4.5 V: CP = ↑
4. PE = CET = CEP = U/D = GND: CP = ↑

LOGIC DIAGRAM



AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF			74F $T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0$ V $\pm 10\%$ $C_L = 50$ pF		Unit
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	100			85		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n (Load) $\overline{PE}$ = LOW	3.0 4.0	5.5 5.0	9.0 9.0	3.0 4.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n (Count) $\overline{PE}$ = HIGH	3.0 4.5	6.0 7.0	9.0 10	2.5 4.5	10 10.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	4.5 5.0	7.5 7.5	10 10	4.5 5.0	10.5 11	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.5 3.5	5.0 5.5	9.0 9.0	3.5 3.5	10 10	ns
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	4.0 4.5	6.0 5.5	9.0 9.5	4.0 4.5	10 10	ns

AC SETUP REQUIREMENTS

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF			74F $T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0$ V $\pm 10\%$ $C_L = 50$ pF			Unit
		Min	Typ	Max	Min	Typ	Max	
$t_s(H)$ $t_s(L)$	Set-up Time, HIGH or LOW P to CP	2.0 2.0			2.5 2.5			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P to CP	1.0 1.0			1.0 1.0			ns
$t_s(H)$ $t_s(L)$	Set-up Time, HIGH or LOW $\overline{PE}$ to CP	5.0 5.5			5.5 6.5			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ to CP	0 0			0 0			ns
$t_s(H)$ $t_s(L)$	Set-up Time, HIGH or LOW $\overline{CET}$, $\overline{CEP}$ to CP	4.5 4.5			5.5 5.5			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CET}$, $\overline{CEP}$ to CP	0 0			0 0			ns
$t_s(H)$ $t_s(L)$	Set-up Time, HIGH or LOW U/$\overline{D}$ to CP	6.0 7.0			7.0 8.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW U/$\overline{D}$ to CP	0 0			0 0			ns
$t_w(H)$ $t_w(L)$	Clock Pulse Width CP	4.0 4.5			4.0 5.0			ns

TIMING DIAGRAM