RF2629

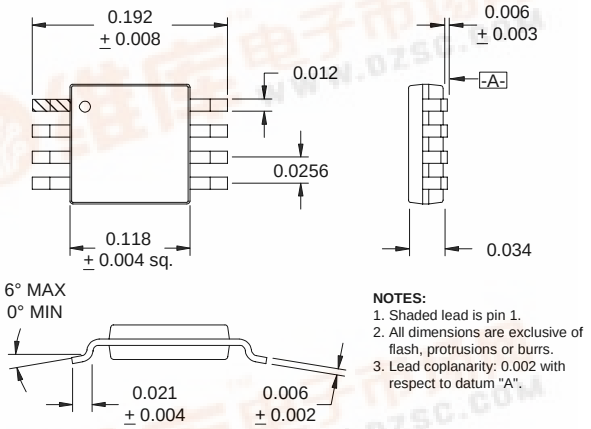
3V CDMA/FM TRANSMIT AGC AMPLIFIER

Typical Applications

- 3V CDMA/FM Cellular Systems
- 3V CDMA PCS Systems
- 3V TDMA Cellular/PCS Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- Portable Battery-Powered Equipment

Product Description

The RF2629 is a complete AGC amplifier designed for the transmit section of 3V dual-mode CDMA/FM cellular and PCS applications. It is designed to amplify IF signals while providing more than 84dB of gain control range. Noise Figure, IP3, and other specifications are designed for CDMA and dual mode CDMA/AMPS handsets. This circuit is designed as part of the RFMD CDMA Chip Set, consisting of this Transmit IF AGC Amp, a Transmit Upconverter, a Receive LNA/Mixer, and a Receive IF AGC Amp. The IC is manufactured on an advanced high frequency Silicon Bipolar process and is packaged in a standard miniature 8-lead plastic MSOP package.



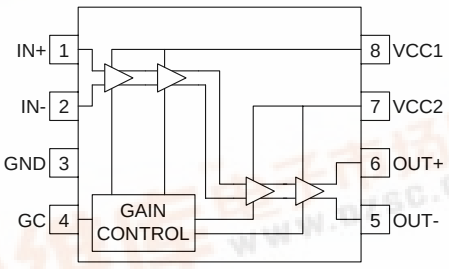
Package Style: MSOP-8

Optimum Technology Matching® Applied

- [x] Si BJT
- [ ] Si Bi-CMOS
- [ ] GaAs HBT
- [ ] SiGe HBT
- [ ] GaAs MESFET
- [ ] Si CMOS

Features

- Supports Dual Mode Operation
- Supports PCS and Cellular Applications
- -48dB to +38dB Gain Control Range
- Single 3V Power Supply
- 12MHz to 175MHz Operation
- Miniature Surface Mount Package



Functional Block Diagram

Ordering Information

RF2629	3V CDMA/FM Transmit AGC Amplifier
RF2629 PCBA	Fully Assembled Evaluation Board

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RF2629

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.0	V_{DC}
Control Voltage	-0.5 to +5.0	V
Input Power Levels	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

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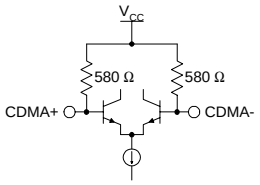
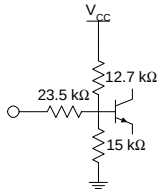
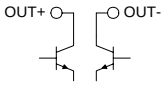
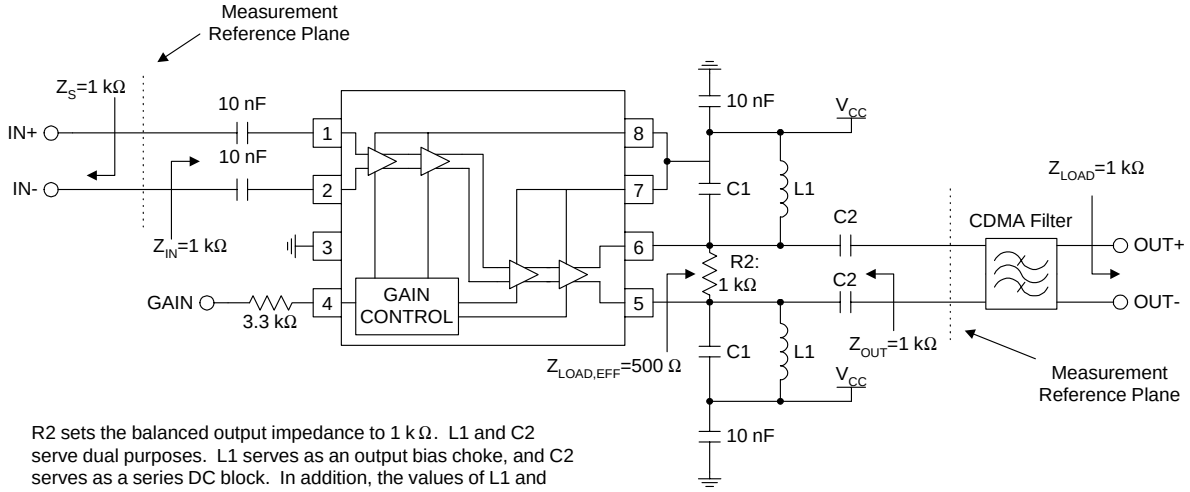
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, 130MHz, V_{CC}=3.0V, Pin=-40dBm, Z_S=1kΩ, Z_L=1kΩ, 1kΩ External Output Terminating Resistor (Effective Z_L=500Ω) (See Application Example)
Frequency Range		12 to 175		MHz	
Maximum Gain	+35	+38		dB	V_{GC}=2.3V
Minimum Gain		-48	-45	dB	V_{GC}=0.3V
Gain Slope		57		dB/V	Measured in 0.5V increments
Gain Control Voltage Range		0 to 2.4		V_{DC}	
Gain Control Input Impedance		30		kΩ	
Noise Figure		10.5	13	dB	At maximum gain and 130MHz
Input IP3	-26	-25		dBm	At +10dB gain and referenced to 1kΩ, Pin=-45dBm per tone
	-28	-26		dBm	At +35dB gain and referenced to 1kΩ, Pin=-45dBm per tone
Input Impedance		1		kΩ	Differential
Stability (Max VSWR)	10:1				Spurious<-70dBm
Power Supply					
Voltage		2.7 to 3.3		V	
Current Consumption		23	25	mA	Maximum gain, V_{CC}=3.0V
Current Consumption		22	24	mA	Minimum gain, V_{CC}=3.0V

Pin	Function	Description	Interface Schematic
1	IN+	Balanced input pin. This pin is internally DC-biased and should be DC blocked if connected to a device with a DC level, other than V_{CC}, present. A DC to connection to V_{CC} is acceptable. For single-ended input operation, one pin is used as an input and the other input is AC-coupled to ground. The balanced input impedance is 1kΩ, while the single-ended input impedance is 500Ω.	
2	IN-	Same as pin 2, except complementary input.	See pin 1 schematic.
3	GND	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane.	
4	GC	Analog gain adjustment for all amplifiers. Valid control ranges are from 0V to 3.0V. Maximum gain is selected with 3.0V. Minimum gain is selected with 0V. These voltages are valid only for a 3.3kΩ DC source impedance.	
5	OUT-	Balanced output pin. This is an open-collector output, designed to operate into a 500Ω balanced load. The load sets the operating impedance, but an external choke or matching inductor to V_{CC} must also be supplied in order to correctly bias this output. This bias inductor is typically incorporated in the matching network between the output and next stage. Because this pin is biased to V_{CC}, a DC-blocking capacitor must be used if the next stage's input has a DC path to ground.	
6	OUT+	Same as pin 5, except complementary output.	See pin 5 schematic.
7	VCC1	Supply voltage pin. External bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. Pins 7 and 8 may share one bypass capacitor if trace lengths are kept minimal.	
8	VCC2	Same as pin 7.	

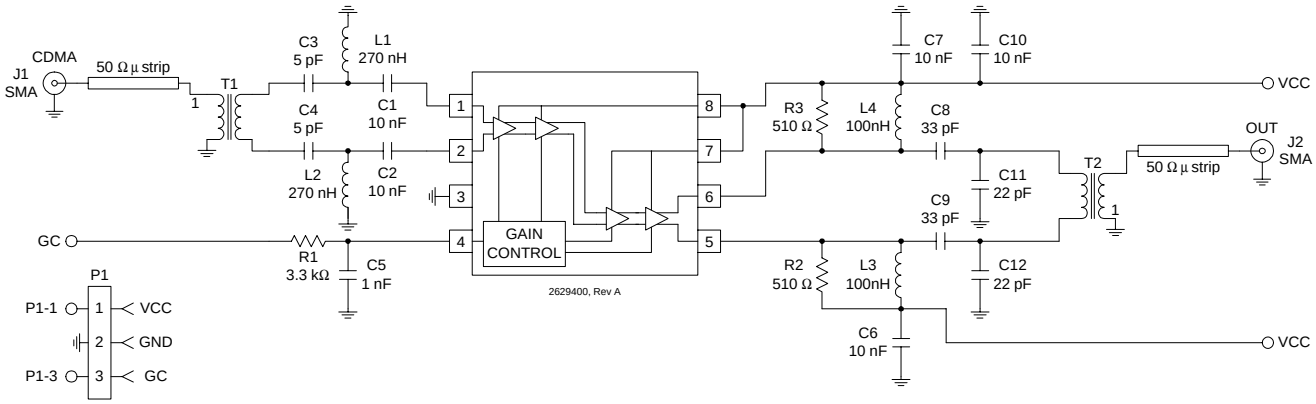
Application Schematic



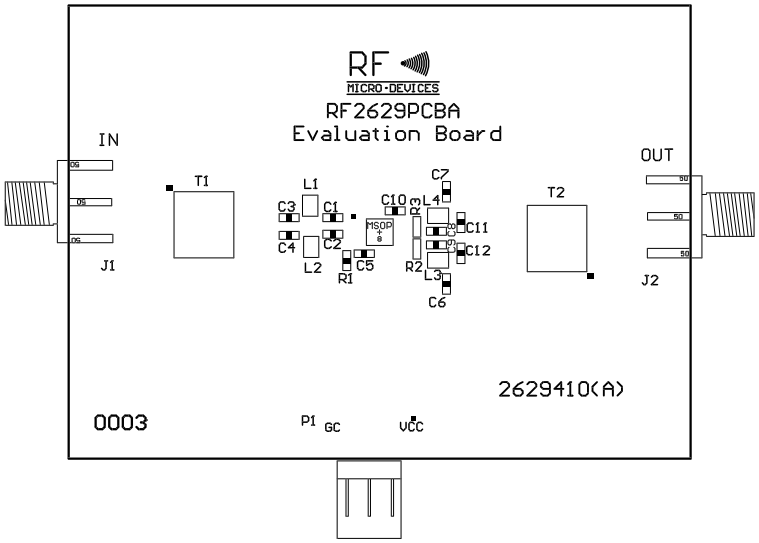
R2 sets the balanced output impedance to 1 kΩ. L1 and C2 serve dual purposes. L1 serves as an output bias choke, and C2 serves as a series DC block. In addition, the values of L1 and C2 may be chosen to form an impedance matching network if the load impedance is not 1 kΩ. Otherwise, the values of L1 and C1 are chosen to form a parallel-resonant tank circuit at the IF when the IF filter's input impedance is 1 kΩ.

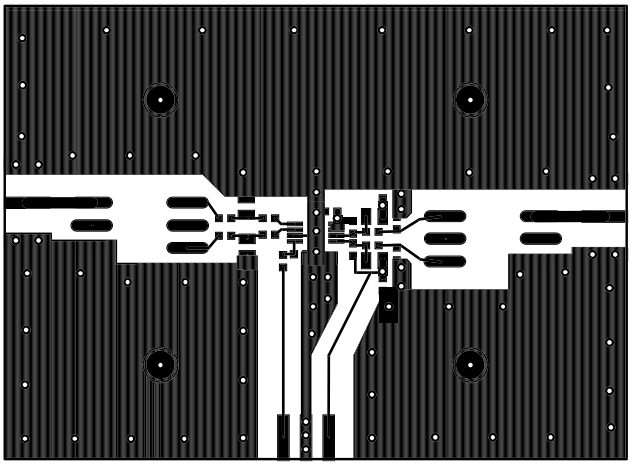
Evaluation Board Schematic

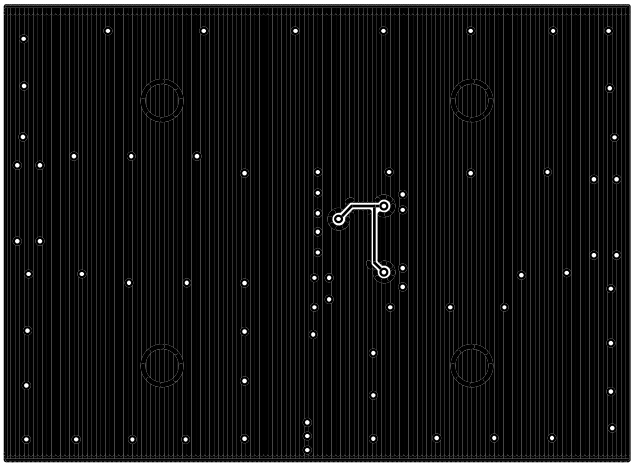
(Download Bill of Materials from www.rfmd.com.)

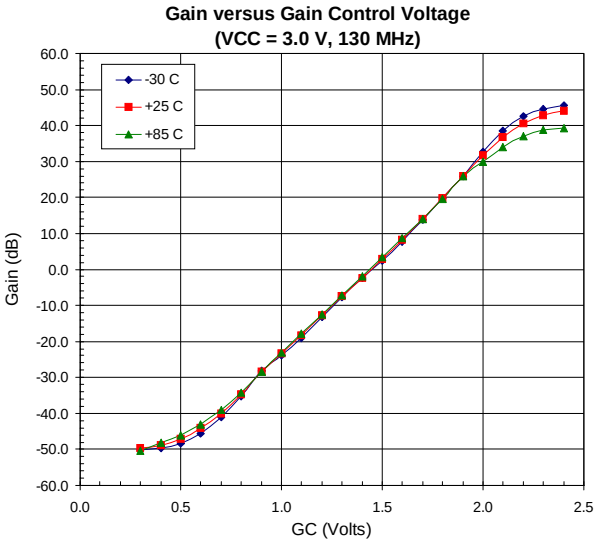


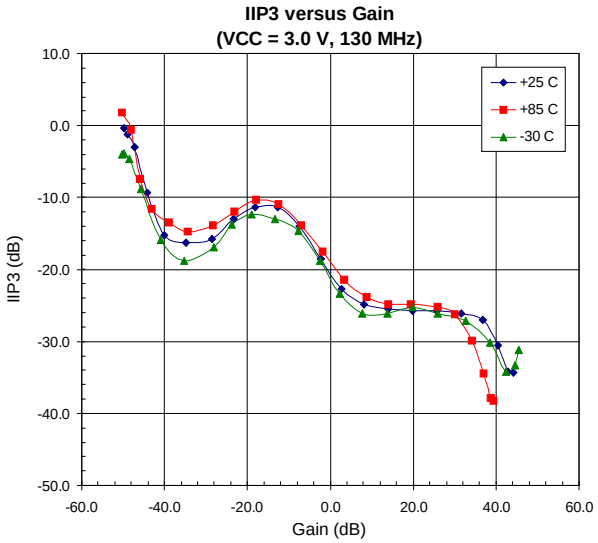
Evaluation Board Layout
Board Size 2.750" x 2.000"
Board Thickness 0.031", FR-4








Gain versus Gain Control Voltage
(VCC = 3.0 V, 130 MHz)
-30 C
+25 C
+85 C
Gain (dB)
GC (Volts)
60.0
50.0
40.0
30.0
20.0
10.0
0.0
-10.0
-20.0
-30.0
-40.0
-50.0
-60.0
0.0
0.5
1.0
1.5
2.0
2.5


IIP3 versus Gain
(VCC = 3.0 V, 130 MHz)
+25 C
+85 C
-30 C
IIP3 (dB)
Gain (dB)
10.0
0.0
-10.0
-20.0
-30.0
-40.0
-50.0
-60.0
-40.0
-20.0
0.0
20.0
40.0
60.0