

Product Description

The RF2642 is a complete upconverter and power amplifier driver designed for CDMA applications. The design features driver amplifier high and low gain states. In the low gain state, the gain is adjustable and the device draws less current. The upconverter is always on. The power down mode turns off the driver amplifier. The device features balanced IF inputs, single-ended LO input and RF output for ease of interface. Packaged in an industry standard 4mmx4mm, 16-pin, leadless chip carrier, the device provides a low-cost solution while easing board space limitations.





Functional Block Diagram

Package Style: LCC, 16-Pin, 4x4

Features

- Single Supply 3.0V Operation
- Step Gain Control
- Power Down Control
- ACPR1=61dBc@885kHz with

 $P_{OUT} = +5 dBm$

Small Leadless LCC 16-Pin Package

Ordering Information RF2642 3V 900MHz Upconverter/ Driver Amplifier with Bypass Mode RF2642 PCBA Fully Assembled Evaluation Board RF Micro Devices, Inc. Tel (336) 664 1233 7625 Thorndike Road Fax (336) 664 0454 Greensboro, NC 27409, USA http://www.rfmd.com 6

Absolute Maximum Ratings

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Parameter	Rating	Unit		
Supply Voltage	-0.5 to +4.5	V _{DC}		
Input RF Power	+3	dBm		
Operating Ambient Temperature	-30 to +85	°C		
Storage Temperature	-30 to +150	°C		



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Baramatar	Specification		llnit	Condition		
Farameter	Min.	Тур.	Max.	Unit	Condition	
Overall					T=25°C, V _{CC} =3.0V, RF _{OUT} =830MHz,	
		0044 040			LO=960MHz@-3dBm, IF=130MHz	
RF Output Frequency Range		824 to 849		MHZ		
IF Frequency Range	-	130		MHZ	0.11	
Output Power	+5		-	dBm		
High Gain Mode					GAIN SELECT=2.7 V, V _{PD} =2.7 V	
Gain	33	34.5	36	dB		
Noise Figure		12	14	dB		
IF Input Impedance		250		Ω	Differential @ 130MHz	
RF Output VSWR		1.5	2:1		824MHz to 849MHz, external components required	
Current Consumption		52		mA		
Adjacent Channel Power Rejection (ACPR1)	55	61		dBc	P _{OUT} =+5dBm, 885kHz offset	
Alternate Channel Power Rejection (ACPR2)	65	78	80	dBc	P _{OUT} =+5dBm, 1.98MHz offset	
Bypass Mode					GAIN SELECT=0V, V _{PD} =2.7V	
Gain		11.9		dB		
Noise Figure		11.9	14	dB		
IF Input Impedance		250		Ω	Differential @ 130MHz	
RF Output VSWR		1.5	2:1		824MHz to 849MHz, external components required	
Output IP3	-4	+5.4		dBm		
Current Consumption		26		mA		
LO Input					954MHz to 979MHz	
LO Frequency Range		954 to 979		MHz		
LO Level	-6	-3	0	dBm		
LO Input Impedance	-	50	-	Ω		
LO to Mixer RF Output Leakage		-33	-20	dBm		
LO Input VSWR		1.4	2:1		GAIN SELECT=0V	
		1.7	2:1		GAIN SELECT=2.7V	
Power Supply						
Voltage	2.7	3.0	3.3	V		
Current Consumption			15	mA	V _{PD} =0V	

NOTE: The measured results <u>do not</u> include the losses from the IF balun and SAW filter. On the evaluation board, those losses are as follows: IF Balun=1dB, SAW Filter=2.5dB to 3.5dB.

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Pin	Function	Description	Interface Schematic
1	GND	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane. This pin is internally con- nected to the die flag.	
2	RF OUT	Output match of the second stage of the power amplifier driver. This amplifier output pin is open collector. It is matched to 50Ω externally using a simple LC match. Refer to the application schematic.	Gain Select =
3	RF GND2	The ground connection for the second stage of the power amplifier driver. The inductance between this pin and the ground plane deter- mines the gain of the second stage. Increased inductance results in reduced gain. On the evaluation board, the emitter ground inductance is set by the length of the PCB trace connected between this pin and the ground. By sliding a 0 Ω ground jumper along this line, the inductance, and hence the gain, may be varied. The evaluation board is shipped with the 0 Ω jumper very close to the part, resulting in minimum inductance, and therefore maximum second stage gain. This translates to higher output IP3 and maximum ACPR1. This setting results in performance 6dB better than the ACPR1 mini- mum specification of 50dBc in the CDMA IS-95 specification for a P_{OUT} =+5dBm.	PCB
4	RF GND1	The ground connection for the first stage of the power amplifier driver. The inductance between this pin and the ground plane determines the gain of the first stage. Increased inductance results in reduced gain. On the evaluation board, the emitter ground inductance is set by the length of the PCB trace connected between this pin and the ground. By sliding a 0 Ω ground jumper along this line, the inductance, and hence the gain, may be varied. The evaluation board is shipped with the 0 Ω jumper far away from the part, resulting in maximum inductance, and therefore minimum first stage gain. More gain may be obtained by shifting the 0 Ω jumper toward the part. A maximum total gain of 40dB may be achieved if the first stage is set to minimum emitter inductor trace length.	See pin 3.
5	VPA1	Power supply pin for the first stage power amplifier. External components provide tuning for the interstage match.	
6	RF IN	RF input to the power amplifier. This input is DC-coupled, so an exter- nal blocking capacitor is needed if the pin is connected to a DC path.	Bias VPA1
7	PD	Power Down control When this pin is low, the amplifier section of the IC is shut off. When this pin is high, the amplifier section of the IC is turned on. The upconverter portion of the IC remains on regardless of the state of PD.	
8	MIX OUT	Output for the upconverting mixer. This input is DC-coupled, so an external blocking capacitor is needed if the pin is connected to a DC path. The output impedance is 50Ω .	
9	GND	Same as pin 1.	

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Pin	Function	Description	Interface Schematic
10	IF-	Balanced IF Input Pin. This pin is internally DC-biased and should be DC-blocked if connected to a device with a DC level present. For single- ended input operation, one pin is used as an input and the other IF input is AC coupled to ground. The input impedance is 250Ω in both the balanced and single-ended modes.	IF+ OFF OFF OFF OFF OFF OFF OFF OFF OFF O
11	IF+	Same as pin 10, except complementary input.	
12	GND	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane.	
13	LO-	Balanced LO Input Pin. This pin is internally DC-biased and should be DC-blocked if connected to a device with a DC level present. For single- ended input operation, one pin is used as an input and the other LO input is AC coupled to ground. The input impedance is 50Ω in both the balanced and single-ended modes.	LO+ O CO-
14	LO+	Same as pin 13, except complementary input.	
15	VCC	Supply voltage for all bias circuits and logic circuits.	
16	GAIN SELECT	When GAIN SELECT is high: the driver amplifier is switched to high gain mode; both amplifier stages are active; the gain is maximized; and, the entire device draws approximately 51 mA. When GAIN SELECT is low, the second stage of the PA driver is turned off and bypassed. This results in a device current of 26 mA, which is approximately a 50% current reduction. The upconverting mixer remains on in both the high and low gain modes to prevent VCO pulling.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with mul- tiple vias.	

PD	Gain Select	Mixer	Amplifier First Stage	Amplifier Second Stage	Gain (dB)*
0	0	ON	OFF	OFF	
0	1	ON	OFF	OFF	
1	0	ON	ACTIVE	BYPASSED	11.9
1	1	ON	ACTIVE	ACTIVE	34.5

*See parameter specifications for conditions.

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Gain and Noise Figure versus LO Drive at $V_{\text{CC}}\text{=}3.0\text{V}$ for Upconverter + PA Driver at High Gain Mode 40.0 35.0 30.0 Gain and Noise Figure (dB) 25.0 20.0 15.0 10.0 - Gain (dB) 5.0 0.0 -10.0 -9.0 -8.0 -7.0 -6.0 -5.0 -4.0 -3.0 -2.0 -1.0 0.0 LO Drive (dBm)



ACPR1 and ACPR2 versus LO Drive at V_{CC} =3.0V for Upconverter + PA Driver at High Gain Mode



Gain and Noise Figure versus LO Drive at $V_{\text{CC}}{=}3.0\text{V}$



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