FUJITSU SEMICONDUCTOR
DATA SHEET

*16-bit Proprietary Microcontroller*

**CMOS**

# F²MC®-16LX MB90335 Series

# MB90337/F337/V330A

## ■ DESCRIPTION

The MB90335 series are 16-bit microcontrollers designed for applications, such as personal computer peripheral devices, that require USB communications. The USB feature supports not only 12-Mbps Function operation but also MiniHost operation. It is equipped with functions that are suitable for personal computer peripheral devices such as displays and audio devices, and control of mobile devices that support USB communications. While inheriting the AT architecture of the F²MC* family, the instruction set supports the C language and extended addressing modes and contains enhanced signed multiplication and division instructions as well as a substantial collection of improved bit manipulation instructions. In addition, long word processing is now available by introducing a 32-bit accumulator.

* : F²MC stands for FUJITSU Flexible Microcontroller, a registered trademark of FUJITSU LIMITED.

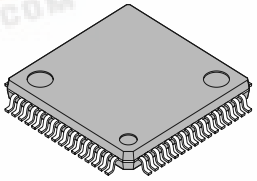
## ■ FEATURES

- **Clock**
  - Built-in oscillation circuit and PLL clock frequency multiplication circuit
  - Oscillation clock
    The machine clock is the oscillation clock divided into 2 (for oscillation 6 MHz : 3 MHz)
    Clock for USB is 48 MHz
    Machine clock frequency of 6 MHz, 12 MHz or 24 MHz selectable
  - Minimum execution time of instruction : 41.6 ns (6 MHz oscillation clock, 4-time multiplied : machine clock 24 MHz and at operating $V_{CC}$ = 3.3 V)
- **The maximum memory space:16 MB**
- **24-bit addressing**
- **Bank addressing**

*(Continued)*

## ■ PACKAGE

64-pin plastic LQFP



(FPT-64P-M09)



FUJITSU

*(Continued)*

- **Instruction system**

  Data types: Bit, Byte, Word, Long word
  Addressing mode (23 types)
  Enhanced high-precision computing with 32-bit accumulator
  Enhance Multiply/Divide instructions with sign and the RETI instruction

- **Instruction system compatible with high-level language (C language) and multitask**
  - Employing system stack pointer
  - Instruction set symmetry and barrel shift instructions
- **Program Patch Function (2 address pointer)**
- **4-byte instruction queue**
- **Interrupt function**
  - Priority levels are programmable
  - 20 interrupts
- **Data transfer function**
  - Expanded intelligent I/O service function (EI$^2$OS) : Maximum of 16 channels
  - µDMAC : Maximum 16 channels
- **Low Power Consumption Mode**
  - Sleep mode (with the CPU operating clock stopped)
  - Time - base timer mode (with the oscillator clock and time - base timer operating)
  - Stop mode (with the oscillator clock stopped)
  - CPU intermittent operation mode (with the CPU operating at fixed intervals of set cycles)
- **Package**
  - LQFP-64P (FPT-64P-M09 : 0.65 mm pin pitch)
- **Process : CMOS technology**
- **Operation guaranteed temperature: –40 °C to +85 °C (0 °C to +70 °C when USB is in use)**

## ■ INTERNAL PERIPHERAL FUNCTION (RESOURCE)

- **I/O port: Max 45 ports**
- **Time-base timer : 1channel**
- **Watchdog timer : 1 channel**
- **16-bit reload timer : 1 channel**
- **Multi-functional timer**
  - 8/16-bit PPG timer (8-bit × 4 channels or 16-bit × 2 channels) the period and duty of the output pulse can be set by the program.
  - 16-bit PWC timer : 1 channel
    Timer function and pulse width measurement function
- **UART : 2 channels**
  - Equipped with Full duplex double buffer with 8-bit lenghth
  - Asynchronous transfer or clock-synchronous serial (I/O extended serial) transfer can be set.
- **Extended I/O serial interface: 1 channel**
- **DTP/External interrupt circuit (8 channels)**
  - Activate the extended intelligent I/O service by external interrupt input
  - Interrupt output by external interrupt input
- **Delayed interrupt output module**
  - Output an interrupt request for task switching
- **USB : 1 channel**
  - USB function (conform to USB 2.0 Full Speed)
  - Supports for Full Speed/Endpoint are specifiable up to six.
  - Dual port RAM (The FIFO mode is supported).
  - Transfer type: Control, Interrupt, Bulk or Isochronous transfer possible
  - USB Mini Host function
- **$I^2C$ Interface : 1 channel**
  - Supports Intel SM bus standards and Phillips $I^2C$ bus standards
  - Two-wire data transfer protocol specification
  - Master and slave transmission/reception

Note : $I^2C$ licenae :
Purchase of Fujitsu $I^2C$ components conveys a license under the Philips $I^2C$ Patent Rights to use, these components in an $I^2C$ system provided that the system conforms to the $I^2C$ Standard Specification as defined by Phillips.

## ■ PRODUCT LINEUP

### 1. MB90335 Series

| Part number | MB90V330A | MB90F337 | MB90337 |
|---|---|---|---|
| Type | For evaluation | Built-in FLASH MEMORY | Built-in Mask ROM |
| ROM capacity | No | 64 Kbyte | |
| RAM capacity | 28 Kbyte | 4 Kbyte | |
| Emulator-specific power supply * | Used bit | — | |
| CPU functions | Number of basic instructions : 351 instructions<br>Minimum instruction execution time : 41.6 ns / at oscillation of 6 MHz (When 4 times is used : Machine clock of 24 MHz)<br>Addressing type : 23 types<br>Program Patch Function : For two address pointers<br>maximum memory space : 16 Mbyte | | |
| Ports | I/O Ports(CMOS) 45 ports | | |
| UART | Equipped with full-duplex double buffer<br>Clock synchronous or asynchronous operation selectable.<br>It can also be used for I/O serial.<br>Built-in special baud-rate generator<br>Built-in 2 channels | | |
| 16-bit reload timer | 16-bit reload timer operation<br>Built-in 1 channel | | |
| Multi-functional timer | 8/16-bit PPG timer (8-bit mode × 4 channels, 16-bit mode × 2 channels)<br>16-bit PWC timer × 1 channel | | |
| DTP/External interrupt | 8 channels<br>Interrupt factor : “L”→“H” edge /“H”→“L” edge /“L” level /“H” level selectable | | |
| $I^2C$ | 1 channel | | |
| Extended I/O serial interface | 1 channel | | |
| USB | 1 channel<br>USB function (conform to USB 2.0 Full Speed)<br>USB Mini-HOST function | | |
| Withstand voltage of 5 V | 6 ports (Excluding VBUS and I/O for $I^2C$) | | |
| Low Power Consumption Mode | Sleep mode/Timebase timer mode/Stop mode/CPU intermittent mode | | |
| Process | CMOS | | |
| Operating voltage VCC | 3.3 V ± 0.3 V (at maximum machine clock 24 MHz) | | |

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used. Please refer to the MB2147-01 or MB2147-20 hardware manual (3.3 Emulator-dedicated Power Supply Switching) about details.

## ■ PACKAGES AND PRODUCT MODELS

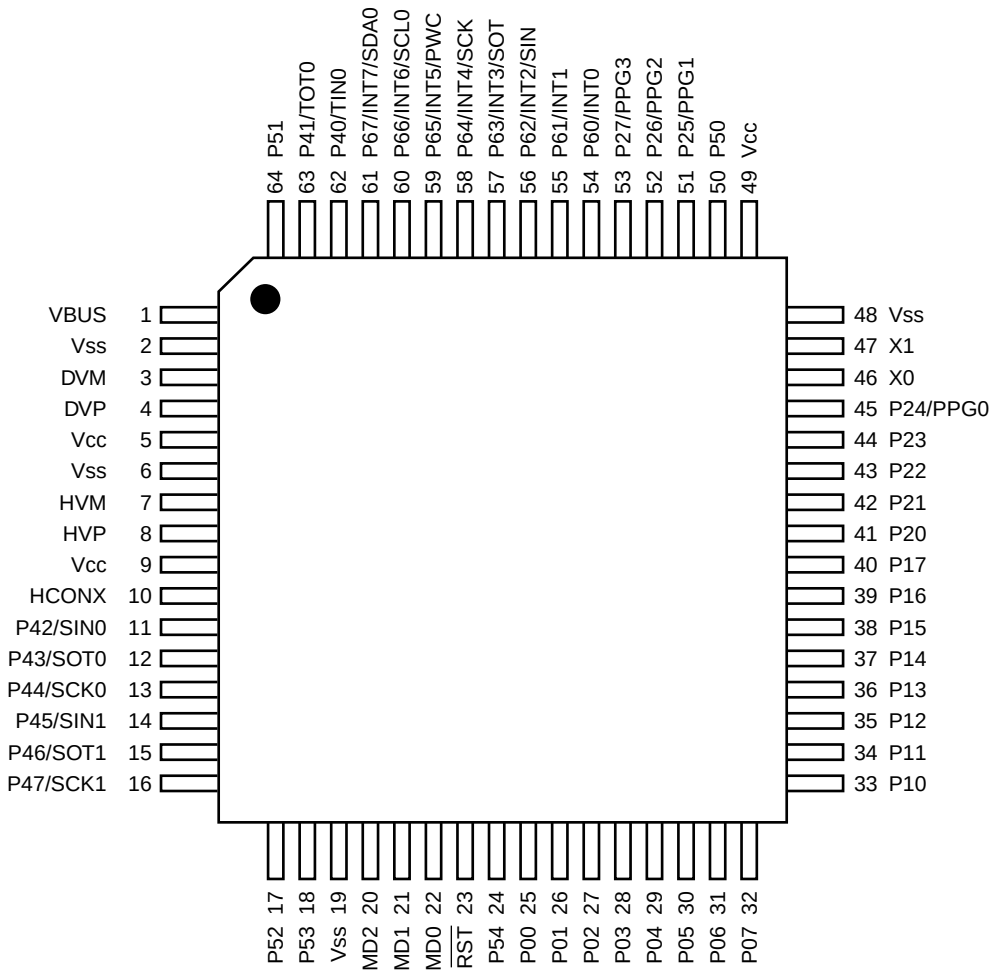
| Package | MB90337 | MB90F337 | MB90V330A |
|---|---|---|---|
| FPT-64P-M09 (LQFP-0.65 mm) | ○ | ○ | × |
| PGA-299C-A01 (PGA) | × | × | ○ |

○ : Yes × : No

Note : For detailed information on each package, see “■ PACKAGE DIMENSIONS”.

## ■ PIN ASSIGNMENT

(TOP VIEW)




(FPT-64P-M09)

## ■ PIN DESCRIPTION

| Pin no. QFPM09 | Pin name | Circuit type* | Status at reset/ function | Function |
|---|---|---|---|---|
| 46 , 47 | X0, X1 | A | Oscillation status | It is a terminal which connects the oscillator.<br>When connecting an external clock, leave the X1 pin side unconnected. |
| 23 | $\overline{\text{RST}}$ | F | Reset input | External reset input pin. |
| 25 to 32 | P00 to P07 | I | Port input (High-Z) | General purpose input/output port.<br>The ports can be set to be added with a pull-up resistor (RD00 to RD07 = 1) by the pull-up resistor setting register (RDR0). (When the power output is set, it is invalid.) |
| 33 to 40 | P10 to P17 | I | | General purpose input/output port.<br>The ports can be set to be added with a pull-up resistor (RD10 to RD17 = 1) by the pull-up resistor setting register (RDR1). (When the power output is set, it is invalid.) |
| 41 to 44 | P20 to P23 | D | | General purpose input/output port. |
| 45 | P24 | D | | General purpose input/output port. |
| | PPG0 | | | Functions as output pins of PPG timers ch0. |
| 51 to 53 | P25 to P27 | D | | General purpose input/output port. |
| | PPG1 to PPG3 | | | Functions as output pins of PPG timers ch1 to ch3. |
| 62 | P40 | H | | General purpose input/output port. |
| | TIN0 | | | Function as event input pin of 16-bit reload timer. |
| 63 | P41 | H | | General purpose input/output port. |
| | TOT0 | | | Function as output pin of 16-bit reload timer. |
| 11 | P42 | H | | General purpose input/output port. |
| | SIN0 | | | Functions as a data input pin for UART ch0. |
| 12 | P43 | H | | General purpose input/output port. |
| | SOT0 | | | Functions as a data output pin for UART ch0. |
| 13 | P44 | H | | General purpose input/output port. |
| | SCK0 | | | Functions as a clock I/O pin for UART ch0. |
| 14 | P45 | H | | General purpose input/output port. |
| | SIN1 | | | Functions as a data input pin for UART ch1. |
| 15 | P46 | H | | General purpose input/output port. |
| | SOT1 | | | Functions as a data output pin for UART ch1. |
| 16 | P47 | H | | General purpose input/output port. |
| | SCK1 | | | Functions as a clock I/O pin for UART ch1. |
| 50 | P50 | K | | General purpose input/output port. |
| 64 | P51 | K | | General purpose input/output port. |
| 17, 18 | P52, P53 | K | | General purpose input/output port. |
| 24 | P54 | K | | General purpose input/output port. |

* : For circuit information, see “■ I/O CIRCUIT TYPE”.

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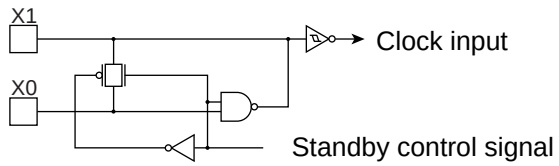
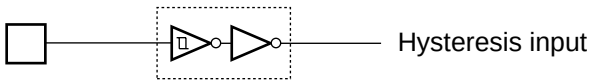
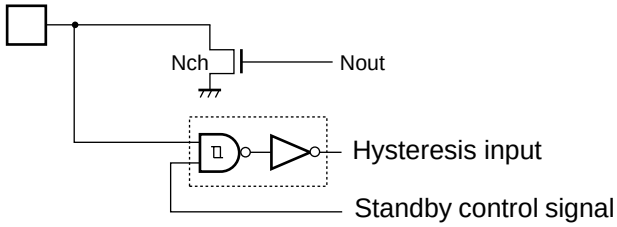
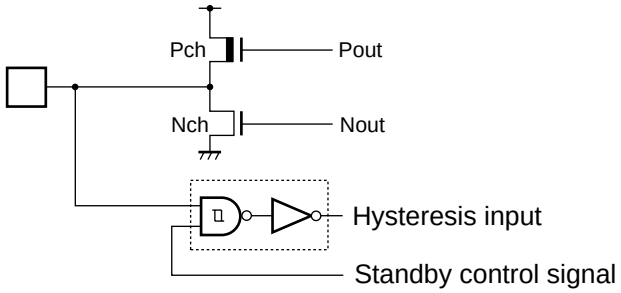
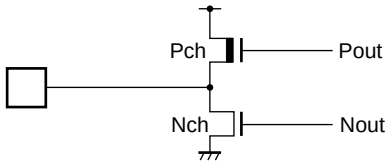
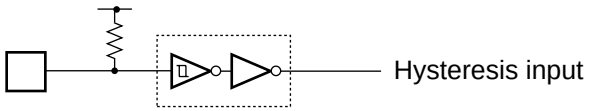
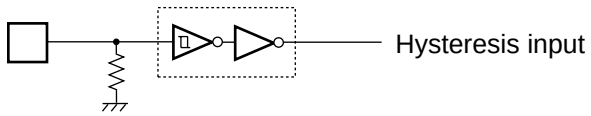
| Pin no. QFPM09 | Pin name | Circuit type* | Status at reset/ function | Function |
|---|---|---|---|---|
| 54, 55 | P60, P61 | C | Port input (High-Z) | General purpose input/output port. (withstand voltage of 5 V) |
| | INT0, INT1 | | | Functions as the input pin for external interrupt ch0 and ch1. |
| 56 | P62 | C | | General purpose input/output port. (withstand voltage of 5 V) |
| | INT2 | | | Functions as the input pin for external interrupt ch2. |
| | SIN | | | Data input pin for simple serial IO. |
| 57 | P63 | C | | General purpose input/output port. (withstand voltage of 5 V) |
| | INT3 | | | Functions as the input pin for external interrupt ch3. |
| | SOT | | | Data output pin for simple serial IO |
| 58 | P64 | C | | General purpose input/output port. (withstand voltage of 5 V) |
| | INT4 | | | Functions as the input pin for external interrupt ch4. |
| | SCK | | | Clock I/O pin for simple serial IO. |
| 59 | P65 | C | | General purpose input/output port. (withstand voltage of 5 V) |
| | INT5 | | | Functions as the input pin for external interrupt ch5. |
| | PWC | | | Functions as the PWC input pin. |
| 60 | P66 | C | | General purpose input/output port. |
| | INT6 | | | Functions as the input pin for external interrupt ch6. |
| | SCL0 | | | Functions as the input/output pin for $I^2C$ interface clock. The port output must be placed in High-Z state during $I^2C$ interface operation. |
| 61 | P67 | C | | General purpose input/output port. |
| | INT7 | | | Functions as the input pin for external interrupt ch7. |
| | SDA0 | | | Functions as the $I^2C$ interface data input/output pin. The port output must be placed in High-Z state during $I^2C$ interface operation. |
| 1 | VBUS | C | VBUS input | Status detection pin of USB cable. |
| 3 | DVM | J | USB input (SUSPEND) | USB function D – pin. |
| 4 | DVP | J | | USB function D + pin. |
| 7 | HVM | J | | USB Mini Host D – pin. |
| 8 | HVP | J | | USB Mini Host D + pin. |
| 10 | HCONX | E | High output | External pull-up resistor connection pin. |
| 21, 22 | MD1, MD0 | B | Mode input Pin | Input pin for selecting operation mode. |
| 20 | MD2 | G | | |
| 5 | Vcc | — | Power supply | Power supply pin. |
| 9 | Vcc | — | | Power supply pin. |
| 49 | Vcc | — | | Power supply pin. |
| 2 | Vss | — | | Power supply pin (GND). |
| 6 | Vss | — | | Power supply pin (GND). |
| 19 | Vss | — | | Power supply pin (GND). |
| 48 | Vss | — | | Power supply pin (GND). |

* : For circuit information, see “■ I/O CIRCUIT TYPE”.

## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|---|---|---|
| A |  | • Oscillation feedback resistance : approx. 1 MΩ<br>• With standby control |
| B |  | • CMOS hysteresis input |
| C |  | • Hysteresis input<br>• Nch open drain output |
| D |  | • CMOS output<br>• CMOS hysteresis input (With input interception function at standby)<br>Note : • The I/O ports and internal resources share one output buffer for their outputs.<br>• The I/O port and internal resources share one input buffer for their input. |
| E |  | • CMOS output |
| F |  | • CMOS hysteresis input with pull-up<br>• Resistor approx. 50 kΩ |
| G |  | • CMOS hysteresis input with pull-down<br>• Resistor approx. 50 kΩ<br>• FLASH product is not provided with pull-down resistor. |

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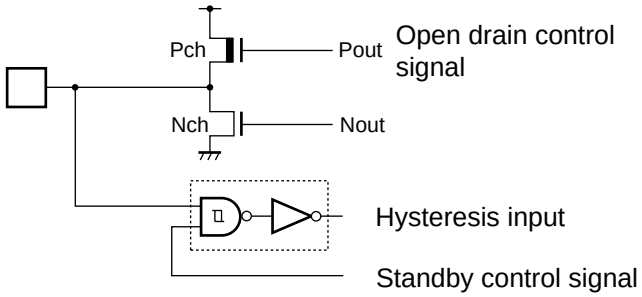
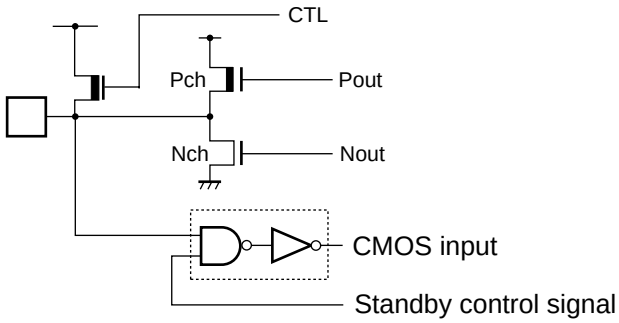
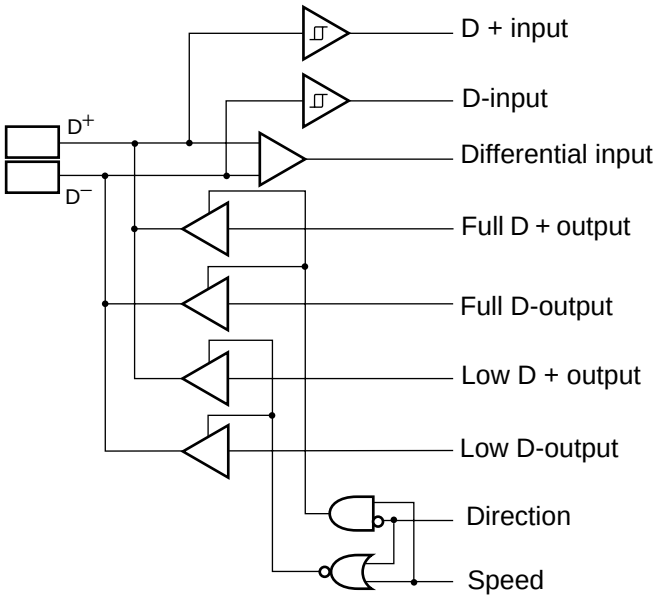
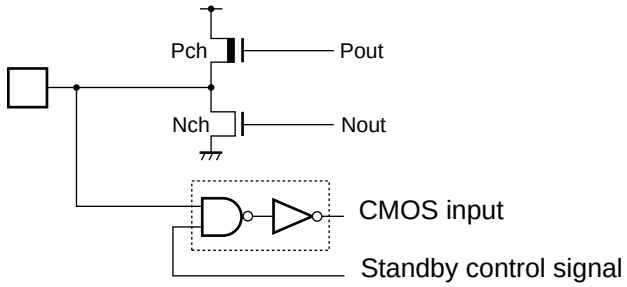
*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| H |  | • CMOS output<br>• CMOS hysteresis input<br>(With input interception function at standby)<br>With open drain control signal |
| I |  | • CMOS output<br>• CMOS input<br>(With input interception function at standby)<br>Programmable pull-up<br>Resistor approx. 50 kΩ |
| J |  | • USB I/O pin |
| K |  | • CMOS output<br>• CMOS input<br>(With input interception function at standby) |

## ■ HANDLING DEVICES

### 1. Preventing latchup and turning on power supply

Latchup may occur on CMOS IC under the following conditions:

1. If a voltage higher than $V_{CC}$ or lower than $V_{SS}$ is applied to input and output pins.

2. A voltage higher than the rated voltage is applied between $V_{CC}$ and $V_{SS}$.

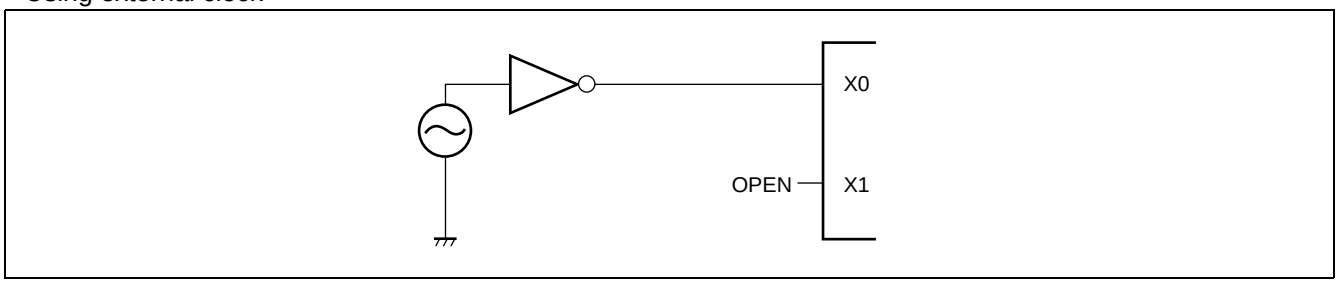
When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using CMOSICs, take great care to prevent the occurrence of latchup.

### 2. Treatment of unused pins

Leaving unused input pins open may cause a malfunction. These pins must therefore be set to a pull-up or pull-down state.

### 3. About the attention when the external clock is used

• Using external clock




### 4. Treatment of power supply pins ($V_{CC}$/$V_{SS}$)

When the device is provided with multiple $V_{CC}$ and $V_{SS}$ pins, be sure to connect all of the power pins to the power supply and ground outside the device to reduce latch-up and unwanted radiation, prevent the strobe signal from malfunctioning due to a rise of grand level, and to follow the standards of total output current for device design reasons. The power supply source should be connected to the $V_{CC}$ and $V_{SS}$ of this device at the lowest possible impedance. It is also advisable to connect a bypass capacitor of approximately 0.1 µF between $V_{CC}$ and $V_{SS}$ near this device.

### 5. About crystal oscillator circuit

Noise near the X0/X1 pin may cause the device to malfunction. When designing the artwork for a PC board using the microcontroller, it is strongly advisable to place the X0/X1 and crystal (ceramic) oscillator, and the bypass capacitor leading to the ground as close to one another as possible and prevent their writing patterns from crossing other patterns as possible be cause stable operation can be expected with such a layout.

### 6. Caution on Operations during PLL Clock Mode

Even if the oscillator comes off or the clock input stops with the PLL clock selected for this microcontroller, the microcontroller may continue to operate at the free-running frequency of the PLL internal automatic oscillator circuit.Performance of this operation, however, cannot be guaranteed.

## 7. Stabilization of supply voltage

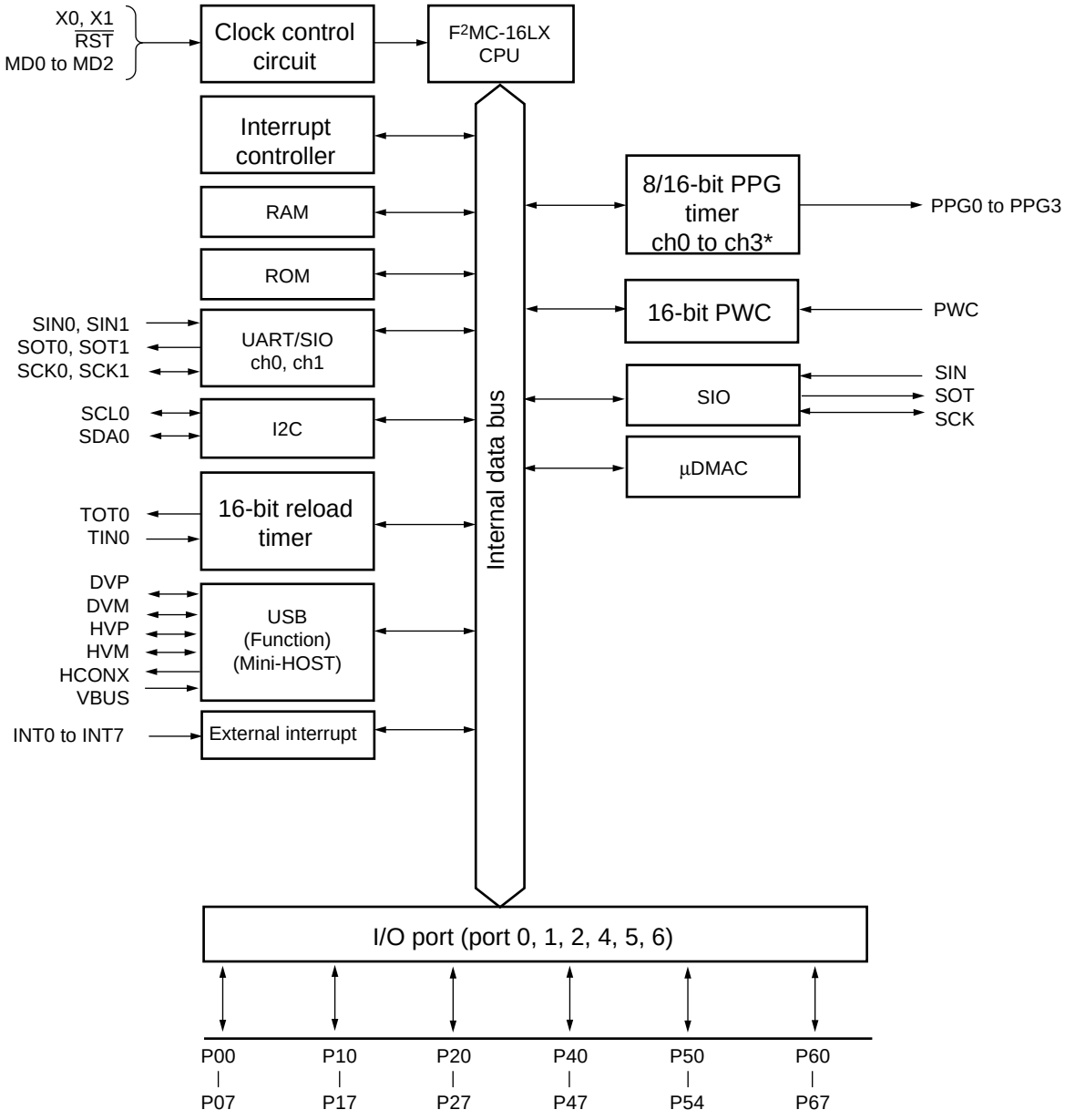
A sudden change in the supply voltage may cause the device to malfunction even within the $V_{CC}$ supply voltage operating range. For stabilization reference, the supply voltage should be controlled so that $V_{CC}$ ripple variations (peak-to-peak values) at commercial frequencies (50 MHz to 60 MHz) fall below 10% of the standard $V_{CC}$ supply voltage and the transient regulation does not exceed
0.1 V/ms at temporary changes such as power supply switching.

## 8. Writing to flash memory

For serial writing to flash memory, always make sure that the operating voltage $V_{CC}$ is between 3.13 V and 3.6 V.

For normal writing to flash memory, always make sure that the operating voltage $V_{CC}$ is between 3.0 V and 3.6 V.

## ■ BLOCK DIAGRAM

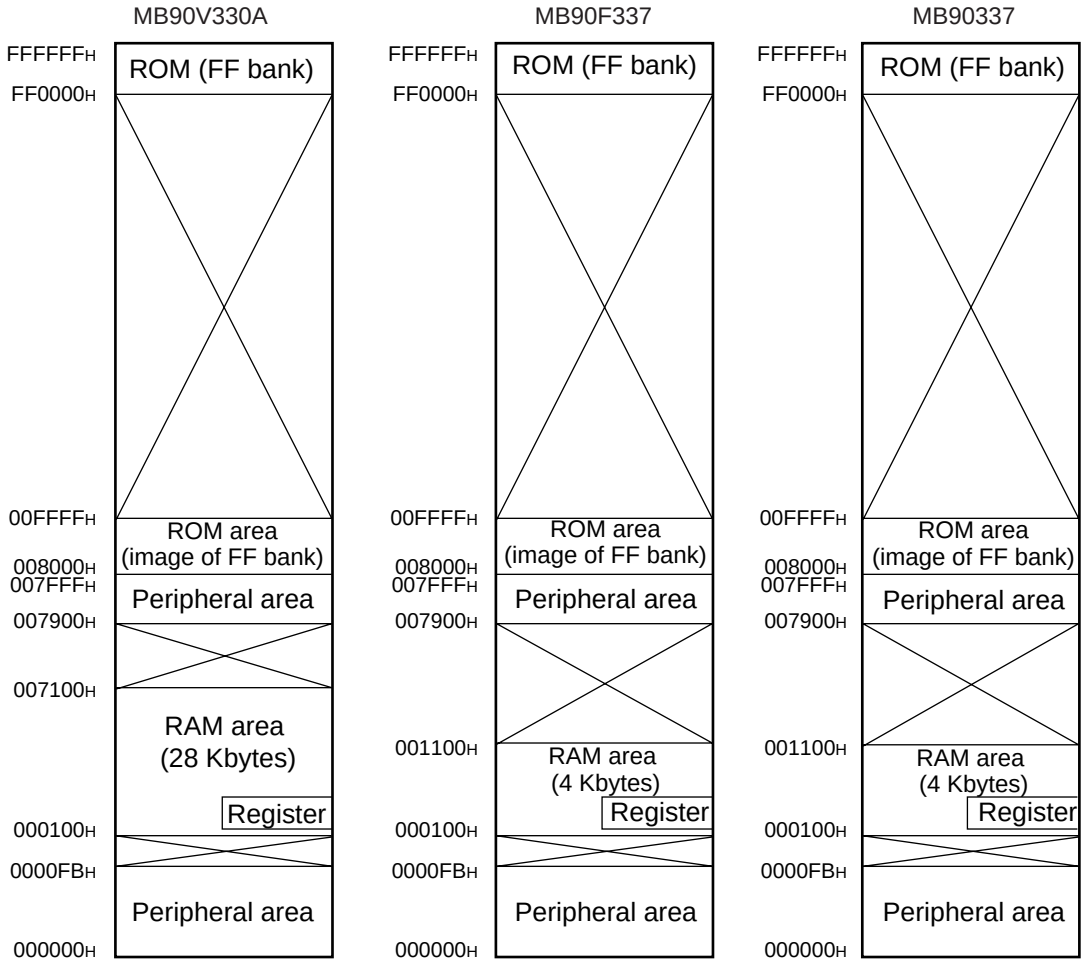



* : Channel for use in 8-bit mode. Two channels (ch1, ch3) are used in 16-bit mode.

Note : I/O ports share pins with peripheral resources.
For details, see “■ PIN ASSIGNMENT” and “■ PIN DESCRIPTION”.
Note also that pins used for peripheral resources cannot serve as I/O ports.

## ■ MEMORY MAP

Single chip mode (ROM mirror function)



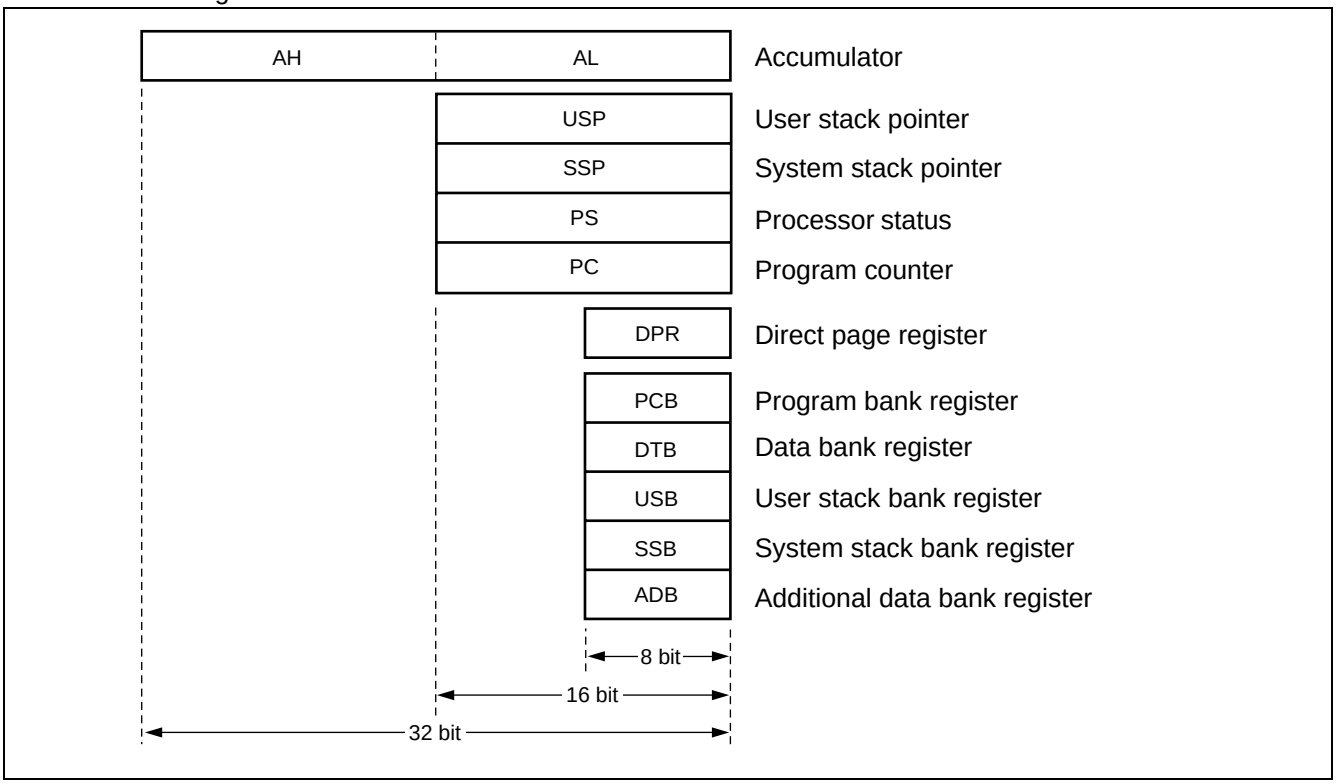

Memory Map of MB90335 Series

Notes :
- When the ROM mirror function register has been set, the mirror image data at higher addresses ("FF8000H to FFFFFFH" ) of bank FF is visible from the higher addresses ("008000H to 00FFFFH") of bank 00.
- For setting the ROM mirror function, see "16. ROM mirror function select module" in "■ PERIPHERAL RESOURCES".

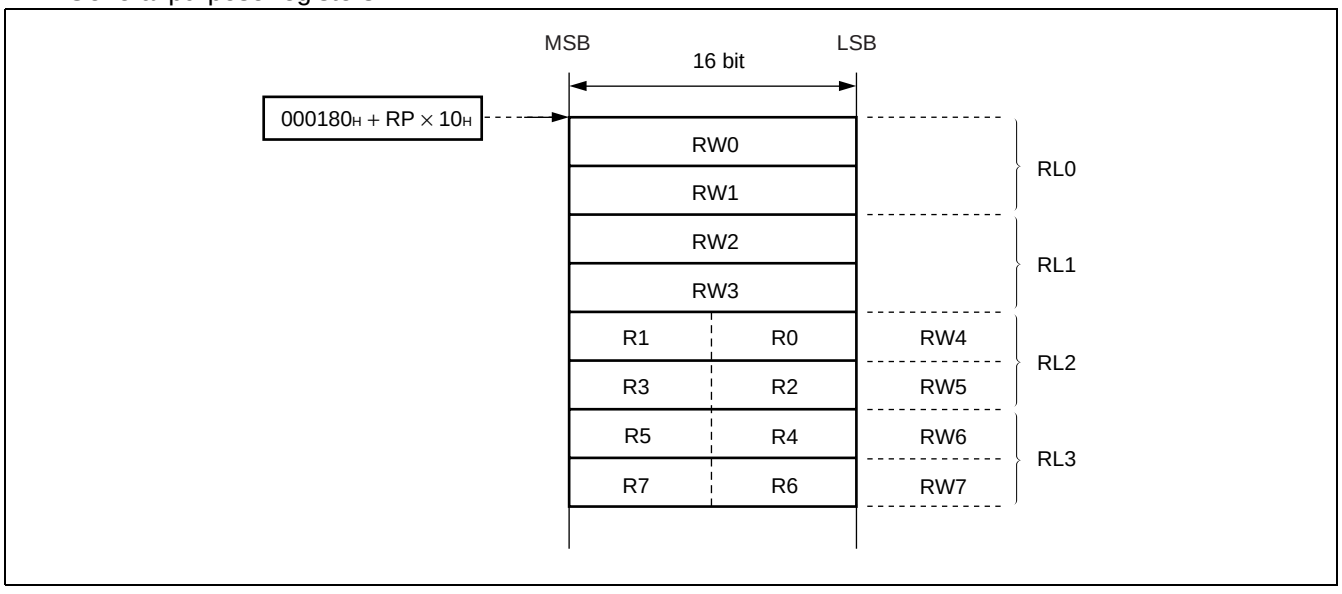
Reference :
- The ROM mirror function is for using the C compiler small model.
- The lower 16-bit addresses of bank FF are equivalent to those of bank 00. Since the ROM area in bank FF exceeds 48 Kbytes, however, the mirror image of all the data in the ROM area cannot be reproduced in bank 00.
- When the C compiler small model is used, the data table mirror image can be shown at "008000H to 00FFFFH" by storing the data table at "FF8000H to FFFFFFH".
  Therefore, data tables in the ROM area can be referenced without declaring the far addressing with the pointer.

## ■ F²MC-16L CPU PROGRAMMING MODEL

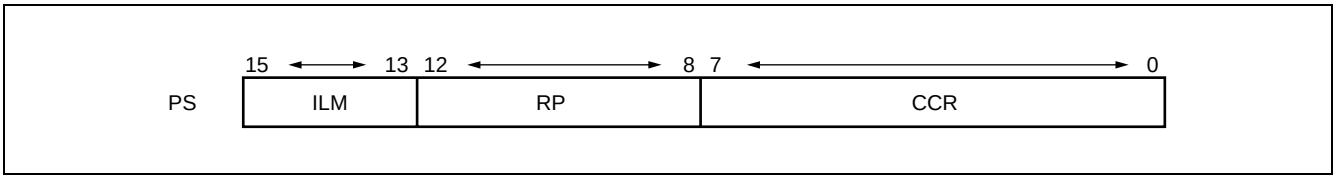
• Dedicated register




• General purpose registers




• Processor status



## ■ I/O MAP

| Address | Register abbreviation | Register | Read/ Write | Resource name | Initial Value |
|---|---|---|---|---|---|
| 000000H | PDR0 | Port 0 Data Register | R/W | Port 0 | XXXXXXXXB |
| 000001H | PDR1 | Port 1 Data Register | R/W | Port 1 | XXXXXXXXB |
| 000002H | PDR2 | Port 2 Data Register | R/W | Port 2 | XXXXXXXXB |
| 000003H | Prohibited | | | | |
| 000004H | PDR4 | Port 4 Data Register | R/W | Port 4 | XXXXXXXXB |
| 000005H | PDR5 | Port 5 Data Register | R/W | Port 5 | - - - XXXXXB |
| 000006H | PDR6 | Port 6 Data Register | R/W | Port 6 | XXXXXXXXB |
| 000007H to 00000FH | Prohibited | | | | |
| 000010H | DDR0 | Port 0 Direction Register | R/W | Port 0 | 0 0 0 0 0 0 0 0B |
| 000011H | DDR1 | Port 1 Direction Register | R/W | Port 1 | 0 0 0 0 0 0 0 0B |
| 000012H | DDR2 | Port 2 Direction Register | R/W | Port 2 | 0 0 0 0 0 0 0 0B |
| 000013H | Prohibited | | | | |
| 000014H | DDR4 | Port 4 Direction Register | R/W | Port 4 | 0 0 0 0 0 0 0 0B |
| 000015H | DDR5 | Port 5 Direction Register | R/W | Port 5 | - - - 0 0 0 0 0B |
| 000016H | DDR6 | Port 6 Direction Register | R/W | Port 6 | 0 0 0 0 0 0 0 0B |
| 000017H to 00001AH | Prohibited | | | | |
| 00001BH | ODR4 | Port 4 Output Pin Register | R/W | Port 4 (OD control) | 0 0 0 0 0 0 0 0B |
| 00001CH | RDR0 | Port 0 Pull-up Resistance Register | R/W | Port 0 (PULL-UP) | 0 0 0 0 0 0 0 0B |
| 00001DH | RDR1 | Port 0 Pull-up Resistance Register | R/W | Port 1 (PULL-UP) | 0 0 0 0 0 0 0 0B |
| 00001EH | Prohibited | | | | |
| 00001FH | | | | | |
| 000020H | SMR0 | Serial Mode Register ch0 | R/W | UART0 | 0 0 1 0 0 0 0 0B |
| 000021H | SCR0 | Serial Control Register ch0 | R/W | | 0 0 0 0 0 1 0 0B |
| 000022H | SIDR0 | Serial Input Data Register ch0 | R | | XXXXXXXXB |
| | SODR0 | Serial Output Data Register ch0 | W | | |
| 000023H | SSR0 | Serial Status Register ch0 | R/W | | 0 0 0 0 1 0 0 0B |
| 000024H | UTRLR0 | UART Prescaler Reload Register ch0 | R/W | Communication Prescaler (UART0) | 0 0 0 0 0 0 0 0B |
| 000025H | UTCR0 | UART Prescaler Control Register ch0 | R/W | | 0 0 0 0 - 0 0 0B |
| 000026H | SMR1 | Serial Mode Register ch1 | R/W | UART1 | 0 0 1 0 0 0 0 0B |
| 000027H | SCR1 | Serial Control Register ch1 | R/W | | 0 0 0 0 0 1 0 0B |
| 000028H | SIDR1 | Serial Input Data Register ch1 | R | | XXXXXXXXB |
| | SODR1 | Serial Output Data Register ch1 | W | | |
| 000029H | SSR1 | Serial Status Register ch1 | R/W | | 0 0 0 0 1 0 0 0B |

*(Continued)*

| Address | Register abbreviation | Register | Read/ Write | Resource name | Initial Value |
|---|---|---|---|---|---|
| 00002A$_H$ | UTRLR1 | UART Prescaler Reload Register ch1 | R/W | Communication Prescaler (UART1) | 0 0 0 0 0 0 0 0$_B$ |
| 00002B$_H$ | UTCR1 | UART Prescaler Control Register ch1 | R/W | | 0 0 0 0 - 0 0 0$_B$ |
| 00002C$_H$ to 00003B$_H$ | Prohibited | | | | |
| 00003C$_H$ | ENIR | Interrupt/DTP Enable Register | R/W | DTP/External interrupt | 0 0 0 0 0 0 0 0$_B$ |
| 00003D$_H$ | EIRR | Interrupt/DTP source Register | R/W | | 0 0 0 0 0 0 0 0$_B$ |
| 00003E$_H$ | ELVR | Request Level Setting Register Lower | R/W | | 0 0 0 0 0 0 0 0$_B$ |
| 00003F$_H$ | | Request Level Setting Register Higher | R/W | | 0 0 0 0 0 0 0 0$_B$ |
| 000040$_H$ to 000045$_H$ | Prohibited | | | | |
| 000046$_H$ | PPGC0 | PPG0 Operation Mode Control Register | R/W | PPG ch0 | 0X0 0 0XX1$_B$ |
| 000047$_H$ | PPGC1 | PPG1 Operation Mode Control Register | R/W | PPG ch1 | 0X0 0 0 0 0 1$_B$ |
| 000048$_H$ | PPGC2 | PPG2 Operation Mode Control Register | R/W | PPG ch2 | 0X0 0 0XX1$_B$ |
| 000049$_H$ | PPGC3 | PPG3 Operation Mode Control Register | R/W | PPG ch3 | 0X0 0 0 0 0 1$_B$ |
| 00004A$_H$ | Prohibited | | | | |
| 00004B$_H$ | | | | | |
| 00004C$_H$ | PPG01 | PPG0 and PPG1 Output Control Register | R/W | PPG ch0/1 | 0 0 0 0 0 0XX$_B$ |
| 00004D$_H$ | Prohibited | | | | |
| 00004E$_H$ | PPG23 | PPG2 and PPG3 Output Control Register | R/W | PPG ch2/3 | 0 0 0 0 0 0 XX$_B$ |
| 00004F$_H$ to 000057$_H$ | Prohibited | | | | |
| 000058$_H$ | SMCS | Serial Mode Control Status Register | R/W | Extended Serial I/O | XXXX0 0 0 0$_B$ |
| 000059$_H$ | | | | | 0 0 0 0 0 0 1 0$_B$ |
| 00005A$_H$ | SDR | Serial Data Register | R/W | | XXXXXXXX$_B$ |
| 00005B$_H$ | SDCR | Communication Prescaler Control Register | R/W | Communication Prescaler | 0XXX0 0 0 0$_B$ |
| 00005C$_H$ | PWCSR | PWC Control Status Register | R/W | 16-bit PWC Timer | 0 0 0 0 0 0 0 0$_B$ |
| 00005D$_H$ | | | | | 0 0 0 0 0 0 0 X$_B$ |
| 00005E$_H$ | PWCR | PWC Data Buffer Register | R/W | | 0 0 0 0 0 0 0 0$_B$ |
| 00005F$_H$ | | | | | 0 0 0 0 0 0 0 0$_B$ |
| 000060$_H$ | DIVR | PWC Dividing Ratio Register | R/W | | - - - - - - 0 0$_B$ |
| 000061$_H$ | Prohibited | | | | |
| 000062$_H$ | TMCSR0 | Timer control status Register | R/W | 16-bit Reload Timer | 0 0 0 0 0 0 0 0$_B$ |
| 000063$_H$ | | | | | XXXX 0 0 0 0$_B$ |
| 000064$_H$ | TMR0 | 16-bit Timer Register Lower | R | | XXXXXXXX$_B$ |
| | TMRLR0 | 16-bit Reload Register Lower | W | | XXXXXXXX$_B$ |
| 000065$_H$ | TMR0 | 16-bit Timer Register Higher | R | | XXXXXXXX$_B$ |
| | TMRLR0 | 16-bit Reload Register Higher | W | | XXXXXXXX$_B$ |

*(Continued)*

| Address | Register abbreviation | Register | Read/ Write | Resource name | Initial Value |
|---|---|---|---|---|---|
| 000066H to 00006EH | Prohibited | | | | |
| 00006FH | ROMM | ROM Mirroring Function Selection Register | W | ROM Mirror Function Selection Module | - - - - - - 1 1B |
| 000070H | IBSR0 | I²C Bus Status Register | R | I²C Bus Interface | 0 0 0 0 0 0 0 0B |
| 000071H | IBCR0 | I²C Bus Control Register | R/W | | 0 0 0 0 0 0 0 0B |
| 000072H | ICCR0 | I²C Bus Clock Selection Register | R/W | | XX 0 XXXXXB |
| 000073H | IADR0 | I²C Bus Address Register | R/W | | XXXXXXXXB |
| 000074H | IDAR0 | I²C Bus Data Register | R/W | | XXXXXXXXB |
| 000075H to 00009AH | Prohibited | | | | |
| 00009BH | DCSR | DMA Descriptor Channel Specification Register | R/W | µDMAC | 0 0 0 0 0 0 0 0B |
| 00009CH | DSRL | DMA Status Register Lower | R/W | | 0 0 0 0 0 0 0 0B |
| 00009DH | DSRH | DMA Status Register Higher | R/W | | 0 0 0 0 0 0 0 0B |
| 00009EH | PACSR | Program Address Detection Control Status Register | R/W | Address Match Detection | 0 0 0 0 0 0 0 0B |
| 00009FH | DIRR | Delayed Interrupt Source generate/ release Register | R/W | Delayed Interrupt | - - - - - - - 0B |
| 0000A0H | LPMCR | Low Power Consumption Mode Register | R/W | Low Power Consumption control circuit | 0 0 0 1 1 0 0 0B |
| 0000A1H | CKSCR | Clock Selection Register | R/W | Clock | 1 1 1 1 1 1 0 0B |
| 0000A2H | Prohibited | | | | |
| 0000A3H | | | | | |
| 0000A4H | DSSR | DMA Stop Status Register | R/W | µDMAC | 0 0 0 0 0 0 0 0B |
| 0000A5H to 0000A7H | Prohibited | | | | |
| 0000A8H | WDTC | Watchdog Control Register | R/W | Watchdog Timer | X - XXX 1 1 1B |
| 0000A9H | TBTC | Time-base Timer Control Register | R/W | Time-base Timer | 1 - - 0 0 1 0 0B |
| 0000AAH | Prohibited | | | | |
| 0000ABH | | | | | |
| 0000ACH | DERL | DMA Enable Register Lower | R/W | µDMAC | 0 0 0 0 0 0 0 0B |
| 0000ADH | DERH | DMA Enable Register Higher | R/W | | 0 0 0 0 0 0 0 0B |
| 0000AEH | FMCR | Flash Memory Control Status Register | R/W | FLASH MEMORY I/F | 0 0 0 X 0 0 0 0B |
| 0000AFH | Prohibited | | | | |

*(Continued)*

| Address | Register abbreviation | Register | Read/ Write | Resource name | Initial Value |
|---|---|---|---|---|---|
| 0000B0H | ICR00 | Interrupt Control Register 00 | R/W | Interrupt Controller | 0 0 0 0 0 1 1 1B |
| 0000B1H | ICR01 | Interrupt Control Register 01 | R/W | | 0 0 0 0 0 1 1 1B |
| 0000B2H | ICR02 | Interrupt Control Register 02 | R/W | | 0 0 0 0 0 1 1 1B |
| 0000B3H | ICR03 | Interrupt Control Register 03 | R/W | | 0 0 0 0 0 1 1 1B |
| 0000B4H | ICR04 | Interrupt Control Register 04 | R/W | | 0 0 0 0 0 1 1 1B |
| 0000B5H | ICR05 | Interrupt Control Register 05 | R/W | | 0 0 0 0 0 1 1 1B |
| 0000B6H | ICR06 | Interrupt Control Register 06 | R/W | | 0 0 0 0 0 1 1 1B |
| 0000B7H | ICR07 | Interrupt Control Register 07 | R/W | | 0 0 0 0 0 1 1 1B |
| 0000B8H | ICR08 | Interrupt Control Register 08 | R/W | | 0 0 0 0 0 1 1 1B |
| 0000B9H | ICR09 | Interrupt Control Register 09 | R/W | | 0 0 0 0 0 1 1 1B |
| 0000BAH | ICR10 | Interrupt Control Register 10 | R/W | | 0 0 0 0 0 1 1 1B |
| 0000BBH | ICR11 | Interrupt Control Register 11 | R/W | | 0 0 0 0 0 1 1 1B |
| 0000BCH | ICR12 | Interrupt Control Register 12 | R/W | | 0 0 0 0 0 1 1 1B |
| 0000BDH | ICR13 | Interrupt Control Register 13 | R/W | | 0 0 0 0 0 1 1 1B |
| 0000BEH | ICR14 | Interrupt Control Register 14 | R/W | | 0 0 0 0 0 1 1 1B |
| 0000BFH | ICR15 | Interrupt Control Register 15 | R/W | | 0 0 0 0 0 1 1 1B |
| 0000C0H | HCNT0 | USB Host Control Register 0 | R/W | USB Mini HOST | 0 0 0 0 0 0 0 0B |
| 0000C1H | HCNT1 | USB Host Control Register 1 | R/W | | 0 0 0 0 0 0 0 1B |
| 0000C2H | HIRQ | USB Host Interruption Register | R/W | | 0 0 0 0 0 0 0 0B |
| 0000C3H | HERR | USB Host Error Status Register | R/W | | 0 0 0 0 0 0 1 1B |
| 0000C4H | HSTATE | USB Host State Status Register | R/W | | XX 0 1 0 0 1 0B |
| 0000C5H | HFCOMP | USB SOF Interrupt FRAME compare Register | R/W | | 0 0 0 0 0 0 0 0B |
| 0000C6H | HRTIMER | USB Retry Timer Setting Register 0 | R/W | | 0 0 0 0 0 0 0 0B |
| 0000C7H | | USB Retry Timer Setting Register 1 | R/W | | 0 0 0 0 0 0 0 0B |
| 0000C8H | | USB Retry Timer Setting Register 2 | R/W | | XXXXXX 0 0B |
| 0000C9H | HADR | USB Host Address Register | R/W | | X 0 0 0 0 0 0 0B |
| 0000CAH | HEOF | USB EOF Setting Register 0 | R/W | | 0 0 0 0 0 0 0 0B |
| 0000CBH | | USB EOF Setting Register 1 | R/W | | XX 0 0 0 0 0 0B |
| 0000CCH | HFRAME | USB FRAME Setting Register 0 | R/W | | 0 0 0 0 0 0 0 0B |
| 0000CDH | | USB FRAME Setting Register 1 | R/W | | XXXXX 0 0 0B |
| 0000CEH | HTOKEN | USB Host Token End Point Register | R/W | | 0 0 0 0 0 0 0 0B |
| 0000CFH | Prohibited | | | | |
| 0000D0H | UDCC | UDC Control Register | R/W | USB function | 1 0 1 0 0 0 0 0B |
| 0000D1H | Prohibited | | | | |

*(Continued)*

| Address | Register abbreviation | Register | Read/ Write | Resource name | Initial Value |
|---|---|---|---|---|---|
| 0000D2H | EP0C | EP0 Control Register | R/W | USB Function | X 1 0 0 0 0 0 0B |
| 0000D3H | | | R/W | | XXXX 0 0 0 XB |
| 0000D4H | EP1C | EP1 Control Register | R/W | | 0 0 0 0 0 0 0 0B |
| 0000D5H | | | R/W | | 0 1 1 0 0 0 0 1B |
| 0000D6H | EP2C | EP2 Control Register | R/W | | 0 1 0 0 0 0 0 0B |
| 0000D7H | | | R/W | | 0 1 1 0 0 0 0 0B |
| 0000D8H | EP3C | EP3 Control Register | R/W | | 0 1 0 0 0 0 0 0B |
| 0000D9H | | | R/W | | 0 1 1 0 0 0 0 0B |
| 0000DAH | EP4C | EP4 Control Register | R/W | | 0 1 0 0 0 0 0 0B |
| 0000DBH | | | R/W | | 0 1 1 0 0 0 0 0B |
| 0000DCH | EP5C | EP5 Control Register | R/W | | 0 1 0 0 0 0 0 0B |
| 0000DDH | | | R/W | | 0 1 1 0 0 0 0 0B |
| 0000DEH | TMSP | Time Stamp Register | R | | 0 0 0 0 0 0 0 0B |
| 0000DFH | | | R/W | | 0 0 0 0 0 0 0 0B |
| 0000E0H | UDCS | UDC Status Register | R/W | | 0 0 0 0 0 0 0 0B |
| 0000E1H | UDCIE | Interrupt Enable Register | R/W | | 0 0 0 0 0 0 0 0B |
| 0000E2H | EP0IS | EP0I Status Register | R/W | | XXXXXXXXB |
| 0000E3H | | | R/W | | 1 0 XXX 1 XXB |
| 0000E4H | EP0OS | EP0O Status Register | R/W | | XXXXXXXXB |
| 0000E5H | | | R/W | | 1 0 0 XX 0 0 XB |
| 0000E6H | EP1S | EP1 Status Register | R | | XXXXXXXXB |
| 0000E7H | | | R/W | | 1 0 0 0 0 0 0 XB |
| 0000E8H | EP2S | EP2 Status Register | R | | XXXXXXXXB |
| 0000E9H | | | R/W | | 1 0 0 0 0 0 0 XB |
| 0000EAH | EP3S | EP3 Status Register | R | | XXXXXXXXB |
| 0000EBH | | | R/W | | 1 0 0 0 0 0 0 XB |
| 0000ECH | EP4S | EP4 Status Register | R | | XXXXXXXXB |
| 0000EDH | | | R/W | | 1 0 0 0 0 0 0 XB |
| 0000EEH | EP5S | EP5 Status Register | R | | XXXXXXXXB |
| 0000EFH | | | R/W | | 1 0 0 0 0 0 0 XB |
| 0000F0H | EP0DT | EP0 Data Register | R/W | | XXXXXXXXB |
| 0000F1H | | | R/W | | XXXXXXXXB |
| 0000F2H | EP1DT | EP1 Data Register | R/W | | XXXXXXXXB |
| 0000F3H | | | R/W | | XXXXXXXXB |
| 0000F4H | EP2DT | EP2 Data Register | R/W | | XXXXXXXXB |
| 0000F5H | | | R/W | | XXXXXXXXB |
| 0000F6H | EP3DT | EP3 Data Register | R/W | | XXXXXXXXB |
| 0000F7H | | | R/W | | XXXXXXXXB |
| 0000F8H | EP4DT | EP4 Data Register | R/W | | XXXXXXXXB |
| 0000F9H | | | R/W | | XXXXXXXXB |

*(Continued)*

| Address | Register abbreviation | Register | Read/ Write | Resource name | Initial Value |
|---|---|---|---|---|---|
| 0000FA$_H$ | EP5DT | EP5 Data Register | R/W | USB Function | XXXXXXXX$_B$ |
| 0000FB$_H$ | | | R/W | | XXXXXXXX$_B$ |
| 0000FC$_H$ to 0000FF$_H$ | Prohibited | | | | |
| 000100$_H$ to 001100$_H$ | RAM Area | | | | |
| 001FF0$_H$ | PADR0 | Program Address Detection Register ch0 Lower | R/W | Address Match Detection | XXXXXXXX$_B$ |
| 001FF1$_H$ | | Program Address Detection Register ch0 Middle | R/W | | XXXXXXXX$_B$ |
| 001FF2$_H$ | | Program Address Detection Register ch0 Higher | R/W | | XXXXXXXX$_B$ |
| 001FF3$_H$ | PADR1 | Program Address Detection Register ch1 Lower | R/W | | XXXXXXXX$_B$ |
| 001FF4$_H$ | | Program Address Detection Register ch1 Middle | R/W | | XXXXXXXX$_B$ |
| 001FF5$_H$ | | Program Address Detection Register ch1 Higher | R/W | | XXXXXXXX$_B$ |
| 007900$_H$ | PRLL0 | PPG Reload Register Lower ch0 | R/W | PPG ch0 | XXXXXXXX$_B$ |
| 007901$_H$ | PRLH0 | PPG Reload Register Higher ch0 | R/W | | XXXXXXXX$_B$ |
| 007902$_H$ | PRLL1 | PPG Reload Register Lower ch1 | R/W | PPG ch1 | XXXXXXXX$_B$ |
| 007903$_H$ | PRLH1 | PPG Reload Register Higher ch1 | R/W | | XXXXXXXX$_B$ |
| 007904$_H$ | PRLL2 | PPG Reload Register Lower ch2 | R/W | PPG ch2 | XXXXXXXX$_B$ |
| 007905$_H$ | PRLH2 | PPG Reload Register Higher ch2 | R/W | | XXXXXXXX$_B$ |
| 007906$_H$ | PRLL3 | PPG Reload Register Lower ch3 | R/W | PPG ch3 | XXXXXXXX$_B$ |
| 007907$_H$ | PRLH3 | PPG Reload Register Higher ch3 | R/W | | XXXXXXXX$_B$ |
| 007908$_H$ to 00790B$_H$ | Prohibited | | | | |
| 00790C$_H$ | FWR0 | Flash Program Control Register 0 | R/W | Flash | 0 0 0 0 0 0 0 0$_B$ |
| 00790D$_H$ | FWR1 | Flash Program Control Register 1 | R/W | Flash | 0 0 0 0 0 0 0 0$_B$ |
| 00790E$_H$ | SSR0 | Sector Conversion Setting Register | R/W | Flash | 0 0 XXXXX0$_B$ |
| 00790F$_H$ to 00791F$_H$ | Prohibited | | | | |

*(Continued)*

*(Continued)*

| Address | Register abbreviation | Register | Read/ Write | Resource name | Initial Value |
|---|---|---|---|---|---|
| 007920H | DBAPL | DMA Buffer Address Pointer Lower 8-bit | R/W | μDMAC | XXXXXXXXB |
| 007921H | DBAPM | DMA Buffer Address Pointer Middle 8-bit | R/W | | XXXXXXXXB |
| 007922H | DBAPH | DMA Buffer Address Pointer Higher 8-bit | R/W | | XXXXXXXXB |
| 007923H | DMACS | DMA Control Register | R/W | | XXXXXXXXB |
| 007924H | DIOAL | DMA I/O Register Address Pointer Lower 8-bit | R/W | | XXXXXXXXB |
| 007925H | DIOAH | DMA I/O Register Address Pointer Higher 8-bit | R/W | | XXXXXXXXB |
| 007926H | DDCTL | DMA Data Counter Lower 8-bit | R/W | | XXXXXXXXB |
| 007927H | DDCTH | DMA Data Counter Higher 8-bit | R/W | | XXXXXXXXB |
| 007928H to 007FFFH | Prohibited | | | | |

- Explanation on read/write
  - R/W Read and write enabled
  - R Read only
  - W Write only

- Explanation of initial values
  - 0 : Initial Value is “0”.
  - 1 : Initial Value is “1”.
  - X : Initial Value is undefined.
  - - : Initial Value is undefined (None).

Note : No IO instruction can be used for registers located between 007900H to 007FFFH.

## ■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

| Interrupt source | EI²OS support | µDMAC | Interrupt vector | | | Interrupt control register | | Priority |
|---|---|---|---|---|---|---|---|---|
| | | | Number* | | Address | ICR | Address | |
| Reset | × | × | #08 | 08H | FFFFDCH | — | — | High |
| INT 9 instruction | × | × | #09 | 09H | FFFFD8H | — | — | |
| Exceptional treatment | × | × | #10 | 0AH | FFFFD4H | — | — | |
| USB Function1 | × | 0, 1 | #11 | 0BH | FFFFD0H | ICR00 | 0000B0H | |
| USB Function2 | × | 2 to 6 | #12 | 0CH | FFFFCCH | | | |
| USB Function3 | × | × | #13 | 0DH | FFFFC8H | ICR01 | 0000B1H | |
| USB Function4 | × | × | #14 | 0EH | FFFFC4H | | | |
| USB Mini-HOST1 | × | × | #15 | 0FH | FFFFC0H | ICR02 | 0000B2H | |
| USB Mini-HOST2 | × | × | #16 | 10H | FFFFBCH | | | |
| I²C ch0 | × | × | #17 | 11H | FFFFB8H | ICR03 | 0000B3H | |
| DTP/External interrupt ch0/1 | ○ | × | #18 | 12H | FFFFB4H | | | |
| No | — | — | #19 | 13H | FFFFB0H | ICR04 | 0000B4H | |
| DTP/External interrupt ch2/3 | ○ | × | #20 | 14H | FFFFACH | | | |
| No | — | — | #21 | 15H | FFFFA8H | ICR05 | 0000B5H | |
| DTP/External interrupt ch4/5 | ○ | × | #22 | 16H | FFFFA4H | | | |
| PWC/Reload timer ch0 | △ | 14 | #23 | 17H | FFFFA0H | ICR06 | 0000B6H | |
| DTP/External interrupt ch6/7 | △ | × | #24 | 18H | FFFF9CH | | | |
| No | — | — | #25 | 19H | FFFF98H | ICR07 | 0000B7H | |
| No | — | — | #26 | 1AH | FFFF94H | | | |
| No | — | — | #27 | 1BH | FFFF90H | ICR08 | 0000B8H | |
| No | — | — | #28 | 1CH | FFFF8CH | | | |
| No | — | — | #29 | 1DH | FFFF88H | ICR09 | 0000B9H | |
| PPG ch0/1 | × | × | #30 | 1EH | FFFF84H | | | |
| No | — | — | #31 | 1FH | FFFF80H | ICR10 | 0000BAH | |
| PPG ch2/3 | × | × | #32 | 20H | FFFF7CH | | | |
| No | — | — | #33 | 21H | FFFF78H | ICR11 | 0000BBH | |
| No | — | — | #34 | 22H | FFFF74H | | | |
| No | — | — | #35 | 23H | FFFF70H | ICR12 | 0000BCH | |
| No | — | — | #36 | 24H | FFFF6CH | | | |
| UART (Send completed) ch0/ch1 | ○ | 13 | #37 | 25H | FFFF68H | ICR13 | 0000BDH | |
| Extended serial I/O | × | 9 | #38 | 26H | FFFF64H | | | |
| UART(Reception completed) ch0/ch1 | ◎ | 12 | #39 | 27H | FFFF60H | ICR14 | 0000BEH | |
| Time-base timer | × | × | #40 | 28H | FFFF5CH | | | |
| Flash memory status | × | × | #41 | 29H | FFFF58H | ICR15 | 0000BFH | |
| Delayed interrupt output module | × | × | #42 | 2AH | FFFF54H | | | Low |

◎ : Available. EI²OS stop function provided (The interrupt request flag is cleared by the interrupt clear signal. There is a stop demand.)
○ : Available (The interrupt request flag is cleared by the interrupt clear signal).
△ : Available when any interrupt source sharing ICR is not used.
× : Unavailable

- If the same interrupt control register (ICR) has two interrupt factors and the use of the EI²OS is permitted, the EI²OS is activated when either of the factors is detected. As any interrupt other than the activation factor is masked while the EI²OS is running, it is recommended that you should mask either of the interrupt requests when using the EI²OS.
- The interrupt flag is cleared by the EI²OS interrupt clear signal for the resource that has two interrupt factors in the same interrupt control register (ICR).

Note : If a resource has two interrupt sources for the same interrupt number, both of the interrupt request flags are cleared by the μDMAC interrupt clear signal. Therefore, when you use either of two interrupt factors for the DMAC function, another interrupt function is disabled. Set the interrupt request permission bit to " 0 " in the appropriate resource, and take measures by software polling.

## ■ USB INTERRUPT FACTOR CONTENTS

| USB interrupt factor | Details |
|---|---|
| USB function 1 | End Point0-IN, EndPoint 0-OUT |
| USB function 2 | End Point 1-5 |
| USB function 3 | VOFF, VON, SUSP, SOF, BRST, WKOP, COHF |
| USB function 4 | SPIT |
| USB Mini-HOST1 | DIRQ, CHHIRQ, URIRQ, RWKIRQ |
| USB Mini-HOST2 | SOFIRQ, CMPIRQ |

## ■ PERIPHERAL RESOURCES

### 1. I/O port

- The I/O ports are used as general-purpose input/output ports (parallel I/O ports). MB90335 series model is provided with 6 ports (45 inputs) . The ports function as input/output pins for peripheral functions also.
- An I/O port, using port data register (PDR) , outputs the output data to I/O pin and input a signal input to I/O port. The port direction register (DDR) specifies direction of input/output of I/O pins on a bit-by-bit basis.
- The following table lists the I/O ports and the peripheral functions with which they share pins.

| | Port pin name | Pin Name (Peripheral) | Peripheral Function that Shares Pin |
|---|---|---|---|
| Port 0 | P00 to P07 | — | |
| Port 1 | P10 to P17 | — | |
| Port 2 | P20 to P23 | — | |
| | P24 to P27 | PPG0 to PPG3 | 8/16 bit PPG timer 0, 1 |
| Port 4 | P40, P41 | TIN0, TOT0 | 16-bit reload timer |
| | P42 to P47 | SIN0, SOT0, SCK0, SIN1, SOT1, SCK1 | UART0, 1 |
| Port 5 | P50 to P54 | — | |
| Port 6 | P60, P61 | INT0, INT1 | External interrupt |
| | P62 to P64 | INT2 to INT4, SIN, SOT, SCK | External interrupt, serial IO |
| | P65 | INT5, PWC | External interrupt, PWC |
| | P66, P67 | INT6, INT7, SCL0, SDA0 | External interrupt, $I^2C$ |

• Register list (port data register)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| PDR0 Address : 000000H | P07 | P06 | P05 | P04 | P03 | P02 | P01 | P00 | XXXXXXXXB | R/W* |
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | |
| PDR1 Address : 000001H | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 | XXXXXXXXB | R/W* |
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| PDR2 Address : 000002H | P27 | P26 | P25 | P24 | P23 | P22 | P21 | P20 | XXXXXXXXB | R/W* |
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| PDR4 Address : 000004H | P47 | P46 | P45 | P44 | P43 | P42 | P41 | P40 | XXXXXXXXB | R/W* |
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | |
| PDR5 Address : 000005H | — | — | — | P54 | P53 | P52 | P51 | P50 | - - - XXXXXB | R/W* |
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| PDR6 Address : 000006H | P67 | P66 | P65 | P64 | P63 | P62 | P61 | P60 | XXXXXXXXB | R/W* |

* : R/W access to I/O ports is a bit different in behavior from R/W access to memory as follows:

- Input mode

  Read : The level at the relevant pin is read.
  Write : Data is written to the output latch.

- Output mode

  Read : The data register latch value is read.
  Write : Data is output to the relevant pin.

• Register list (port direction register)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| DDR0 Address : 000010H | D07 | D06 | D05 | D04 | D03 | D02 | D01 | D 00 | 00000000B | R/W |
| DDR1 Address : 000011H | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 00000000B | R/W |
| | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | | |
| DDR2 Address : 000012H | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 00000000B | R/W |
| | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | | |
| DDR4 Address : 000014H | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 00000000B | R/W |
| | D47 | D46 | D45 | D44 | D43 | D42 | D41 | D40 | | |
| DDR5 Address : 000015H | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | - - - 00000B | R/W |
| | — | — | — | D54 | D53 | D52 | D51 | D50 | | |
| DDR6 Address : 000016H | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 00000000B | R/W |
| | D67 | D66 | D65 | D64 | D63 | D62 | D61 | D60 | | |

- When each pin is serving as a port, the corresponding pin is controlled as follows:
  0 : Input mode
  1 : Output mode
  This bit becomes 0 after a reset.

Note : If these registers are accessed by a read modify write instruction (such as a bit set instruction) , the bits manipulated by the instruction are set to prescribed values but those other bits in output registers which have been set for input are rewritten to the current input values of the pins. When switching a pin from input port to output port, therefore, write a desired value in the PDR first, then set the DDR to switch the pin for output.

• Register list (Port pull-up register)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| RDR0 Address : 00001CH | RD07 | RD06 | RD05 | RD04 | RD03 | RD02 | RD01 | RD00 | 00000000B | R/W |
| RDR1 Address : 00001DH | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 00000000B | R/W |
| | RD17 | RD16 | RD15 | RD14 | RD13 | RD12 | RD11 | RD10 | | |

Controls the pull-up resistor in input mode.

0 : Without pull-up resistor in input mode.

1 : With Pull-up resistor in input mode.

Meaningless in output mode (without pull-up resistor) ./ The input/output register is decided by the setting of the direction register (DDR) .

No pull-up resistor is used in stop mode (SPL = 1).

• Register list (output pin register)

ODR4

Address : 00001B$_H$

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value | Access |
|---|---|---|---|---|---|---|---|---|---|
| OD47 | OD46 | OD45 | OD44 | OD43 | OD42 | OD41 | OD40 | 00000000$_B$ | R/W |

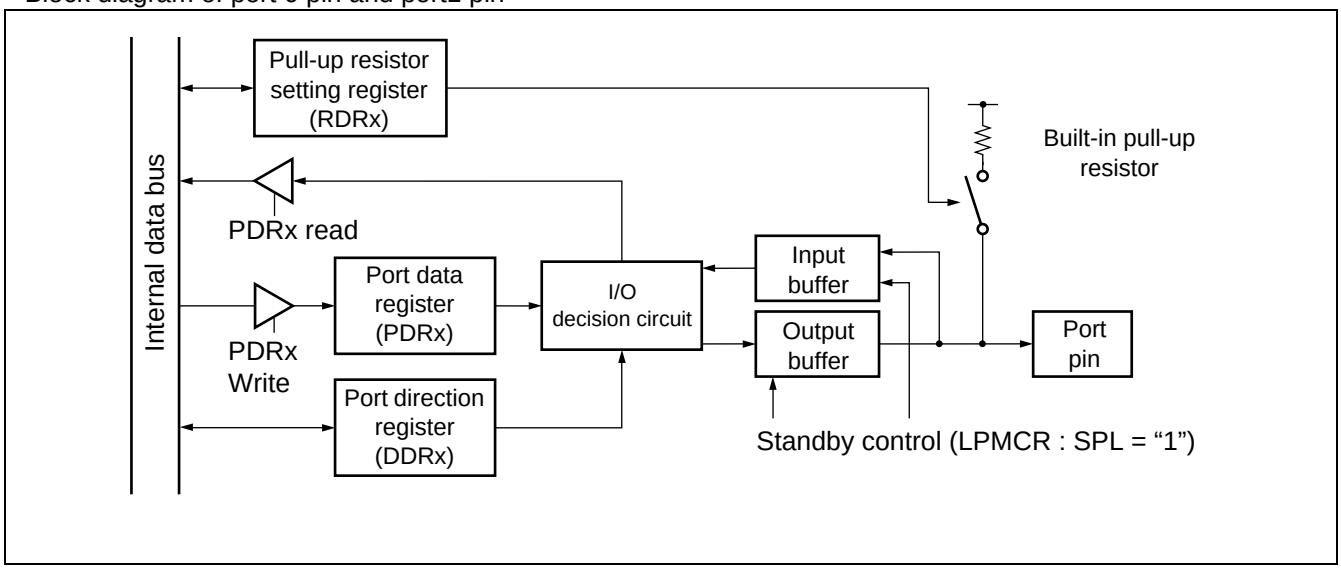
Controls open-drain output in output mode.

0 : Serves as a standard output port in output mode.

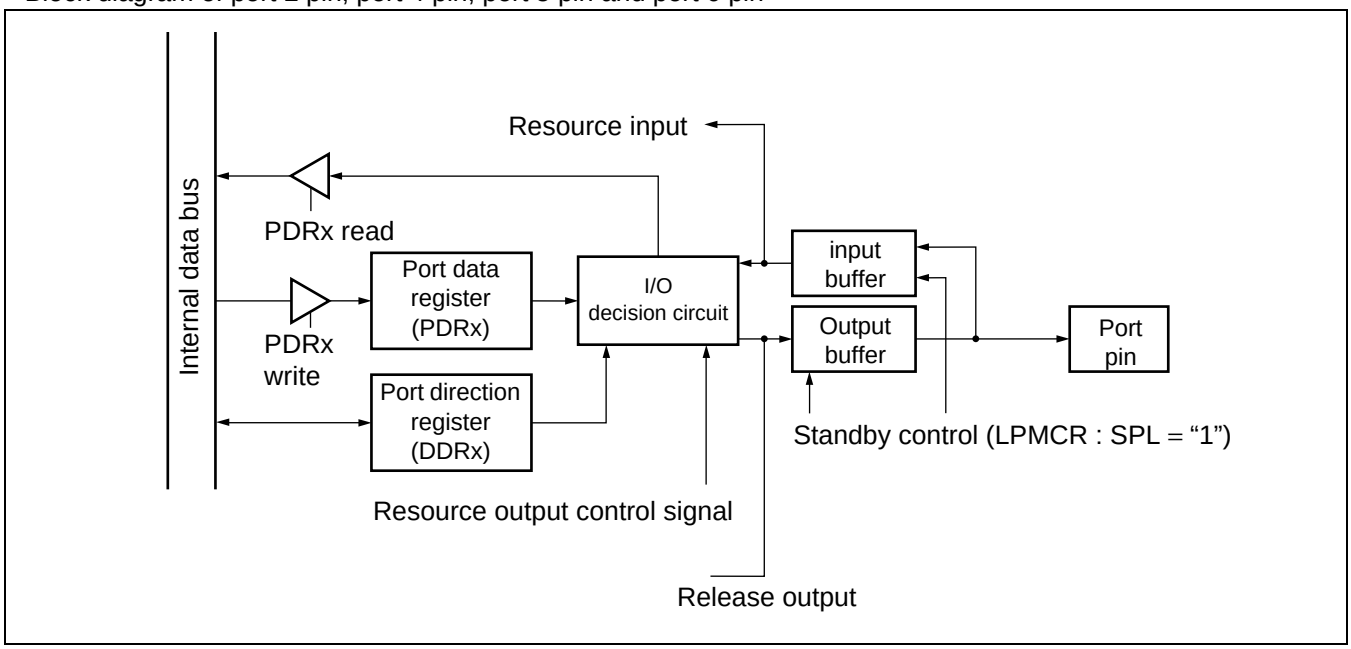
1 : Serves as an open-drain output port in output mode.

Meaningless in input mode. (output High-Z) / The input/output register is decided by the setting of the direction register (DDR) .

• Block diagram of port 0 pin and port1 pin




• Block diagram of port 2 pin, port 4 pin, port 5 pin and port 6 pin



## 2. Time-base timer

- The time-base timer is an 18-bit free-running counter (time-base timer counter) that counts in synchronization with the main clock (2 cycles of the oscillation clock HCLK).
- Four different time intervals can be selected, for each of which an interrupt request can be generated.
- Operating clock signals are supplied to peripheral resources such as the oscillation stabilization wait timer and watchdog timer.

**• Interval time of time-base timer**

| Internal count clock cycle | Interval time |
|---|---|
| 2/HCLK (0.33 µs) | $2^{12}$/HCLK (Approx. 0.68 ms) |
| | $2^{14}$/HCLK (Approx. 2.7 ms) |
| | $2^{16}$/HCLK (Approx. 10.9 ms) |
| | $2^{19}$/HCLK (Approx. 87.4 ms) |

Notes : • HCLK : Oscillation clock frequency
• The parenthesized values assume an oscillator clock frequency of 6 MHz.

**• Clock cycles supplied from time-base timer**

| Where to supply clock | Clock cycle |
|---|---|
| Oscillation stabilization wait of main clock | $2^{13}$/HCLK (Approx. 1.36 ms) |
| | $2^{15}$/HCLK (Approx. 5.46 ms) |
| | $2^{17}$/HCLK (Approx. 21.84 ms) |
| Watch dog timer | $2^{12}$/HCLK (Approx. 0.68 ms) |
| | $2^{14}$/HCLK (Approx. 2.7 ms) |
| | $2^{16}$/HCLK (Approx. 10.9 ms) |
| | $2^{19}$/HCLK (Approx. 87.4 ms) |

Notes : • HCLK : Oscillation clock frequency
• The parenthesized values assume an oscillator clock frequency of 6 MHz.

**• Register list**

Time-base timer control register (TBTC)

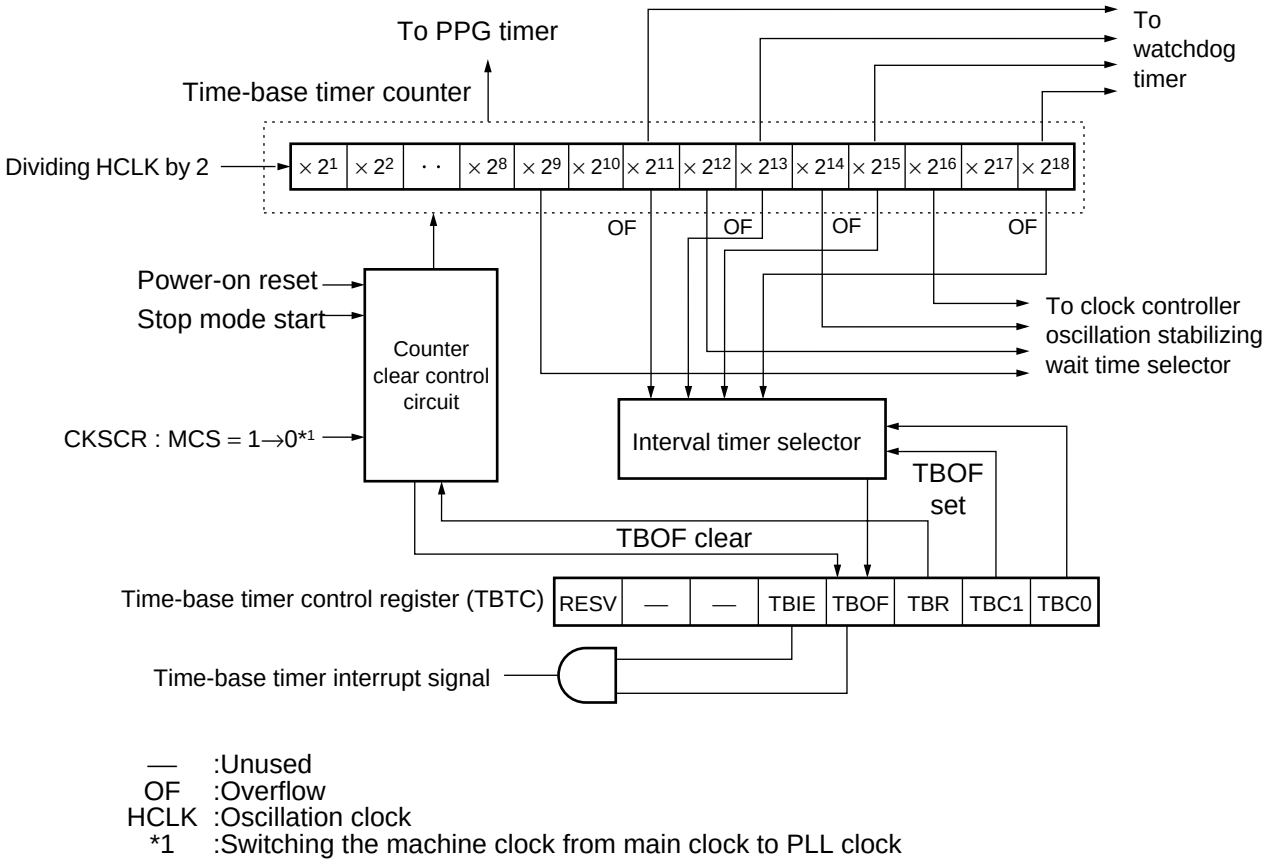
Address : $0000A9_H$

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESV | — | — | TBIE | TBOF | TBR | TBC1 | TBC0 |
| ( R/W ) | ( — ) | ( — ) | ( R/W ) | ( R/W ) | ( W ) | ( R/W ) | ( R/W ) |

Initial Value
$1\text{--}00100_B$

Note : For the conditions for clearing the time-base timer, refer to the chapter for the time-base timer in the hardware manual.

• Block Diagram




— :Unused
OF :Overflow
HCLK :Oscillation clock
*1 :Switching the machine clock from main clock to PLL clock

Actual interrupt request number of time-base timer is as follows:
Interrupt request number:#40 ($28_H$)

## 3. Watchdog timer

- The watchdog timer is a timer counter prepared in case programs run out of control.
- The watchdog timer is a 2-bit counter using the time-base timer as the count clock.
- When started, the watchdog timer resets the CPU if it is not cleared before the two-bit counter overflows.

**• Interval time of watchdog timer**

| HCLK: Oscillation clock (6 MHz) | | |
|---|---|---|
| **Min** | **Max** | **Clock cycle** |
| Approx. 2.39 ms | Approx. 3.07 ms | $2^{14} \pm 2^{11}$ / HCLK |
| Approx. 9.56 ms | Approx. 12.29 ms | $2^{16} \pm 2^{13}$ / HCLK |
| Approx. 38.23 ms | Approx. 49.15 ms | $2^{18} \pm 2^{15}$ / HCLK |
| Approx. 305.83 ms | Approx. 393.22 ms | $2^{21} \pm 2^{18}$ / HCLK |

Notes :
- The maximum and minimum time intervals for the watchdog timer depend on the counter clear timing.
- The watchdog timer contains a 2-bit counter that counts the carry signals of the time-base timer. When the device is operating with HCLK, therefore, clearing the time-base timer lengthens the watchdog reset generation time interval.

• Event that stop the watchdog timer

1 : Stop due to a Power-on reset

2 : watchdog reset

• Clear factor of watch dog timer

1 : External reset input by RST pin

2 : Writing “0” to the software reset bit

3 : Writing “0” to the watchdog control bit (second and subsequent times)

4 : Transition to sleep mode (Clearing the watchdog timer, and suspend counting)

5 : Transition to time-base timer mode (Clearing the watchdog timer, and suspend counting)

6 : Transition to stop mode (Clearing the watchdog timer, and suspend counting)

• Register list

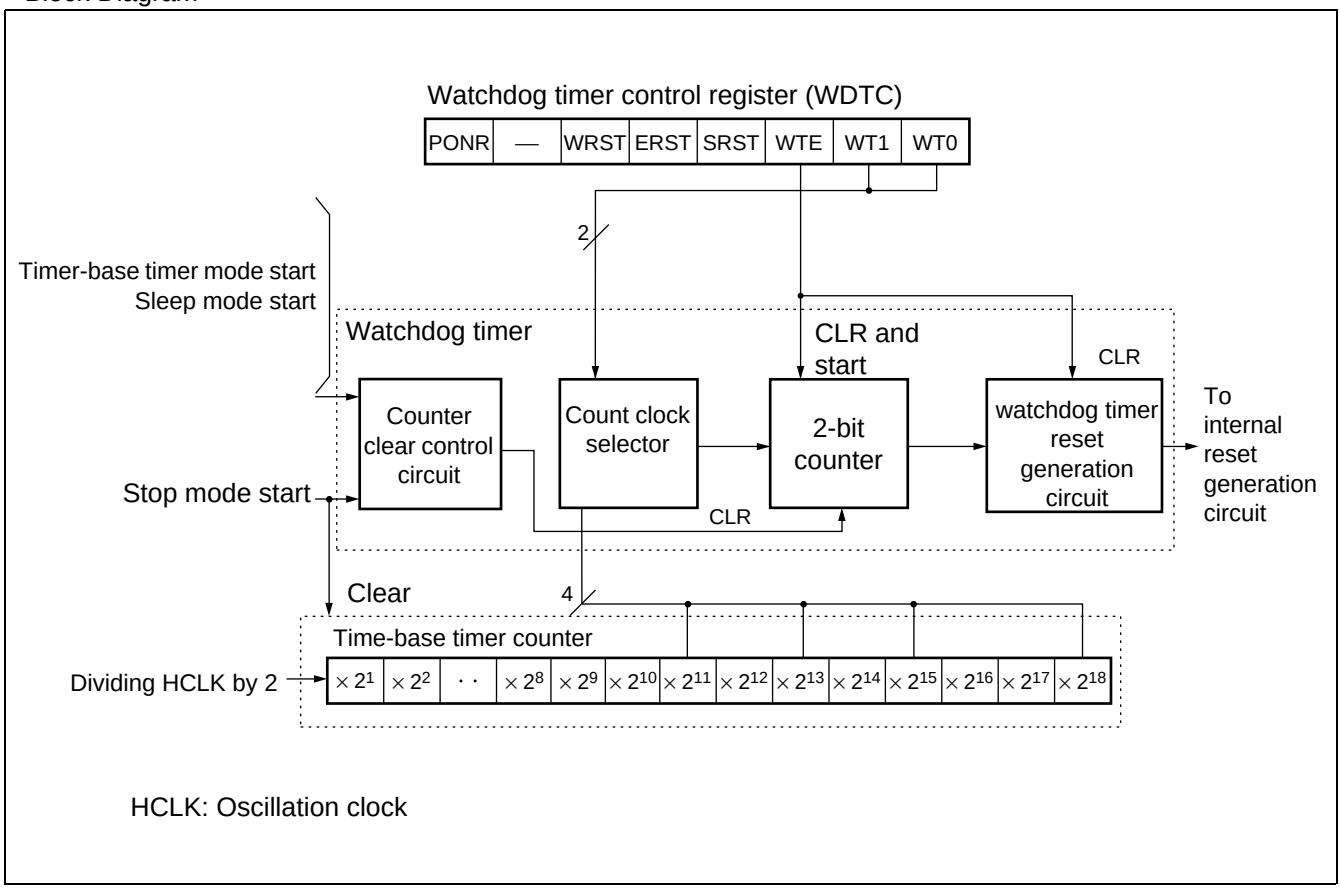
Watchdog timer control register (WDTC)

Address : 0000A8H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PONR | — | WRST | ERST | SRST | WTE | WT1 | WT0 |
| ( R ) | ( — ) | ( R ) | ( R ) | ( R ) | ( W ) | ( W ) | ( W ) |

Initial Value
X-XXX111B

• Block Diagram




HCLK: Oscillation clock

## 4. 16 - bit Reload Timer

The 16-bit reload timer has the internal clock mode to be decrement in synchronization with three different internal clocks and the event count mode to decrement upon detection of an arbitrary edge of the pulse input to the external pin. Either can be selected. This timer defines when the count value changes from $0000_H$ to $FFFF_H$ as an underflow. The timer therefore causes an underflow when the count reaches [reload register setting +1]. Either mode can be selected for the count operation from the reload mode which repeats the count by reloading the count setting value at the underflow occurrence or the one-shot mode which stops the count at the underflow occurrence. The interrupt can be generated at the counter underflow occurrence so as to correspond to the DTC.

• Register list

• Timer control status register

Timer control status register (Higher) (TMCSR0)

Address : $000063_H$

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | CSL1 | CSL0 | MOD2 | MOD1 |
| ( — ) | ( — ) | ( — ) | ( — ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value $XXXX0000_B$

Timer control status register (Lower) (TMCSR0)

Address : $000062_H$

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MOD0 | OUTE | OUTL | RELD | INTE | UF | CNTE | TRG |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value $00000000_B$

• 16-bit timer register/16-bit reload register

TMR0/TMRLR0 (Higher)

Address : $000065_H$

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D09 | D08 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value $XXXXXXXX_B$

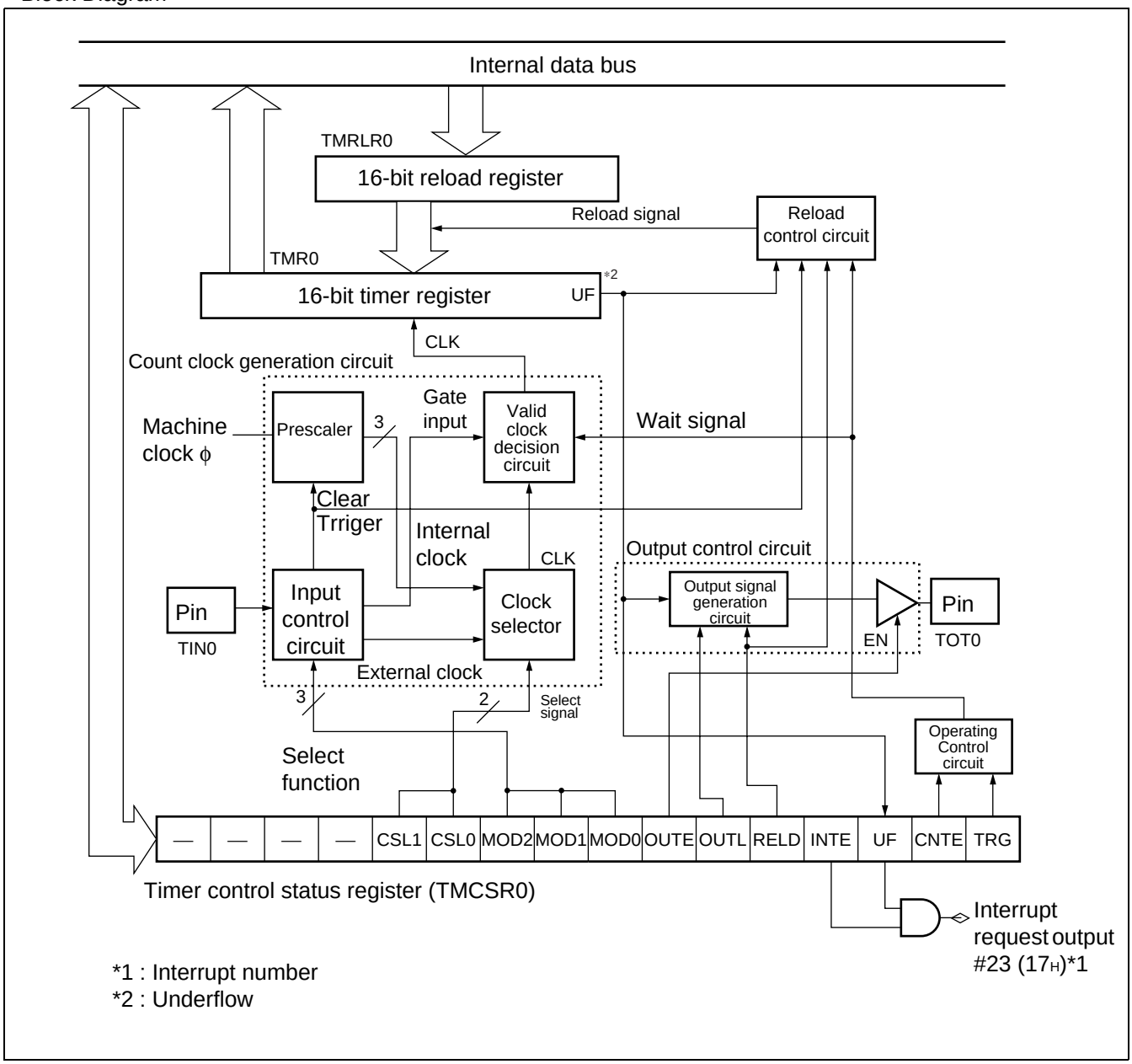
TMR0/TMRLR0 (Lower)

Address : $000064_H$

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value $XXXXXXXX_B$

• Block Diagram



## 5. Multifunction timer

- The multifunction timer can be used for waveform output, input pulse width measurement, and external clock cycle measurement.

**• Configuration of a multi-functional timer**

| 8/16 bit PPG timer | 16 bit PWC timer |
|---|---|
| 8 bit × 4 ch<br>(16 bit × 2 ch) | 1 ch |

• 8/16 bit PPG timer (8 bit : 4 channels, 16 bit : 2 channels)

8/16 bit PPG timer consists of a 8 bit down counter (PCNT) , PPG control register (PPGC0 to PPGC3) , PPG clock control register (PCS01, PCS23) and PPG reload register (PRLL0 to PRLL3, PRLH0 to PRLH3) .

When used as an 8/16 bit reload timer, the PPG timer serves as an event timer. It can also output pulses of an arbitrary duty ratio at an arbitrary frequency.

- 8 bit PPG mode
  Each channel operates as an independent 8 bit PPG.
- 8 bit prescaler + 8 bit PPG mode
  Operates as an arbitrary-cycle 8 bit PPG with ch0 (ch2) operating as an 8 bit prescaler and ch2 (ch3) counted by the borrow output of ch0 (ch2).
- 16 bit PPG mode
  Operates as a 16 bit PPG with ch0 (ch2) and ch1 (ch3) connected.
- PPG Operation
  The PPG timer outputs pulses of an arbitrary duty ratio (the ratio between the High and Low level periods of pulse waveform) at an arbitrary frequency. Can also be used as a D/A converter by an external circuit.

• Register list

PPG operation mode control register
(PPGC1/PPGC3)

Address : 000047H, 000049H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| PEN1 | — | PE10 | PIE1 | PUF1 | MD1 | MD0 | Reserved |
| ( R/W ) | ( — ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value
0X000001B

(PPGC0/PPGC2)

Address : 000046H, 000048H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PEN0 | — | PE0O | PIE0 | PUF0 | — | — | Reserved |
| ( R/W ) | ( — ) | ( R/W ) | ( R/W ) | ( R/W ) | ( — ) | ( — ) | ( R/W ) |

Initial Value
0X000XX1B

PPG output control register (PPG01/PPG23)

Address : 00004CH, 00004EH

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PCS2 | PCS1 | PCS0 | PCM2 | PCM1 | PCM0 | Reserved | Reserved |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value
000000XXB

PPG reload register
(PRLH0 to PRLH3)

Address : 007901H, 007903H, 007905H, 007907H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D09 | D08 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value
XXXXXXXXB

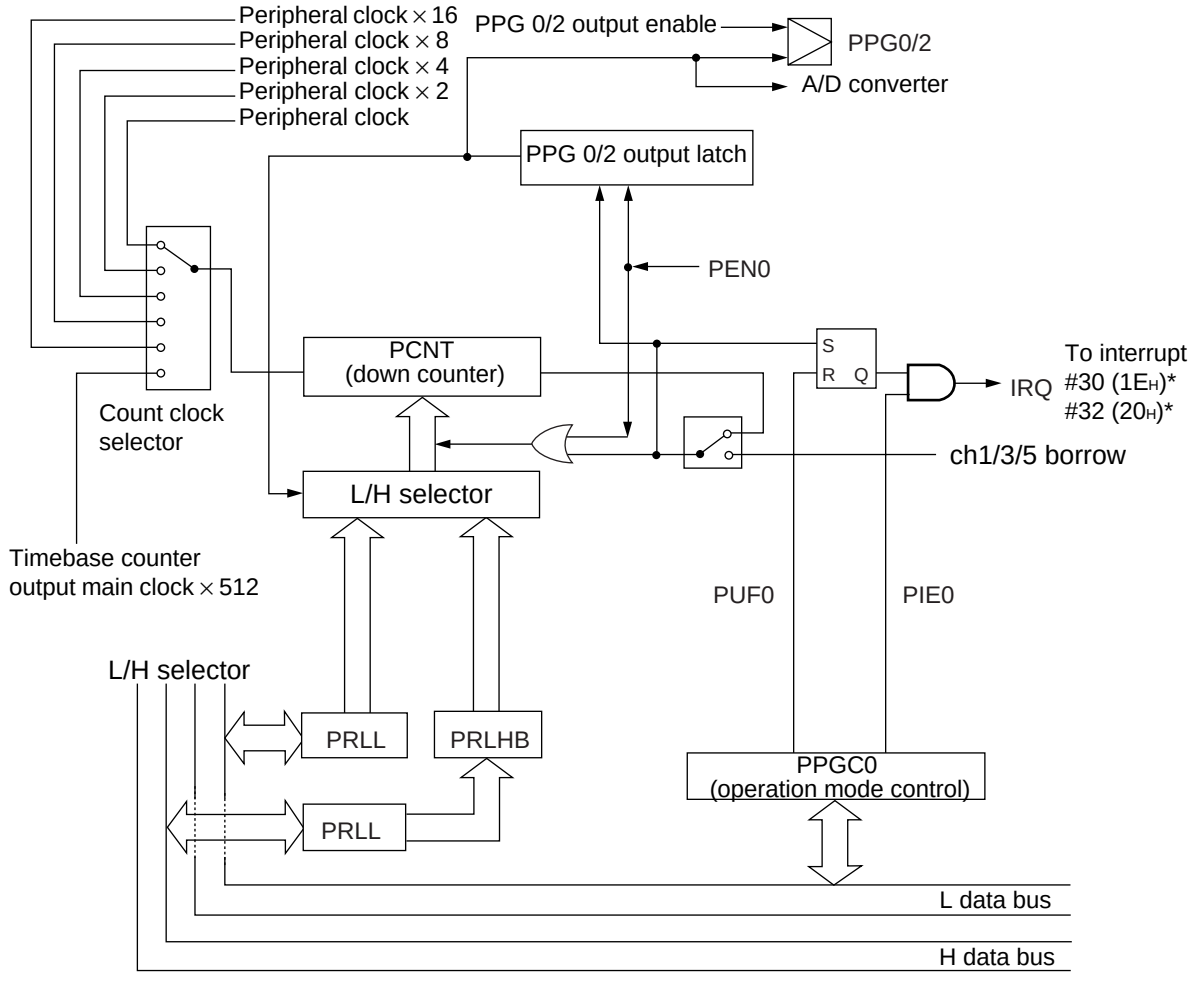
(PRLL0 to PRLL3)

Address : 007900H, 007902H, 007904H, 007906H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

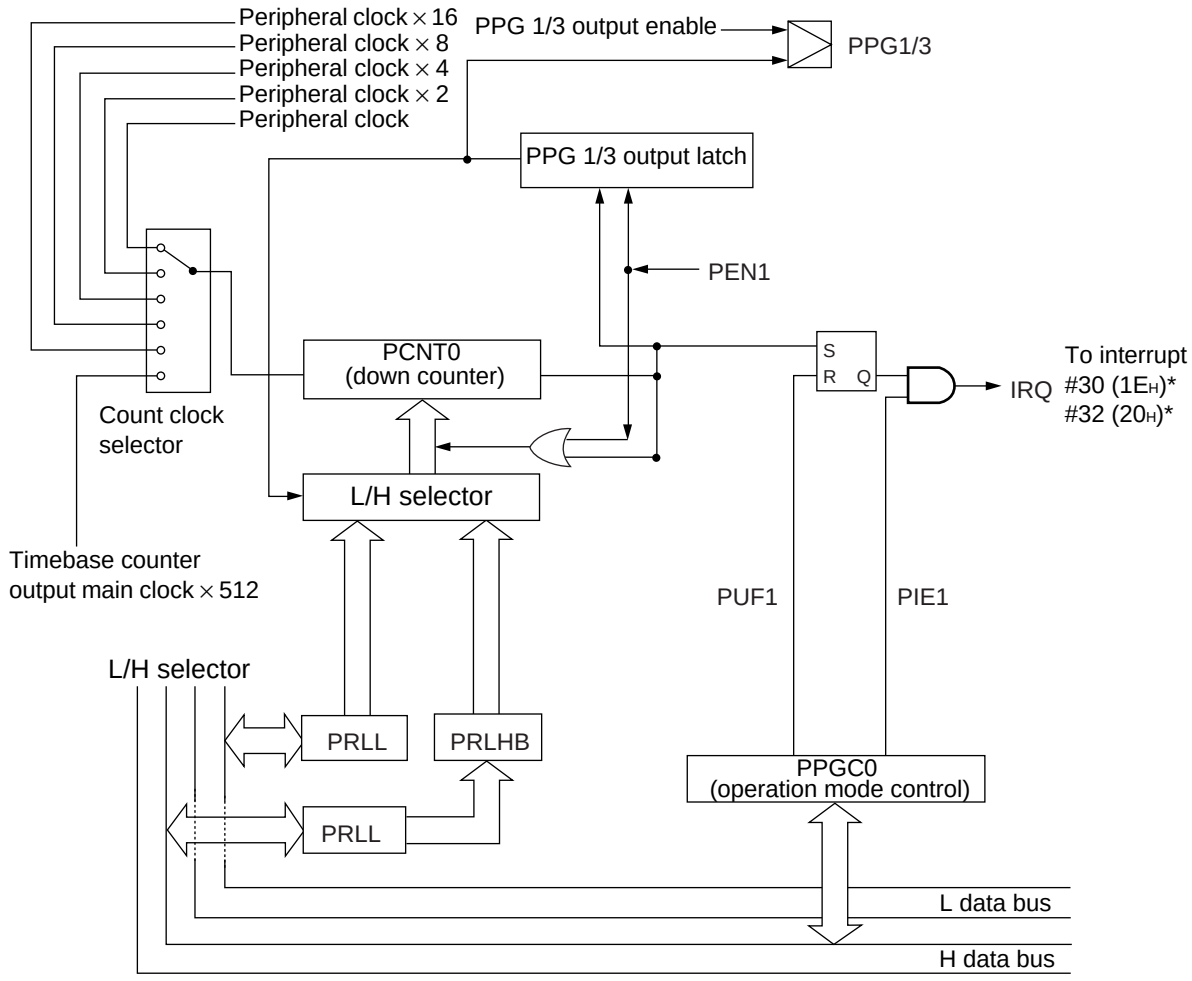
Initial Value
XXXXXXXXB

• 8 bit PPG ch0/2 block diagram




* : Interrupt number

• 8 bit PPG ch1/3 block diagram




* : Interrupt number

• PWC timer

The PWC timer is a 16 bit multifunction up-count timer capable of measuring the input signal pulse width.

• Register list

PWC control status register (PWCSR)

Address : 00005D$_H$

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| STRT | STOP | EDIR | EDIE | OVIR | OVIE | ERR | Reserved |
| ( R/W ) | ( R/W ) | ( R ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R ) | ( R/W ) |

Initial Value 0000000X$_B$

Address : 00005C$_H$

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CKS1 | CKS0 | PIS1 | PIS0 | S/C | MOD2 | MOD1 | MOD0 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000000$_B$

PWC data buffer register (PWCR)

Address : 00005F$_H$

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000000$_B$

Address : 00005E$_H$

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000000$_B$

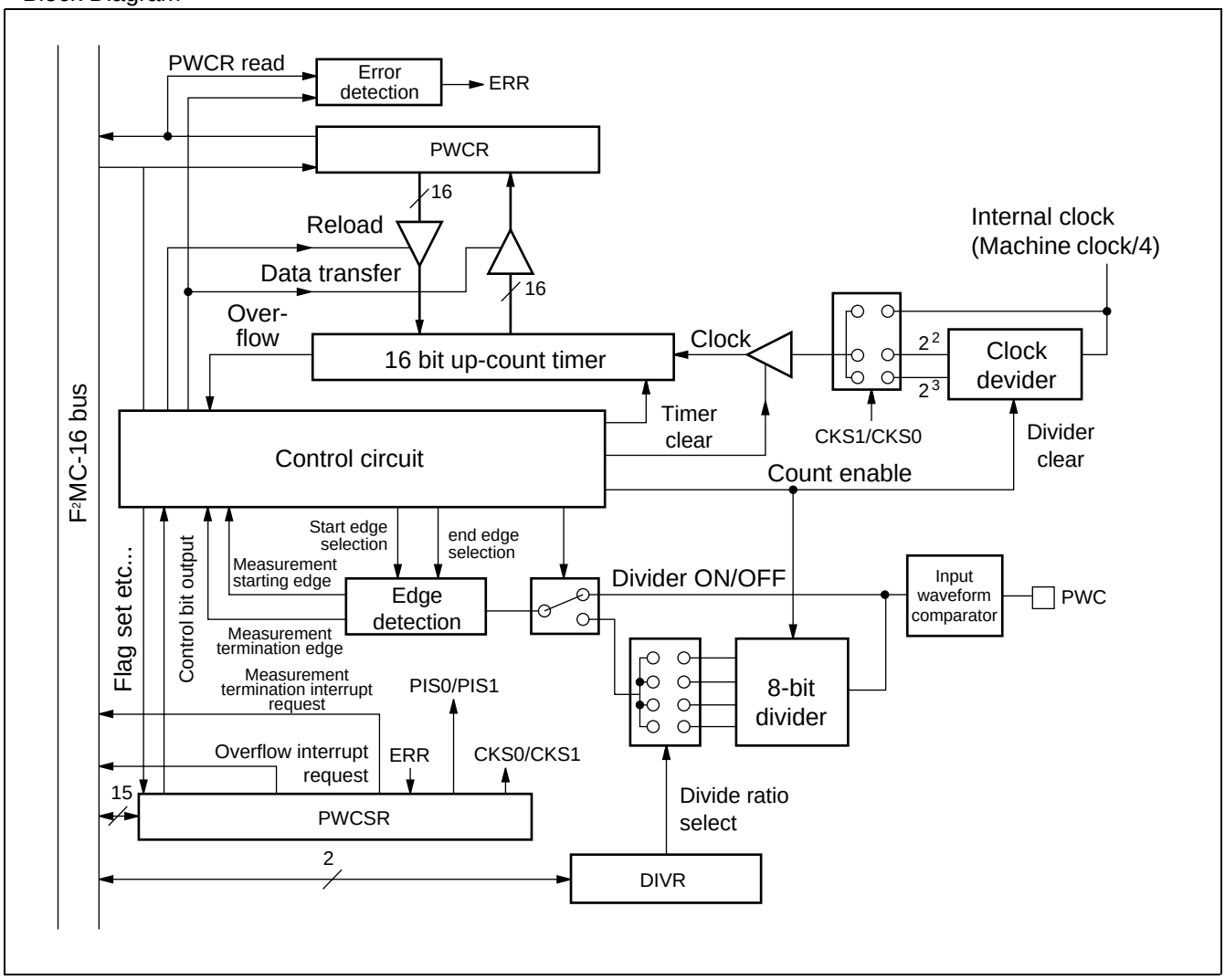
Ratio of dividing frequency control register (DIVR)

Address : 000060$_H$

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | DIV1 | DIV0 |
| ( — ) | ( — ) | ( — ) | ( — ) | ( — ) | ( — ) | ( R/W ) | ( R/W ) |

Initial Value ------00$_B$

• Block Diagram



## 6. UART

**Overview of UART**

- UART is a general purpose serial communication interface for synchronous or asynchronous (start-stop synchronization) communications with external devices.
- It supports bi-directional communication (normal mode) and master/slave communication (multi-processor mode: supported on master side only).
- An interrupt can be generated upon completion of reception, detection of a reception errror, or upon completion of transmission. EI$^2$OS is supported also.

• UART functions

UART, or a generic serial data communication interface that sends and receives serial data to and from other CPU and peripherals, has the functions listed in following.

| | Function |
|---|---|
| Data buffer | Full-duplex double-buffered |
| Transmission mode | • Clock synchronous (without start/stop bit)<br>• Clock asynchronous (start-stop synchronous) |
| Baud rate | • Special-purpose baud-rate generator<br>It is optional from eight kinds.<br>• Baud rate by external clock (clock of SCK0/SCK1 terminal input) |
| Data length | • 8 bits or 7 bits (in the asynchronous normal mode only)<br>• 1 to 8 bits (in the synchronous mode only) |
| Signaling system | Non Return to Zero (NRZ) system |
| Reception error detection | • Framing error<br>• Overrun error<br>• Parity error (Not supported in operation mode 1) |
| Interrupt request | • Receive interrupt (reception completed, reception error detected)<br>• Transmission interrupt (transmission completed)<br>• Both the transmission and reception support EI$^2$OS. |
| Master/slave type communication function (multi processor mode) | Capable of 1 (master) to n (slaves) communication (available just as master) |

Note : In clock synchronous transfer mode, the UART transfers only data with no start or stop bit added.

**UART operation modes**

| Operation mode | | Data length | | Synchronization | Stop bit length |
|---|---|---|---|---|---|
| | | Without parity | With parity | | |
| 0 | Normal mode | 7 bits or 8 bits | | Asynchronous | 1 bit or 2 bits *2 |
| 1 | Multi processor mode | 8 + 1 *1 | — | Asynchronous | |
| 2 | Normal mode | 8 | — | Synchronous | No |

— : Setting disabled

*1 : + 1 is an address/data setting bit (A/D) which is used for communication control.

*2 : Only one bit can be detected as a stop bit at reception.

• Register list

Serial mode register (SMR0, SMR1)

Address : 000020H / 000026H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MD1 | MD0 | SCKL | M2L2 | M2L1 | M2L0 | SCKE | SOE |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00100000B

Serial control register (SCR0, SCR1)

Address : 000021H / 000027H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| PEN | P | SBL | CL | A/D | REC | RXE | TXE |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( W ) | ( R/W ) | ( R/W ) |

Initial Value 00000100B

Serial input/output register (SIDR0, SIDR1 / SODR0, SODR1)

Address : 000022H / 000028H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value XXXXXXXXB

Serial data register (SSR0, SSR1)

Address : 000023H / 000029H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| PE | ORE | FRE | RDRF | TDRE | BDS | RIE | TIE |
| ( R ) | ( R ) | ( R ) | ( R ) | ( R ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00001000B

UART prescaler reload register (UTRLR0, UTRLR1)

Address : 000024H / 00002AH

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000000B

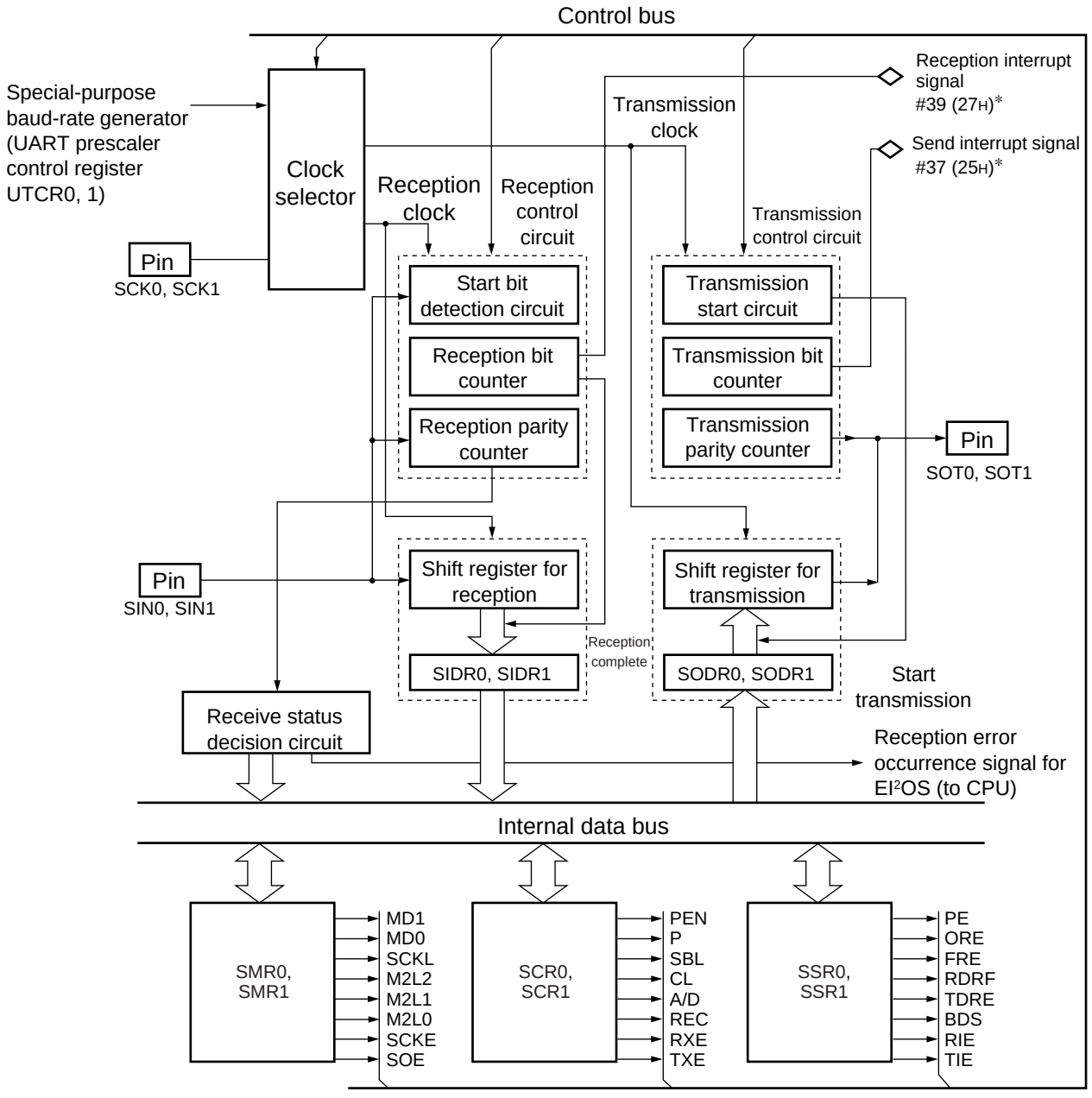
UART prescaler control register (UTCR0, UTCR1)

Address : 000025H / 00002BH

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| MD | SRST | CKS | Reserved | — | D10 | D9 | D8 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( — ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 0000-000B

• Block Diagram




* : Interrupt number

## 7. Extended I/O serial interface

The extended I/O serial interface is a serial I/O interface that can transfer data through the adoption of 8-bit × 1 channel configured clock synchronization scheme. LSB-first or MSB-first transfer mode can be selected for data transfer.

There are two serial I/O operation modes available:

- Internal shift clock mode: Transfer data in synchronization with the internal clock.
- External shift clock mode: Transfer data in synchronization with the clock supplied via the external pin (SCK). By manipulating the general-purpose port sharing the external pin (SCK) in this mode, data can also be transferred by a CPU instruction.

• Register list

Serial mode control status register (SMCS)

Address : 000059H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| SMD2 | SMD1 | SMD0 | SIE | SIR | BUSY | STOP | STRT |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000010B

Address : 000058H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | MODE | BDS | SOE | SCOE |
| ( — ) | ( — ) | ( — ) | ( — ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value XXXX0000B

Serial data register (SDR)

Address : 00005AH

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value XXXXXXXXB

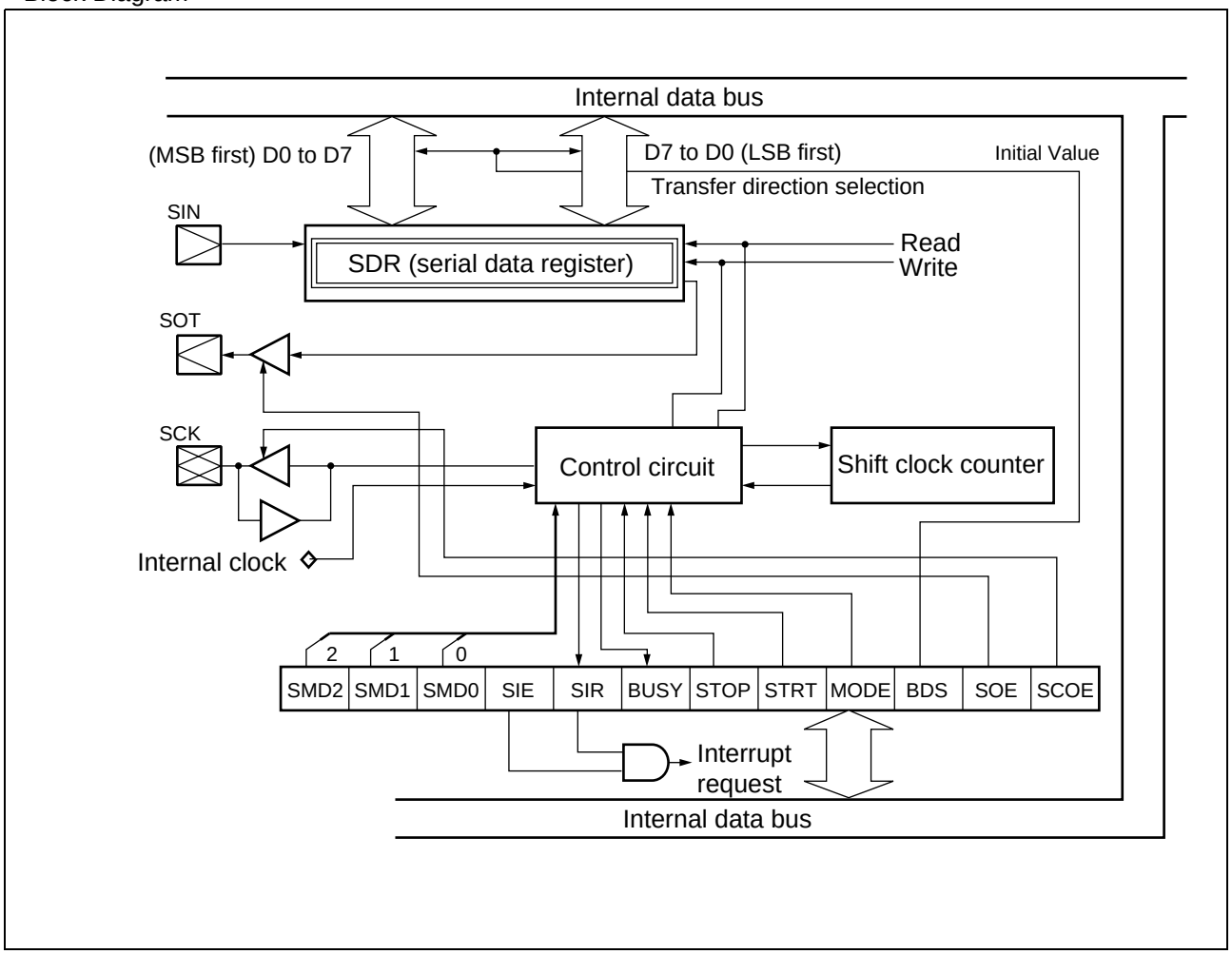
Communication prescaler control register (SDCR)

Address : 00005BH

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| MD | — | — | — | DIV3 | DIV2 | DIV1 | DIV0 |
| ( R/W ) | ( — ) | ( — ) | ( — ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 0XXX0000B

• Block Diagram



## 8. I²C Interface

The I²C interface is a serial I/O port supporting the Inter IC BUS. It serves as a master/slave device on the I²C bus and has the following features.

- Master/slave sending and receiving
- Arbitration function
- Clock synchronization function
- Slave address and general call address detection function
- Detecting transmitting direction function
- Start condition repeated generation and detection function
- Bus error detection function

• Register list

I²C bus status register (IBSR0)

Address : 000070H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BB | RSC | AL | LRB | TRX | AAS | GCA | FBT |
| ( R ) | ( R ) | ( R ) | ( R ) | ( R ) | ( R ) | ( R ) | ( R ) |

Initial Value 00000000B

I²C bus control register (IBCR0)

Address : 000071H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| BER | BEIE | SCC | MSS | ACK | GCAA | INTE | INT |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000000B

I²C bus clock selection register (ICCR0)

Address : 000072H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| — | — | EN | CS4 | CS3 | CS2 | CS1 | CS0 |
| ( — ) | ( — ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value XXX0XXXXB

I²C bus address register (IADR0)

Address : 000073H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| — | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| ( — ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value XXXXXXXXB

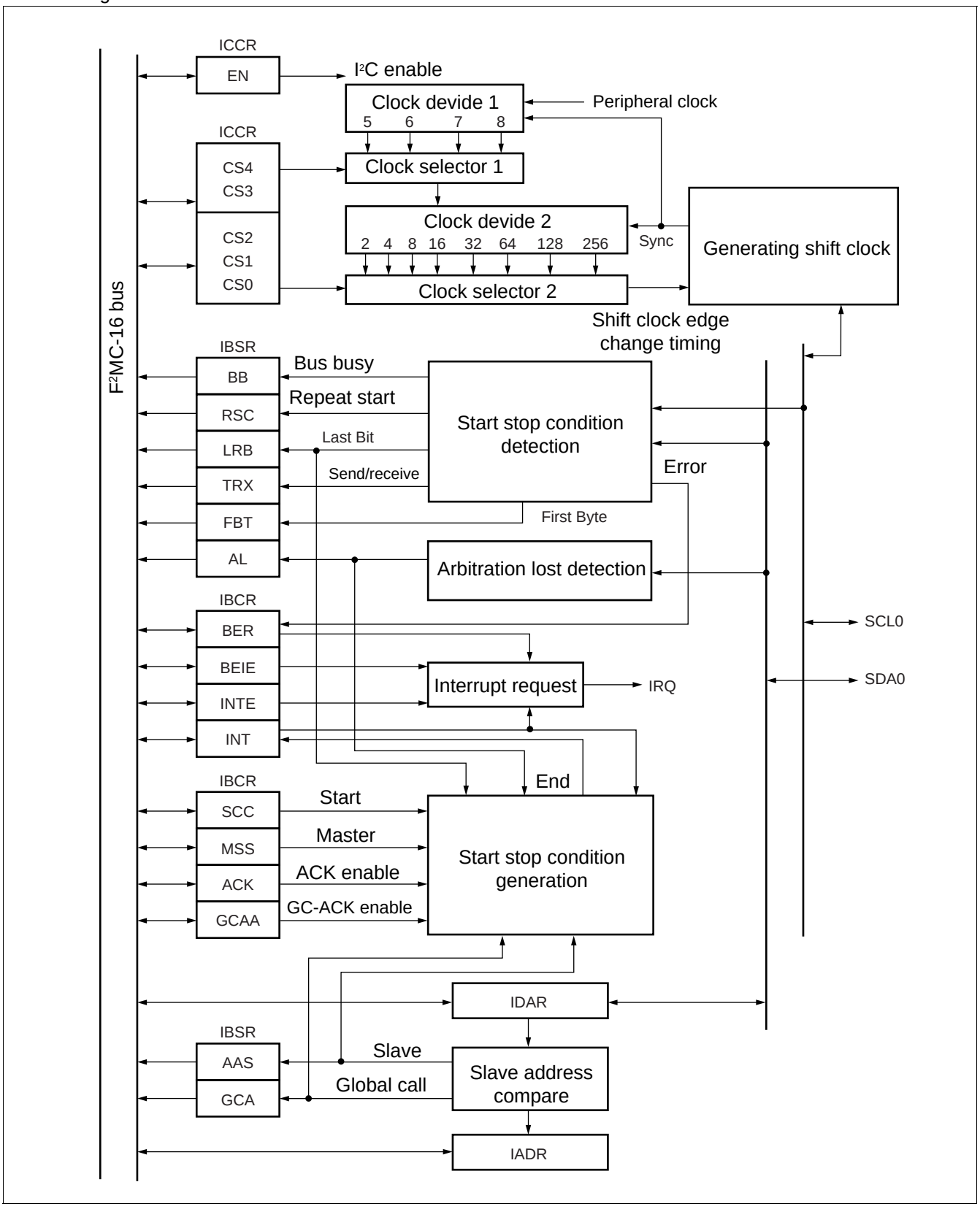
I²C bus data register (IDAR0)

Address : 000074H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value XXXXXXXXB

• Block Diagram



## 9. USB Function

The USB is an interface supporting the USB (Universal Serial Bus) communications protocol.

Feature of USB function

- Conform to USB 2.0 Full Speed
- FULL speed (12 Mbps) is supported.
- The device status is auto-answer.
- Bit stripping, bit stuffing, and automatic generation and check of CRC5 and CRC16.
- Toggle check by data synchronization bit.
- Automatic response to all standard commands except Get/SetDescriptor and SynchFrame commands (these three commands can be processed the same way as the class vendor commands).
- The class vendor commands can be received as data and responded via firmware.
- Supports up to maximum six EndPoints (EndPoint0 is fixed to control transfer).
- Two transfer data buffers integrated for each end point (one IN buffer and one OUT buffer for end point 0).
- Supports automatic transfer mode for transfer data via DMA (except buffers for EndPoint0).
- Capable of detection of connection and disconnection by monitoring the USB bus power line.

• Register list

UDC control register (UDCC)

Address : 0000D0H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|
| RST | RESUM | HCONX | USTP | Reserved | Reserved | RFBK | PWC | 10100000B |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | |

EP0 control register (EP0C)

Address : 0000D2H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|
| Reserved | PKS0 | PKS0 | PKS0 | PKS0 | PKS0 | PKS0 | PKS0 | X1000000B |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | |

Address : 0000D3H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|
| — | — | — | — | Reserved | Reserved | STAL | Reserved | XXXX0000B |
| ( — ) | ( — ) | ( — ) | ( — ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | |

EP1 control register (EP1C)

Address : 0000D4H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|
| PKS1 | PKS1 | PKS1 | PKS1 | PKS1 | PKS1 | PKS1 | PKS1 | 00000000B |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | |

Address : 0000D5H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|
| EPEN | TYPE | TYPE | DIR | DMAE | NULE | STAL | PKS1 | 01100001B |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | |

*(Continued)*

EP2/3/4/5 control register (EP2C ～ EP5C)

Address : 0000D6H, 0000D8H, 0000DAH, 0000DCH

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|
| Reserved | PKS2~5 | PKS2~5 | PKS2~5 | PKS2~5 | PKS2~5 | PKS2~5 | PKS2~5 | 01000000B |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | |

Address : 0000D7H, 0000D9H, 0000DBH, 0000DDH

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|
| EPEN | TYPE | TYPE | DIR | DMAE | NULE | STAL | Reserved | 01100000B |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | |

Time stamp register (TMSP)

Address : 0000DEH

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|
| TMSP | TMSP | TMSP | TMSP | TMSP | TMSP | TMSP | TMSP | 00000000B |
| ( R ) | ( R ) | ( R ) | ( R ) | ( R ) | ( R ) | ( R ) | ( R ) | |

Address : 0000DFH

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|
| — | — | — | — | — | TMSP | TMSP | TMSP | 00000000B |
| ( — ) | ( — ) | ( — ) | ( — ) | ( — ) | ( R ) | ( R ) | ( R ) | |

UDC status register (UDCS)

Address : 0000E0H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|
| VOFF | VON | SUSP | SOF | BRST | WKUP | SETP | CONF | 00000000B |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | |

Interrupt enable register (UDCIE)

Address : 0000E1H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|
| VOFFIE | VONIE | SUSPIE | SOFIE | BRSTIE | WKUPIE | CONFN | CONFIE | 00000000B |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R ) | ( R/W ) | |

EP0I status register (EP0IS)

Address : 0000E2H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — | XXXXXXXXB |
| ( — ) | ( — ) | ( — ) | ( — ) | ( — ) | ( — ) | ( — ) | ( — ) | |

Address : 0000E3H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|
| BFINI | DRQIIE | — | — | — | DRQI | — | — | 10XXX1XXB |
| ( R/W ) | ( R/W ) | ( — ) | ( — ) | ( — ) | ( R/W ) | ( — ) | ( — ) | |

*(Continued)*

*(Continued)*

EP0O status register (EP0OS)

Address : 0000E4H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| — | SIZE | SIZE | SIZE | SIZE | SIZE | SIZE | SIZE |
| (—) | (R) | (R) | (R) | (R) | (R) | (R) | (R) |

Initial Value XXXXXXXXB

Address : 0000E5H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| BFINI | DRQOIE | SPKIE | — | — | DRQO | SPK | — |
| (R/W) | (R/W) | (R/W) | (—) | (—) | (R/W) | (R/W) | (—) |

Initial Value 100XX00XB

EP1 status register (EP1S)

Address : 0000E6H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SIZE | SIZE | SIZE | SIZE | SIZE | SIZE | SIZE | SIZE |
| (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) |

Initial Value XXXXXXXXB

Address : 0000E7H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| BFINI | DRQIE | SPKIE | — | BUSY | DRQ | SPK | SIZE |
| (R/W) | (R/W) | (R/W) | (—) | (R) | (R/W) | (R/W) | (R/W) |

Initial Value 1000000XB

EP2/3/4/5 status register (EP2S to EP5S)

Address : 0000E8H, 0000EAH, 0000ECH, 0000EEH

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| — | SIZE | SIZE | SIZE | SIZE | SIZE | SIZE | SIZE |
| (—) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) |

Initial Value XXXXXXXXB

Address : 0000E9H, 0000EBH, 0000EDH, 0000EFH

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| BFINI | DRQIE | SPKIE | — | BUSY | DRQ | SPK | — |
| (R/W) | (R/W) | (R/W) | (—) | (R) | (R/W) | (R/W) | (—) |

Initial Value 1000000XB

EP0/1/2/3/4/5 data register (EP0DT to EP5DT)

Address : 0000F0H, 0000F2H, 0000F4H, 0000F6H, 0000F8H, 0000FAH

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BFDT | BFDT | BFDT | BFDT | BFDT | BFDT | BFDT | BFDT |
| (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) |

Initial Value XXXXXXXXB

Address : 0000F1H, 0000F3H, 0000F5H, 0000F7H, 0000F9H, 0000FBH

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| BFDT | BFDT | BFDT | BFDT | BFDT | BFDT | BFDT | BFDT |
| (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) |

Initial Value XXXXXXXXB

## 10. USB Mini-HOST

USB Mini-HOST provides minimal host operations required and is a function that enables data to be transferred to and from Device without PC intervention.

**Feature of USB Mini-HOST**

- Automatic detection of Low Speed/Full Speed transfer
- Low Speed/Full Speed transfer support
- Automatic detection of connection and cutting device
- Reset sending function support to USB-bus
- Support of IN/OUT/SETUP/SOF token
- In-token handshake packet automatic transmission (excluding STALL)
- Handshake packet automatic detection at out-token
- Supports a maximum packet length of 256 bytes
- Error (CRC error/toggle error/time-out) various supports
- Wake-Up function support

**Differences between the USB HOST and USB Mini-HOST**

| | | HOST | Mini-HOST |
|---|---|---|---|
| Hub support | | ○ | × |
| Transfer | Bulk transfer | ○ | ○ |
| | Control transfer | ○ | ○ |
| | Interrupt transfer | ○ | ○ |
| | ISO transfer | ○ | × |
| Transfer speed | Low Speed | ○ | ○ |
| | Full Speed | ○ | ○ |
| PRE packet support | | ○ | × |
| SOF packet support | | ○ | ○ |
| Error | CRC error | ○ | ○ |
| | Toggle error | ○ | ○ |
| | Time-out | ○ | ○ |
| | Maximum packet < receive data | ○ | ○ |
| Detection of connection and cutting of device | | ○ | ○ |
| Transfer speed detection | | ○ | ○ |

○ : Supported
× : Not supported

• Register list

USB HOST control register 0 (HCONT0)

Address : 0000C0H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RWKIRE | URIRE | CMPIRE | CNNIRE | DIRE | SOFIRE | URST | HOST |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000000B

USB HOST control register 1 (HCONT1)

Address : 0000C1H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | Reserved | Reserved | SOFSTEP | CANCEL | RETRY |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000001B

USB HOST interruption register (HIRQ)

Address : 0000C2H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TCAN | Reserved | RWKIRQ | URIRQ | CMPIRQ | CNNIRQ | DIRQ | SOFIRQ |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000000B

USB HOST error status register (HERR)

Address : 0000C3H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| LSTSOF | RERR | TOUT | CRC | TGERR | STUFF | HS | HS |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000011B

USB HOST state status register (HSTATE)

Address : 0000C4H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| — | — | ALIVE | CLKSEL | SOFBUSY | SUSP | TMODE | CSTAT |
| ( — ) | ( — ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R ) | ( R ) |

Initial Value XX010010B

USB SOF interruption FRAME comparison register (HFCOMP)

Address : 0000C5H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| FRAME COMP | FRAME COMP | FRAME COMP | FRAME COMP | FRAME COMP | FRAME COMP | FRAME COMP | FRAME COMP |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000000B

USB retry timer setting register 0/1/2 (HRTIMER)

Address : 0000C6H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RTIMER0 | RTIMER0 | RTIMER0 | RTIMER0 | RTIMER0 | RTIMER0 | RTIMER0 | RTIMER0 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000000B

Address : 0000C7H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RTIMER1 | RTIMER1 | RTIMER1 | RTIMER1 | RTIMER1 | RTIMER1 | RTIMER1 | RTIMER1 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000000B

Address : 0000C8H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | RTIMER2 | RTIMER2 |
| ( — ) | ( — ) | ( — ) | ( — ) | ( — ) | ( — ) | ( R/W ) | ( R/W ) |

Initial Value XXXXXX00B

*(Continued)*

*(Continued)*

USB HOST address register (HADR)

Address : 0000C9H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| — | ADDRESS | ADDRESS | ADDRESS | ADDRESS | ADDRESS | ADDRESS | ADDRESS |
| ( — ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value X0000000B

USB EOF setting register 0/1 (HEOF)

Address : 0000CAH

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EOF0 | EOF0 | EOF0 | EOF0 | EOF0 | EOF0 | EOF0 | EOF0 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000000B

Address : 0000CBH

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| — | — | EOF1 | EOF1 | EOF1 | EOF1 | EOF1 | EOF1 |
| ( — ) | ( — ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value XX000000B

USB FRAME setting register (HFRAME)

Address : 0000CCH

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FRAME0 | FRAME0 | FRAME0 | FRAME0 | FRAME0 | FRAME0 | FRAME0 | FRAME0 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000000B

Address : 0000CDH

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | FRAME1 | FRAME1 | FRAME1 |
| ( — ) | ( — ) | ( — ) | ( — ) | ( — ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value XXXXX000B

USB token end point register (HTOKEN)

Address : 0000CEH

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TGGL | TKNEN | TKNEN | TKNEN | ENDPT | ENDPT | ENDPT | ENDPT |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000000B

## 11. DTP/external interrupt circuit

### Feature of DTP/external interrupt circuit

DTP (Data Transfer Peripheral)/external interrupt circuit detects the interrupt request input from the external interrupt input terminal INT7 to INT0, and outputs the interrupt request.

- DTP/external interrupt circuit function

  The DTP/external interrupt function outputs an interrupt request upon detection of the edge or level signal input to the external interrupt input pins (INT7 to INT0).

  If CPU accept the interrupt request, and if the extended intelligent I/O service (EI$^2$OS) is enabled, branches to the interrupt handling routine after completing the automatic data transfer (DTP function) performed by EI$^2$OS. And if EI$^2$OS is disabled, it branches to the interrupt handling routine without activating the automatic data transfer (DTP function) performed by EI$^2$OS.

- **Feature of DTP/external interrupt circuit**

| | External interrupt | DTP function |
|---|---|---|
| Input pin | 8 channels (P60/INT0, P61/INT1, P62/INT2/SIN, P63/INT3/SOT, P64/INT4/SCK, P65/INT5/PWC, P66/INT6/SCL0, P67/INT7/SDA0) | |
| Interrupt source | The detection level or the type of the edge for each terminals can be set in the request level setting register (ELVR) | |
| | Input of “H” level/ “L” level/rising edge/falling edge. | |
| Interrupt number | #18 ($12_H$) , #20 ($14_H$) , #22 ($16_H$) , #24 ($18_H$) | |
| Interrupt control | Enabling/Prohibit the interrupt request output using the DTP/interrupt enable register (ENIR) | |
| Interrupt flag | Holding the interrupt source using the DTP/interrupt cause register (EIRR) | |
| Process setting | Prohibit EI$^2$OS (ICR: ISE=“0”) | Enable EI$^2$OS (ICR: ISE=“1”) |
| Process | Branched to the interrupt handling routine | After an automatic data transfer by EI$^2$OS, Branched to the interrupt handling routine |

- Register list

Interrupt/DTP enable register (ENIR)

Address : $00003C_H$

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EN7 | EN6 | EN5 | EN4 | EN3 | EN2 | EN1 | EN0 |
| (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) |

Initial Value $00000000_B$

Interrupt/DTP source register (EIRR)

Address : $00003D_H$

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| ER7 | ER6 | ER5 | ER4 | ER3 | ER2 | ER1 | ER0 |
| (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) |

Initial Value $00000000_B$

Request level setting register (ELVR)

Address : $00003E_H$

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LB3 | LA3 | LB2 | LA2 | LB1 | LA1 | LB0 | LA0 |
| (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) |

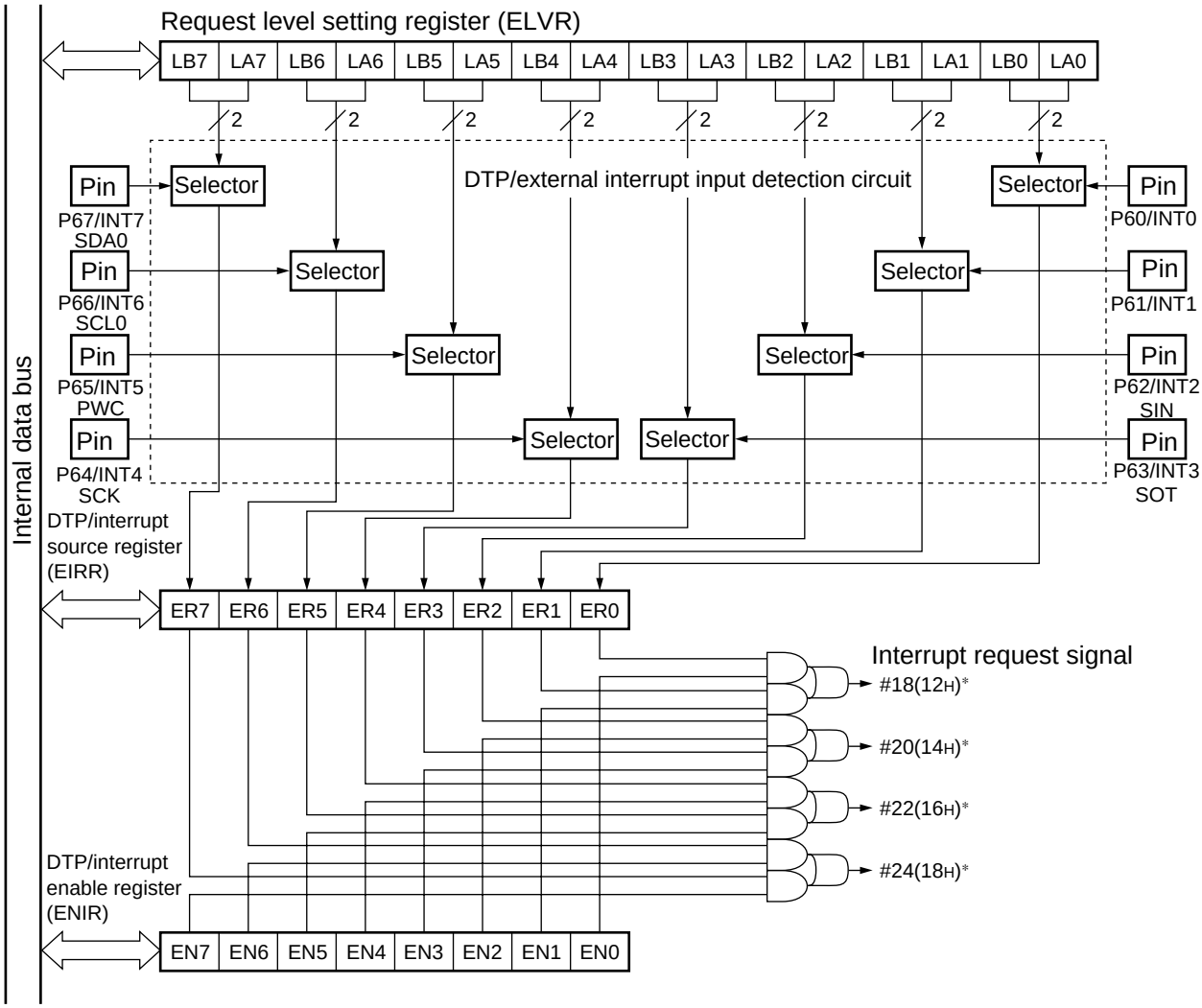
Initial Value $00000000_B$

Address : $00003F_H$

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| LB7 | LA7 | LB6 | LA6 | LB5 | LA5 | LB4 | LA4 |
| (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) |

Initial Value $00000000_B$

• Block Diagram




* : Interrupt number

## 12. Interrupt controller

The interrupt control register is located inside the interrupt controller, it exists for every I/O having an interrupt function. This register has the following functions.

- Setting of the interrupt levels of relevant peripheral

**• Register list**

Interrupt control register

Address : ICR01 : 0000B1H
ICR03 : 0000B3H
ICR05 : 0000B5H
ICR07 : 0000B7H
ICR09 : 0000B9H
ICR11 : 0000BBH
ICR13 : 0000BDH
ICR15 : 0000BFH

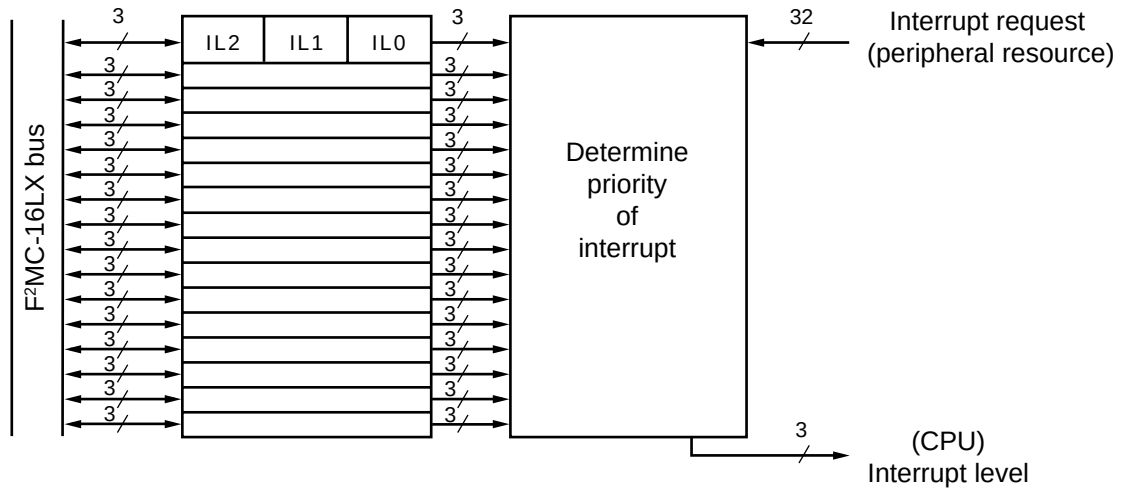
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | |
|---|---|---|---|---|---|---|---|---|---|
| | ICS3 | ICS2 | ICS1 | ICS0 | ISE | IL2 | IL1 | IL0 | ICR01, 03, 05, 07, 09, 11, 13, 15 |
| Read/Write → | ( W ) | ( W ) | ( W ) | ( W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | |
| Initial Value → | ( 0 ) | ( 0 ) | ( 0 ) | ( 0 ) | ( 0 ) | ( 1 ) | ( 1 ) | ( 1 ) | |

Address : ICR00 : 0000B0H
ICR02 : 0000B2H
ICR04 : 0000B4H
ICR06 : 0000B6H
ICR08 : 0000B8H
ICR10 : 0000BAH
ICR12 : 0000BCH
ICR14 : 0000BEH

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| | ICS3 | ICS2 | ICS1 | ICS0 | ISE | IL2 | IL1 | IL0 | ICR00, 02, 04, 06, 08, 10, 12, 14 |
| Read/Write → | ( W ) | ( W ) | ( W ) | ( W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | |
| Initial Value → | ( 0 ) | ( 0 ) | ( 0 ) | ( 0 ) | ( 0 ) | ( 1 ) | ( 1 ) | ( 1 ) | |

Note : Do not access interrupt control registers using any read modify write instruction because it causes a malfunction.

• Block Diagram



## 13. µDMAC

µDMAC is simple DMA with the function equal with EI²OS. It has 16 channels DMA transfer channels with the following features.

- Performs automatic data transfer between the peripheral resource (I/O) and memory
- The program execution of CPU stops in the DMA startup
- Capable of selecting whether to increment the transfer source and destination addresses
- DMA transfer is controlled by the DMA enable register, DMA stop status register, DMA status register and descriptor
- A STOP request is available for stopping DMA transfer from the resource
- Upon completion of DMA transfer, the flag bit corresponding to the transfer completed channel in the DMA status register is set and a termination interrupt is output to the transfer controller.

• Register list

DMA enable register higher (DERH)

Address : 0000AD$_H$

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| EN15 | EN14 | EN13 | EN12 | EN11 | EN10 | EN9 | EN8 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000000$_B$

DMA enable register lower (DERL)

Address : 0000AC$_H$

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EN7 | EN6 | EN5 | EN4 | EN3 | EN2 | EN1 | EN0 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000000$_B$

DMA stop status register (DSSR)

Address : 0000A4$_H$

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| STP7<br>STP15 | STP6<br>STP14 | STP5<br>STP13 | STP4<br>STP12 | STP3<br>STP11 | STP2<br>STP10 | STP1<br>STP9 | STP0<br>STP8 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000000$_B$ *

DMA status register higher (DSRH)

Address : 00009D$_H$

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| DTE15 | DTE14 | DTE13 | DTE12 | DTE11 | DTE10 | DTE9 | DTE8 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000000$_B$

DMA status register lower (DSRL)

Address : 00009C$_H$

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTE7 | DTE6 | DTE5 | DTE4 | DTE3 | DTE2 | DTE1 | DTE0 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000000$_B$

DMA descriptor channel specification register (DCSR)

Address : 00009B$_H$

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| STP | Reserved | Reserved | Reserved | DCSR3 | DCSR2 | DCSR1 | DCSR0 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value 00000000$_B$

* : The DSSR is lower when the STP bit of DCSR in the DSSR is 0.
The DSSR is upper when the STP bit of DCSR in the DSSR is 1.

*(Continued)*

*(Continued)*

DMA buffer address pointer lower 8 bit (DBAPL)

Address : 007920H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DBAPL | DBAPL | DBAPL | DBAPL | DBAPL | DBAPL | DBAPL | DBAPL |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value XXXXXXXXB

DMA buffer address pointer middle 8 bit (DBAPM)

Address : 007921H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| DBAPM | DBAPM | DBAPM | DBAPM | DBAPM | DBAPM | DBAPM | DBAPM |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value XXXXXXXXB

DMA Buffer address pointer higher 8 bit (DBAPH)

Address : 007922H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DBAPH | DBAPH | DBAPH | DBAPH | DBAPH | DBAPH | DBAPH | DBAPH |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value XXXXXXXXB

DMA control register (DMACS)

Address : 007923H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RDY2 | RDY1 | BYTEL | IF | BW | BF | DIR | SE |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value XXXXXXXXB

DMA I/O register address pointer lower 8 bit (DIOAL)

Address : 007924H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| A07 | A06 | A05 | A04 | A03 | A02 | A01 | A00 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value XXXXXXXXB

DMA I/O register address pointer higher 8 bit (DIOAH)

Address : 007925H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| A15 | A14 | A13 | A12 | A11 | A10 | A09 | A08 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value XXXXXXXXB

DMA data counter lower 8 bit (DDCTL)

Address : 007926H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| B07 | B06 | B05 | B04 | B03 | B02 | B01 | B00 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value XXXXXXXXB

DMA data counter higher 8 bit (DDCTH)

Address : 007927H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| B15 | B14 | B13 | B12 | B11 | B10 | B09 | B08 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value XXXXXXXXB

Note : The above register is switched for each channel depending on the DCSR.

## 14. Address matching detection function

When the address is equal to the value set in the address detection register, the instruction code to be read into the CPU is forcibly replaced with the INT9 instruction code (01H). As a result, the CPU executes the INT9 instruction when executing the set instruction. By performing processing by the INT#9 interrupt routine, the program patch function is enabled.
Two address detection registers are provided, for each of which there is an interrupt enable bit. When the address matches the value set in the address detection register with the interrupt enable bit set to 1, the instruction code to be read into the CPU is forcibly replaced with the INT9 instruction code.

• Register list

• Program address detect register 0 to 2 (PADR0)

PADR0 (lower)
Address : 001FF0H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) |

Initial Value
XXXXXXXXB

PADR0 (middle)
Address : 001FF1H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) |

Initial Value
XXXXXXXXB

PADR0 (higher)
Address : 001FF2H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) |

Initial Value
XXXXXXXXB

• Program address detect register 3 to 5 (PADR1)

PADR1 (lower)
Address : 001FF3H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) |

Initial Value
XXXXXXXXB

PADR1 (middle)
Address : 001FF4H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) |

Initial Value
XXXXXXXXB

PADR1 (higher)
Address : 001FF5H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) |

Initial Value
XXXXXXXXB

• Program address detect control status register (PACSR)

PACSR
Address : 00009EH

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | Reserved | AD1E | Reserved | AD0E | Reserved |
| (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) |

Initial Value
00000000B

R/W : Readable and Writable
X : Undefined

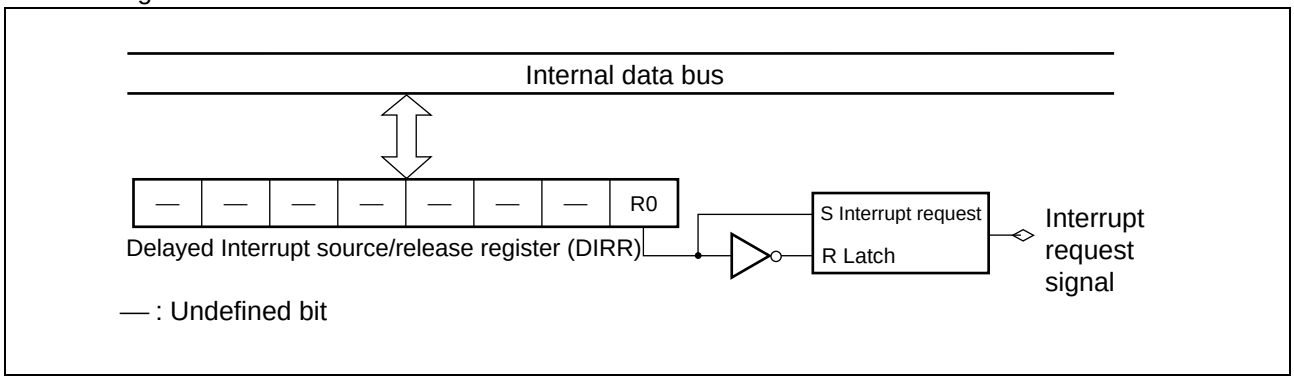
## 15. Delay interrupt generator module

- The delay interrupt generation module is a module that generates interrupts for switching tasks. A hardware interrupt can be generated by software.

**• Function of delay interrupt generator module**

| | Function and control |
|---|---|
| Interrupt source | • Setting the R0 bit in the delayed interrupt request generate/cancel register to 1 (DIRR: R0 = 1) generates a interrupt request.<br>• Setting the R0 bit in the delayed interrupt request generate/cancel register to 0 (DIRR: R0 = 0) cancels the interrupt request. |
| Interrupt control | • No setting of permission register is provided. |
| Interrupt flag | • Set in bit R0 of the delayed interrupt request generation/clear register (DIRR : R0) |
| EI²OS support | • Not ready for expanded intelligent I/O service (EI²OS). |

• Block Diagram



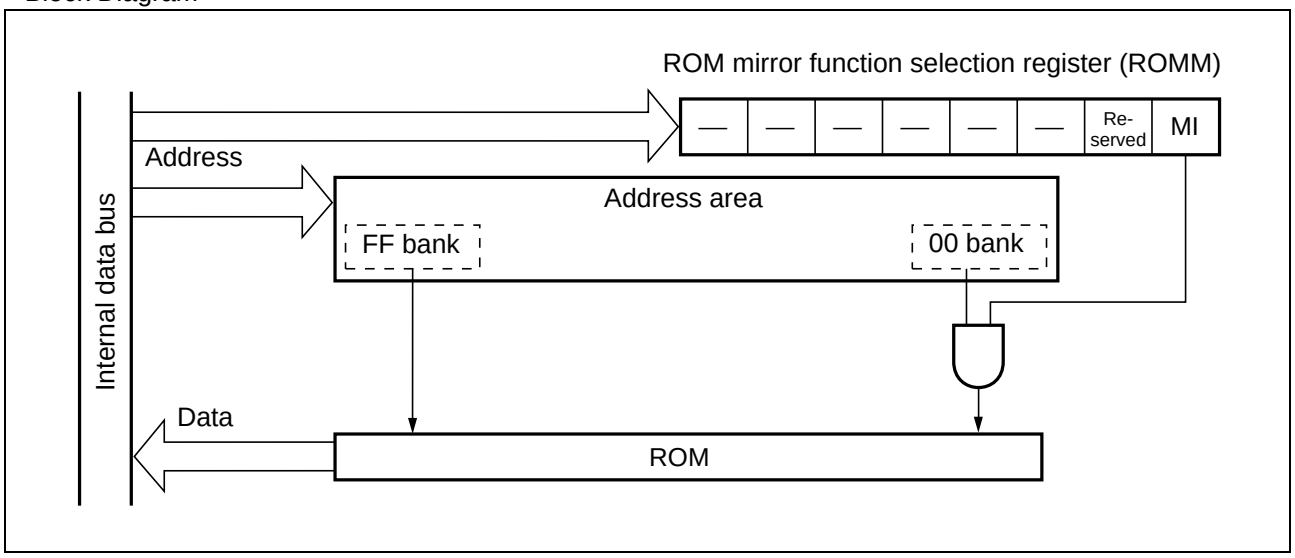
## 16. ROM mirroring function selection module

- The ROM mirror function select module can make a setting so that ROM data located in bank FF can be read by accessing bank 00.

**• ROM mirroring function selection module**

| | Description |
|---|---|
| Mirror setting address | FFFFFF$_H$ to FF8000$_H$ in the FF bank can be read through 00FFFF$_H$ to 008000$_H$ in the 00 bank. |
| Interrupt source | • None |
| EI$^2$OS support | • Not ready for extended intelligent I/O service (EI$^2$OS). |

• Block Diagram



## 17. Low power consumption (standby) mode

- The F²MC-16LX can be set to save power consumption by selecting and setting the low power consumption mode.

**• CPU operation mode and functional description**

| CPU operating clock | Operation mode | Description |
|---|---|---|
| PLL clock | Normally run | The CPU and peripheral resources operate at the clock frequency obtained by PLL multiplication of the oscillator clock (HCLK) frequency. |
| | Sleep | Only peripheral resources operate at the clock frequency obtained by PLL multiplication of the oscillator clock (HCLK) frequency. |
| | Time-base timer | Only the time-base timer operates at the clock frequency obtained by PLL multiplication of the oscillator clock (HCLK) frequency. |
| | Stop | The CPU and peripheral resources are suspended with the oscillator clock stopped. |
| Main clock | normally run | The CPU and peripheral resources operate at the clock frequency obtained by dividing the oscillator clock (HCLK) frequency by two. |
| | Sleep | Only peripheral resources operate at the clock frequency obtained by dividing the oscillator clock (HCLK) frequency by two. |
| | Time-base timer | Only the time-base timer operates at the clock frequency obtained by dividing the oscillator clock (HCLK) frequency by two. |
| | Stop | The CPU and peripheral resources are suspended with the oscillator clock stopped. |
| CPU intermittent operation mode | Normally run | The halved or PLL-multiplied oscillator clock (HCLK) frequency is used for operation while being decimated in a certain period. |

• Register list

Lowe power consumption mode control register (LPMCR)

Address : $0000A0_H$

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| STP | SLP | SPL | RST | TMD | CG1 | CG0 | Reserved |
| ( W ) | ( W ) | ( R/W ) | ( W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value
$00011000_B$

## 18. Clock

The clock generator controls the internal clock as the operating clock for the CPU and peripheral resources. The internal clock is referred to as machine clock whose one cycle is defined as machine cycle. The clock based on source oscillation is referred to as oscillator clock while the clock based on internal PLL oscillation as PLL clock.

• Register list

Clock selection register (CKSCR)

Address : 0000A1H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| SCM | MCM | WS1 | WS0 | SCS | MCS | CS1 | CS0 |
| ( R ) | ( R ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value
11111100B

## 19. 512 Kbits flash memory

The description that follows applies to the flash memory built in the MB90F334; it is not applicable to evaluation ROM or masked ROM.

The method of data write/erase to flash memory is following three types.

- Parallel writer
- Serial dedicated writer
- Write/erase by executing program

• Description of 512 Kbits flash memory

512 Kbits flash memory is located in $FF_H$ bank in the CPU memory map. Function of flash memory interface circuit enables read and program access from CPU.
Write/erase to flash interface is executed by instruction from CPU via flash memory interface, so rewrite of program and data is carried on in the mounting state effectively.

Data can be reprogrammed not only by program execution in existing RAM but by program execution in flash memory by dual operation. The different banks (the upper and lower banks) can be used to execute an erase/program and a read concurrently.
Also, erase/write and read in the defferent bank (Upper Bank/Lower Bank) is executed simultaneously.

• Features of 512 Kbits flash memory

- Sector configuration : 64 Kwords $\times$ 8 bits/32 words $\times$ 16 bits (4K $\times$ 4 + 16K $\times$ 2 + 4K $\times$ 4)
- Simultaneous execution of erase/write and read by 2-bank configuration
- Automatic program algorithm (Embeded Algorithm™*)
- Built-in deletion pause/deletion resume function
- Detection of programming/erasure completion using data polling and the toggle bit
- At least 10,000 times guaranteed
- Minimum flash read cycle time : 2 machine cycles

* : Embedded Algorithm™ is a trade mark of Advanced Micro Devices Inc.

Note : The read function of manufacture code and device coad is not including.
Also, these code is not accessed by the command.

- Flash write/erase
- Flash memory can not execute write/erase and read by the same bank simultaneously.
- Data can be programmed/deleted into and erased from flash memory by executing either the program residing in the flash memory or the one copied to RAM from the flash memory.

• Sector configuration of flash memoly

| Flash Memory | CPU address | Writer address * | |
|---|---|---|---|
| SA0 (4 Kbyte) | FF0000H<br>FF0FFFH | 70000H<br>70FFFH | Lower Bank |
| SA1 (4 Kbyte) | FF1000H<br>FF1FFFH | 71000H<br>71FFFH | |
| SA2 (4 Kbyte) | FF2000H<br>FF2FFFH | 72000H<br>72FFFH | |
| SA3 (4 Kbyte) | FF3000H<br>FF3FFFH | 73000H<br>73FFFH | |
| SA4 (16 Kbyte) | FF4000H<br>FF7FFFH | 74000H<br>77FFFH | Upper Bank |
| SA5 (16 Kbyte) | FF8000H<br>FFBFFFH | 78000H<br>78FFFH | |
| SA6 (4 Kbyte) | FFC000H<br>FFCFFFH | 7C000H<br>7CFFFH | |
| SA7 (4 Kbyte) | FFD000H<br>FFDFFFH | 7D000H<br>7DFFFH | |
| SA8 (4 Kbyte) | FFE000H<br>FFEFFFH | 7E000H<br>7EFFFH | |
| SA9 (4Kbyte) | FFF000H<br>FFFFFFH | 7F000H<br>7FFFFH | |

* : Flash memory writer address indicates the address equivalent to the CPU address when data is written to the flash memory using a parallel writer. Programming and erasing by the general-purpose parallel programmer are executed based on writer addresses.

• Register list

Flash memory control register (FMCS)

Address : 0000AE$_H$

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| INTE | RDYINT | WE | RDY | Reserved | LPM1 | Reserved | LPM0 |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R ) | ( W ) | ( R/W ) | ( W ) | ( R/W ) |

Initial Value
000X0000$_B$

Flash memory program control register (FWR0)

Address : 00790C$_H$

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SA7E | SA6E | SA5E | SA4E | SA3E | SA2E | SA1E | SA0E |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value
00000000$_B$

Flash memory program control register (FWR1)

Address : 00790D$_H$

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | SA9E | SA8E |
| ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) | ( R/W ) |

Initial Value
00000000$_B$

Sector conversion setting register (SSR0)

Address : 00790E$_H$

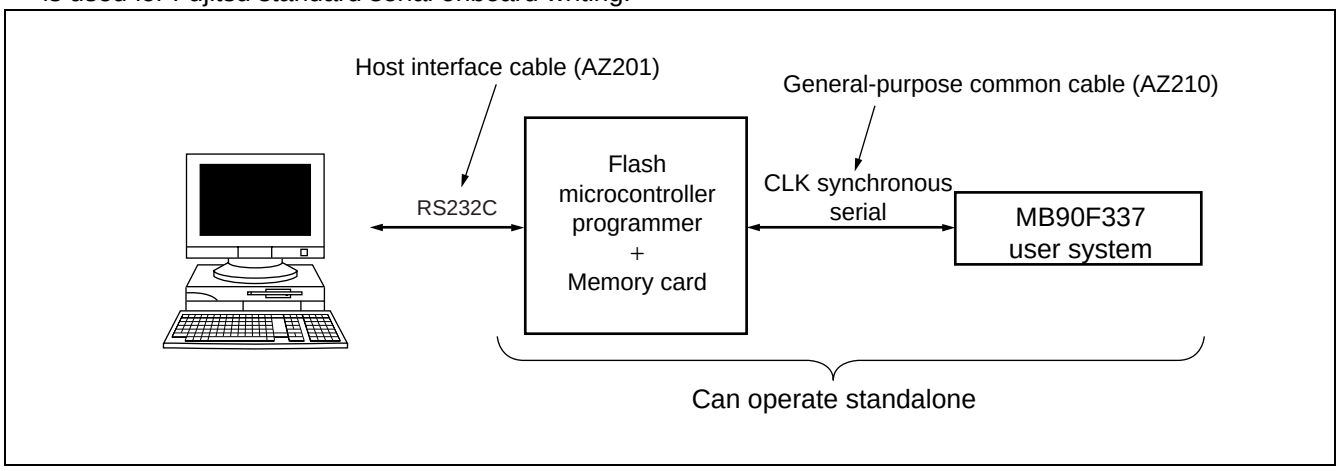
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | SEN0 |
| ( R/W ) | ( R/W ) | ( — ) | ( — ) | ( — ) | ( — ) | ( — ) | ( R/W ) |

Initial Value
00XXXXX0$_B$

* When writing to SSR0 register, write “0” except for SEN0.

• Standard configuration for Fujitsu standard serial on-board writing

The flash microcontroller programmer (AF220/AF210/AF120/AF110) made by Yokogawa Digital Computer Corp. is used for Fujitsu standard serial onboard writing.

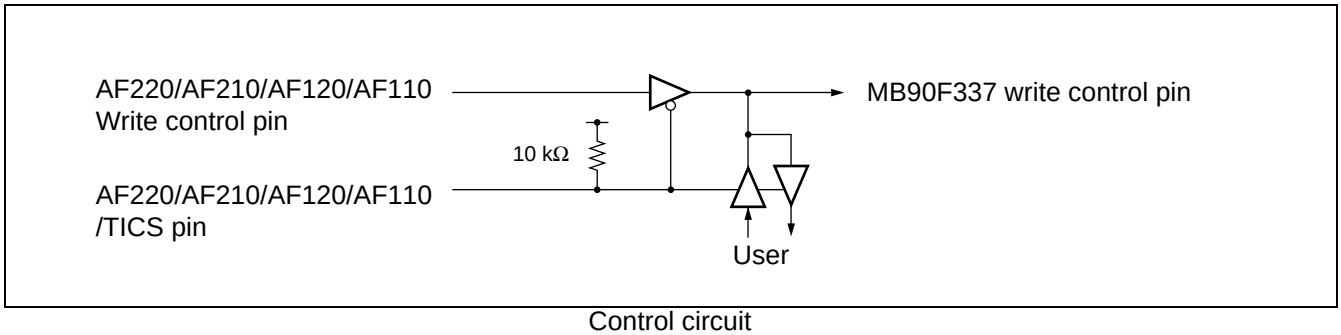



Note : Inquire of Yokogawa Digital Computer Corporation for details about the functions and operations of the flash microcontroller programmer (AF220, AF210, AF120 and AF110) , general-purpose common cable for connection (AZ210) and connectors.

• **Pins Used for Fujitsu Standard Serial On-board Programming**

| Pin | Function | Description |
|---|---|---|
| MD2, MD1, MD0 | Mode input pin | The device enters the serial program mode by setting MD2 = 1, MD1 = 1 and MD0 = 0. |
| X0, X1 | Oscillation pin | Because the internal CPU operation clock is set to be the 1 multiplication PLL clock in the serial write mode, the internal operation clock frequency is the same as the oscillation clock frequency. |
| P60, P61 | Write program start pins | Input a Low level to P60 and a High level to P61. |
| $\overline{RST}$ | Reset input pin | — |
| SIN0 | Serial data input pin | UART0 is used as CLK synchronous mode. In write mode, the pins used for the UART0 CLK synchronous mode are SIN0, SOT0, and SCK0. |
| SOT0 | Serial data output pin | |
| SCK0 | Serial clock input pin | |
| $V_{CC}$ | Power source input pin | When supplying the write voltage (MB90F337 : 3.3 V±0.3 V) from the user system, connection with the flash microcontroller programmer is not necessary. When connecting, do not short-circuit with the user power supply. |
| $V_{SS}$ | GND Pin | Share GND with the flash microcontroller programmer. |

The control circuit shown in the diagram is required for using the P60, P61, SIN0, SOT0 and SCK0 pins on the user system. Isolate the user circuit during serial on-board writing, with the /TICS signal of the flash microcontroller programmer.




Control circuit

The MB90F337 serial clock frequency that can be input is determined by the following expression • Use the flash microcontroller programmer to change the serial clock input frequency setting depending on the oscillator clock frequency to be used.

Imputable serial clock frequency = 0.125 × oscillation clock frequency.

• Maximum serial clock frequency

| Oscillation clock frequency | Maximum serial clock frequency acceptable to the microcontroller | Maximum serial clock frequency that can be set with the AF220/AF210/ AF120/AF110 | Maximum serial clock frequency that can be set with the AF200 |
|---|---|---|---|
| At 6 MHz | 750 kHz | 500 kHz | 500 kHz |

**• System configuration of the flash microcontroller programmer (AF220/AF210/AF120/AF110) (made by Yokogawa Digital Computer Corp.)**

| Part number | | Function | |
|---|---|---|---|
| Unit | AF220/AC4P | Model with internal Ethernet interface | /100 V to 220 V power adapter |
| | AF210/AC4P | Standard model | /100 V to 220 V power adapter |
| | AF120/AC4P | Single key internal Ethernet interface mode | /100 V to 220 V power adapter |
| | AF110/AC4P | Single key model | /100 V to 220 V power adapter |
| AZ221 | | PC/AT RS232C cable for writer | |
| AZ210 | | Standard target probe (a) length : 1 m | |
| FF201 | | Control module for Fujitsu F²MC-16LX flash microcontroller control module | |
| AZ290 | | Remote controller | |
| /P2 | | 2 MB PC Card (option) FLASH memory capacity to respond to 128 KB | |
| /P4 | | 4 MB PC Card (option) FLASH memory capacity to respond to 512 KB | |

Contact to : Yokogawa Digital Computer Corp. TEL : (81)-42-333-6224

Note : The AF200 flash micon programmer is a retired product, but it can be supported using control module FF201.

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

($V_{CC}$ = 3.3 V, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $V_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 4.0 | V | |
| Input voltage | $V_I$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 4.0 | V | *1 |
| | | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | Nch0.D (Withstand voltage I/O of 5 V) |
| | | – 0.5 | $V_{SS}$ + 4.5 | V | USB I/O |
| Output voltage | $V_O$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 4.0 | V | *1 |
| | | – 0.5 | $V_{SS}$ + 4.5 | V | USB I/O |
| L level maximum output current | $I_{OL1}$ | — | 10 | mA | Other than USB I/O*2 |
| | $I_{OL2}$ | — | 43 | mA | USB I/O*2 |
| L level average output current | $I_{OLAV}$ | — | 3 | mA | *3 |
| L level maximum total output current | $\Sigma I_{OL}$ | — | 60 | mA | |
| L level average total output current | $\Sigma I_{OLAV}$ | — | 30 | mA | *4 |
| H level maximum output current | $I_{OH1}$ | — | – 10 | mA | Other than USB I/O*2 |
| | $I_{OH2}$ | — | – 43 | mA | USB I/O*2 |
| H level average output current | $I_{OHAV}$ | — | – 3 | mA | *3 |
| H level maximum total output current | $\Sigma I_{OH}$ | — | – 60 | mA | |
| H level average total output current | $\Sigma I_{OHAV}$ | — | – 30 | mA | *4 |
| Power consumption | Pd | — | 351 | mW | Target value |
| Operating temperature | $T_A$ | – 40 | + 85 | °C | |
| Storage temperature | Tstg | – 55 | + 150 | °C | |
| | | – 55 | + 125 | °C | USB I/O |

*1 : $V_I$ and $V_O$ must not exceed $V_{CC}$ + 0.3 V. However, if the maximum current to/from an input is limited by some means with external components, the $I_{CLAMP}$ rating supersedes the $V_I$ rating.

*2 : A peak value of an applicable one pin is specified as a maximum output current.

*3 : The average output current specifies the mean value of the current flowing in the relevant single pin during a period of 100 ms.

*4 : The average total output current specifies the mean value of the currents flowing in all of the relevant pins during a period of 100 ms.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

($V_{SS}$ = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $V_{CC}$ | 3.0 | 3.6 | V | At normal operation (At USB is used) |
| | | 2.7 | 3.6 | V | At normal operation (At USB is unused) |
| | | 1.8 | 3.6 | V | Hold state of stop operation |
| Input H level voltage | $V_{IH}$ | 0.7 $V_{CC}$ | $V_{CC}$ + 0.3 | V | CMOS input pin |
| | $V_{IHS}$ | 0.8 $V_{CC}$ | $V_{CC}$ + 0.3 | V | CMOS hysteresis input pin |
| | $V_{IHM}$ | $V_{CC}$ – 0.3 | $V_{CC}$ + 0.3 | V | MD input pin |
| | $V_{IHUSB}$ | 2.0 | $V_{CC}$ + 0.3 | V | USB input pin |
| Input L level voltage | $V_{IL}$ | $V_{SS}$ – 0.3 | 0.3 $V_{CC}$ | V | CMOS input pin |
| | $V_{ILS}$ | $V_{SS}$ – 0.3 | 0.2 $V_{CC}$ | V | CMOS hysteresis input pin |
| | $V_{ILM}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 0.3 | V | MD input pin |
| | $V_{ILUSB}$ | $V_{SS}$ | 0.8 | V | USB input pin |
| Differential input sensitivity | $V_{DI}$ | 0.2 | — | V | USB input pin |
| Differential common mode input voltage range | $V_{CM}$ | 0.8 | 2.5 | V | USB input pin |
| Series resistance | $R_S$ | 25 | 30 | Ω | Recommended value = 27 Ω at using USB |
| Operating temperature | $T_A$ | – 40 | + 85 | °C | At USB is unused |
| | | 0 | + 70 | °C | At USB is used |

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

### 3. DC Characteristics

($T_A$ = – 40 °C to +85 °C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Output H level voltage | $V_{OH}$ | Output pin of other than P60 to P67, HVP, HVM, DVP, DVM | $I_{OH}$ = –4.0 mA | $V_{CC}$ – 0.5 | — | Vcc | V | |
| | | HVP, HVM, DVP, DVM | RL = 15 kΩ ± 5% | 2.8 | — | 3.6 | V | |
| Output L level voltage | $V_{OL}$ | Output pin of other than HVP, HVM, DVP, DVM | $I_{OL}$ = 4.0 mA | Vss | — | Vss + 0.4 | V | |
| | | HVP, HVM, DVP, DVM | RL = 1.5 kΩ ± 5% | 0 | — | 0.3 | V | |
| Input leak current | $I_{IL}$ | Output pin of other than P60 to P67, HVP, HVM, DVP, DVM | $V_{CC}$ = 3.3 V, Vss < $V_I$ < $V_{CC}$ | – 10 | — | 10 | µA | |
| | | HVP, HVM, DVP, DVM | — | – 5 | — | 5 | µA | |
| Pull-up resistor | $R_{PULL}$ | P00 to P07, P10 to P17 | $V_{CC}$ = 3.3 V, Ta = + 25 °C | 25 | 50 | 100 | kΩ | |
| Open drain output current | $I_{LIOD}$ | P60 to P67 | — | — | 0.1 | 10 | µA | |
| Power supply current | $I_{CC}$ | $V_{CC}$ | $V_{CC}$ = 3.3 V, Internal frequency 24 MHz, At normal operating | — | TBD | — | mA | At USB operating Max 90 mA (Target) |
| | | | $V_{CC}$ = 3.3 V, Internal frequency 24 MHz, At normal operating | — | 70 | — | mA | At non-operating USB (USTP = 0) |
| | | | $V_{CC}$ = 3.3 V, Internal frequency 24 MHz, At normal operating | — | TBD | — | mA | At non-operating USB (USTP = 1) |
| | $I_{CCS}$ | | $V_{CC}$ = 3.3 V, Internal frequency 24 MHz, At sleep mode | — | 27 | — | mA | |
| | $I_{CTS}$ | | $V_{CC}$ = 3.3 V, Internal frequency 24 MHz, At timer mode | — | 3.5 | — | mA | |
| | | | $V_{CC}$ = 3.3 V, Internal frequency 3 MHz, At timer mode | — | 1 | — | mA | |
| | $I_{CCH}$ | | Ta = +25 °C, At Stop mode | — | 1 | — | µA | |
| Input capacitance | $C_{IN}$ | Other than Vcc and Vss | — | — | 5 | 15 | pF | |
| Pull-up resistor | $R_{up}$ | $\overline{RST}$ | — | 25 | 50 | 100 | kΩ | |

Note : P60 to P67 are N-ch open-drain pins usually used as CMOS.

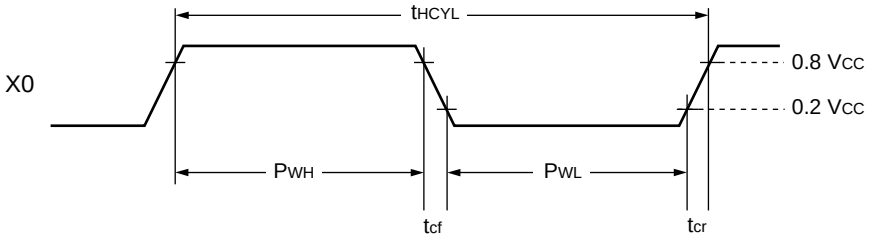
## 4. AC Characteristics

### (1) Clock input timing

($T_A$ = –40 °C to +85 °C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0.0 V)

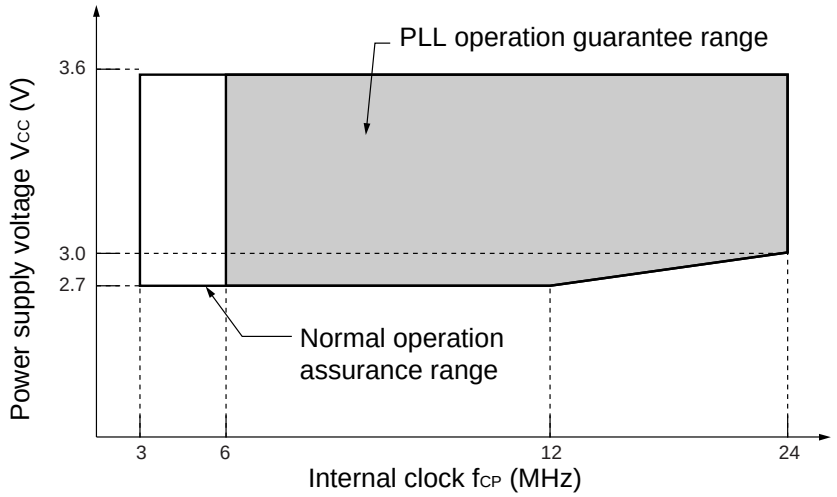
| Parameter | Sym-bol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Clock frequency | $f_{CH}$ | X0, X1 | — | 6 | — | MHz | External crystal oscillation |
| | | | 6 | — | 24 | MHz | External clock input |
| Clock cycle time | $t_{HCYL}$ | X0, X1 | — | 166.7 | — | ns | External crystal oscillation |
| | | | 166.7 | — | 41.7 | ns | External clock input |
| Input clock pulse width | $P_{WH}$<br>$P_{WL}$ | X0 | 10 | — | — | ns | A reference duty ratio is 30% to 70%. |
| Input clock rise time and fall time | tcr<br>tcf | X0 | — | — | 5 | ns | At external clock |
| Internal operating clock frequency | $f_{CP}$ | — | 3 | — | 24 | MHz | At main clock is used |
| Internal operating clock cycle time | $t_{CP}$ | — | 42 | — | 333 | ns | At main clock is used |

• Clock timing



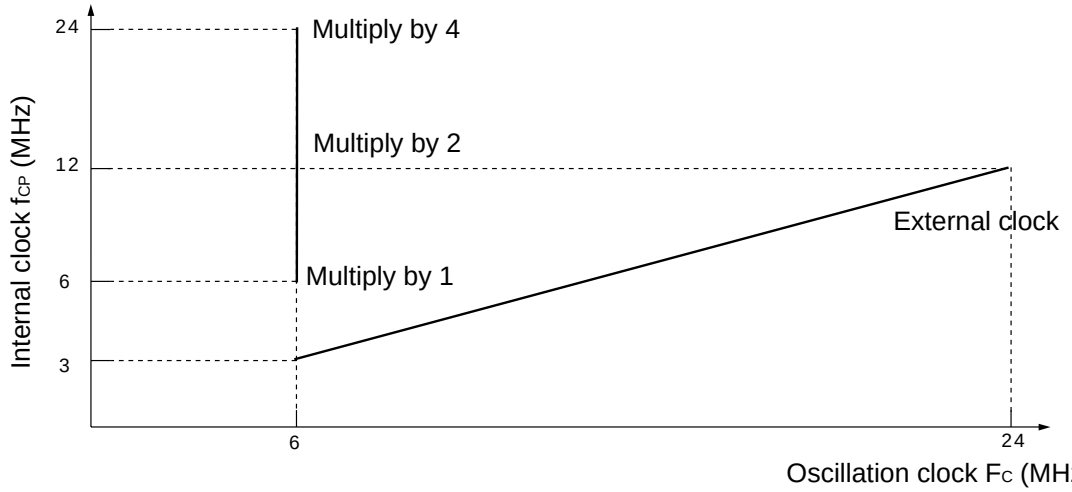
• PLL operation guarantee range

Relation between internal operation clock frequency and power supply voltage




* : When the USB is used, operation is guaranteed at voltages between 3.0 V to 3.6 V.

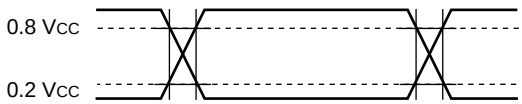
Relation between oscillation frequency and internal operation clock frequency



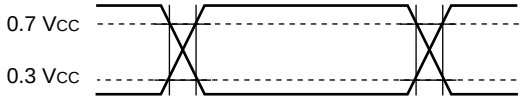

The AC standards provide that the following measurement reference voltages.

• Input signal waveform

Hysteresis input pin

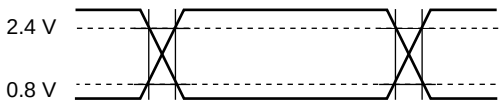



Hysteresis input/other than MD input pin




• Output signal waveform

Output pin



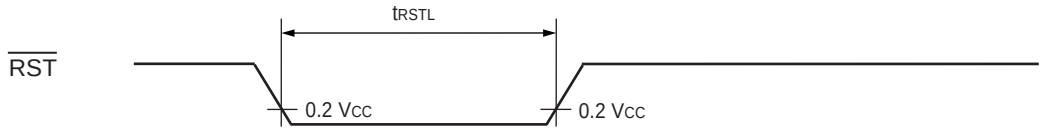
**(2) Reset**

($V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

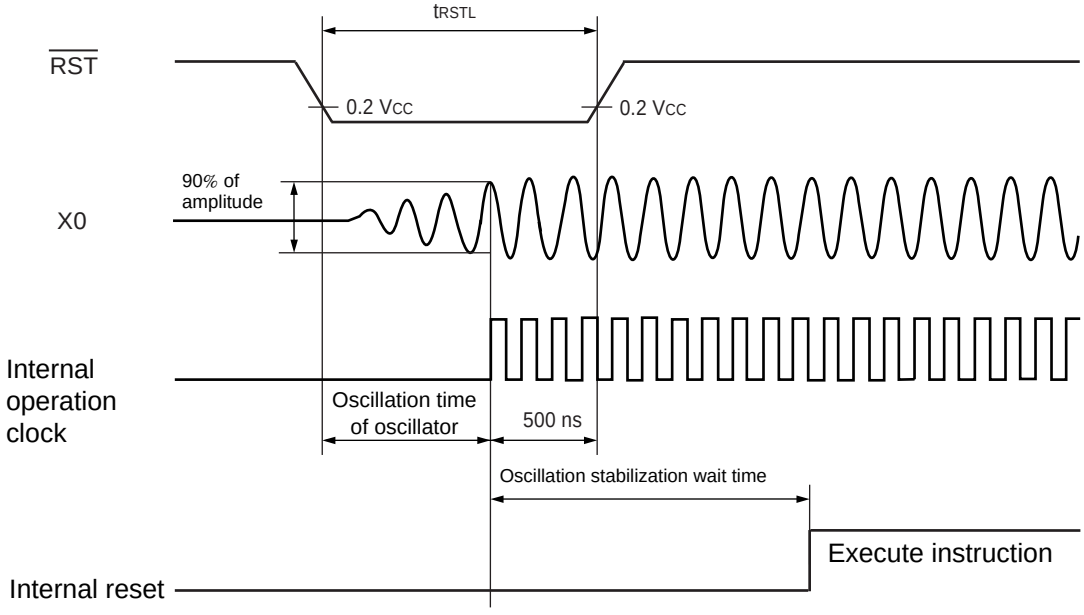
| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Reset input time | $t_{RSTL}$ | $\overline{RST}$ | — | 500 | — | ns | At normal operating, At time base timer mode, At main sleep mode, At PLL sleep mode |
| | | | | Oscillation time of oscillator* + 500 ns | — | µs | At stop mode |

* : Oscillation time of oscillator is the time that the amplitude reaches 90 %. It takes several milliseconds to several dozens of milliseconds on a crystal oscillator, several hundreds of microseconds to several milliseconds on a FAR/ceramic oscillator, and 0 milliseconds on an external clock.

• During normal operation, in time-base timer mode, in main sleep mode and in PLL sleep mode




• In stop mode

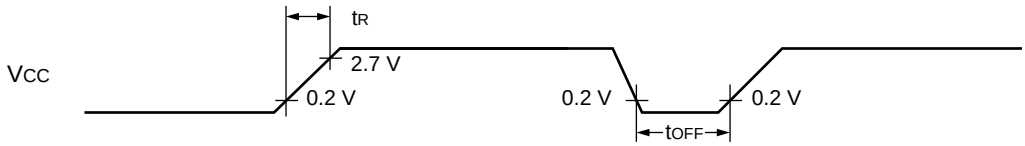


**(3) Power-on reset**

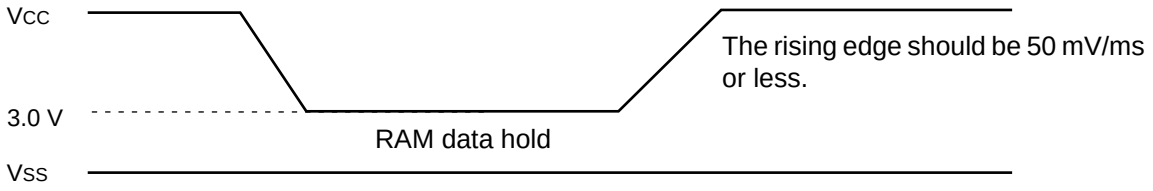
($T_A$ = –40 °C to +85 °C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin name | Condi-tions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Power supply rising time | $t_R$ | $V_{CC}$ | — | — | 30 | ms | |
| Power supply shutdown time | $t_{OFF}$ | $V_{CC}$ | | 1 | — | ms | For repeated operation |

Notes :
- $V_{CC}$ must be lower than 0.2 V before the power supply is turned on.
- The above standard is a value for performing a power - on reset.
- In the device, there are internal registers which is initialized only by a power-on reset. When the initial ization of these items is expected, turn on the power supply according to the standards.




Sudden change of power supply voltage may activate the power-on reset function.
When changing the power supply voltage during operation as illustrated below, voltage fluctuation should be minimized so that the voltage rises as smoothly as possible. When raising the power, do not use PLL clock. However, if voltage drop is 1 V/s or less, use of PLL clock is allowed during operation.



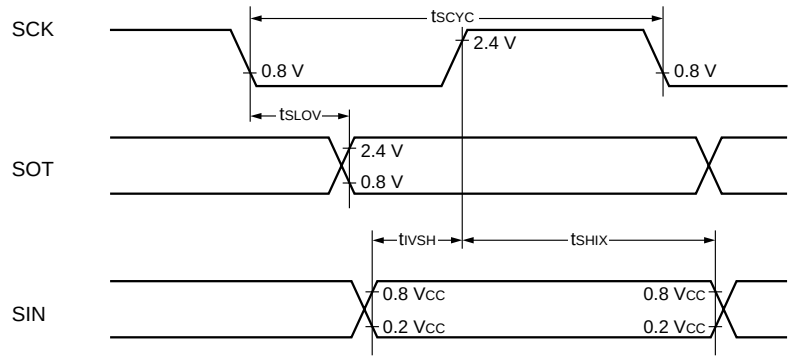
### (4) UART0, UART1 I/O extended serial timing

($T_A$ = –40 °C to +85 °C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0.0 V)

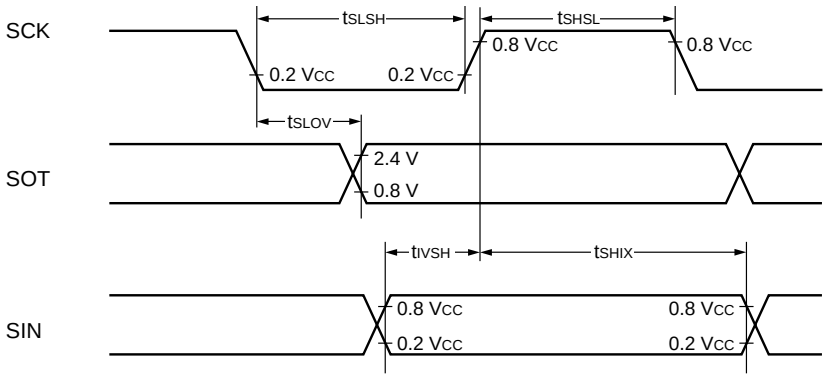
| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCKx | Internal shiftc lock Mode output pin is $C_L$ = 80 pF + 1 TTL | 8 $t_{CP}$ | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | SCKx SOTx | | – 80 | 80 | ns | |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | SCKx SINx | | 100 | — | ns | |
| SCK ↑ → valid SIN hold time | $t_{SHIX}$ | SCKx SINx | | 60 | — | ns | |
| Serial clock H pulse width | $t_{SHSL}$ | SCKx, SINx | External shift clock Mode output pin is $C_L$ = 80 pF + 1 TTL | 4 $t_{CP}$ | — | ns | |
| Serial clock L pulse width | $t_{SLSH}$ | SCKx, SINx | | 4 $t_{CP}$ | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | SCKx SOTx | | — | 150 | ns | |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | SCKx SINx | | 60 | — | ns | |
| SCK ↑ → valid SIN hold time | $t_{SHIX}$ | SCKx SINx | | 60 | — | ns | |

Notes :
- AC rating in CLK synchronous mode.
- $C_L$ is a load capacitance value on pins for testing.
- $t_{CP}$ is the machine cycle period (unit : ns) .

- Internal shift clock mode



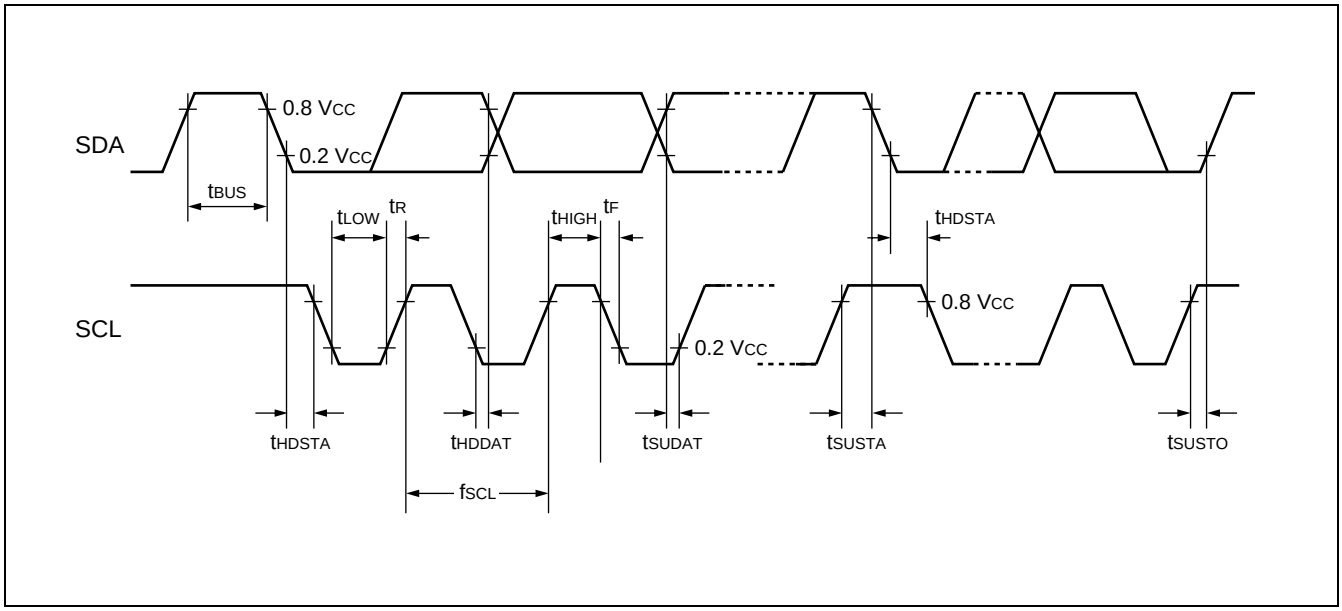

- External shift clock mode



### (5) I²C timing

($V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

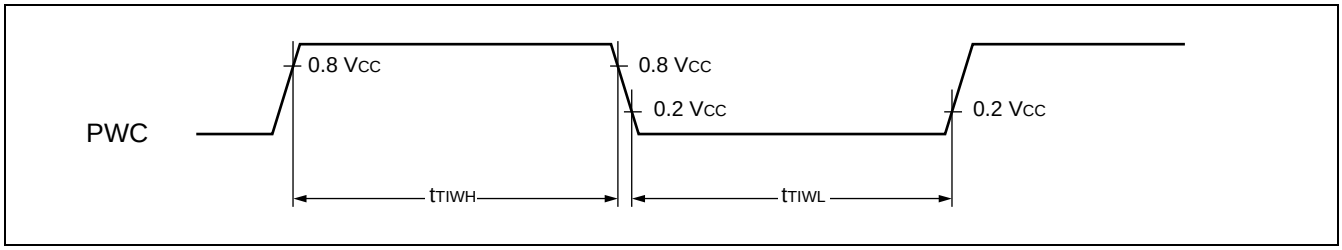
| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCL clock frequency | $f_{SCL}$ | — | — | 0 | 100 | kHz | |
| Bus-free time between stop and start conditions | $t_{BUS}$ | — | | 4.7 | — | µs | |
| Hold time (resend) start | $t_{HDSTA}$ | — | | 4.0 | — | µs | The first clock pulse is generated immediately after the period. |
| SCL clock “L” status hold time | $t_{LOW}$ | — | | 4.7 | — | µs | |
| SCL clock “H” status hold time | $t_{HIGH}$ | — | | 4.0 | — | µs | |
| Resend start condition setup time | $t_{SUSTA}$ | — | | 4.7 | — | µs | |
| Data hold time | $t_{HDDAT}$ | — | | 0 | — | µs | |
| Data set-up time | $t_{SUDAT}$ | — | | 40 | — | ns | |
| SDA and SCL signal rise time | $t_R$ | — | | — | 1000 | ns | |
| SDA and SCL signal fall time | $t_F$ | — | | — | 300 | ns | |
| Stop condition setup time | $t_{SUSTO}$ | — | | 4.0 | — | µs | |



### (6) Timer Input Timing

($T_A$ = –40 °C to +85 °C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0.0 V)

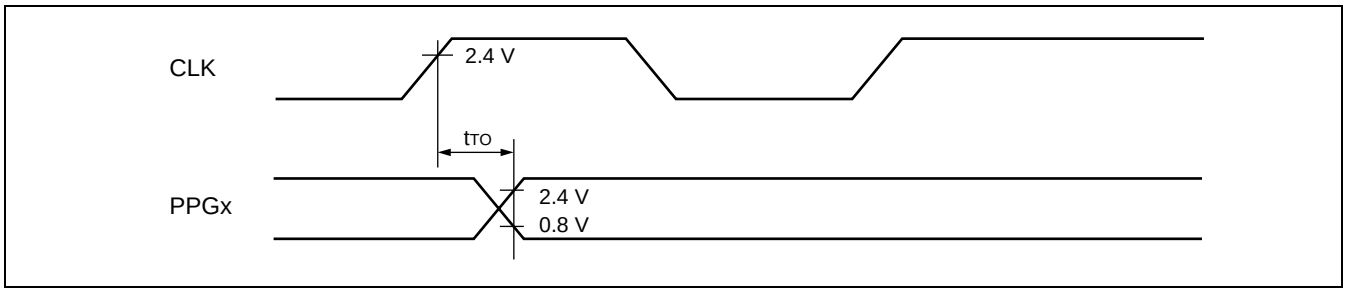
| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TIWH}$<br>$t_{TIWL}$ | PWC | — | 4 $t_{CP}$ | — | ns | |




### (7) Timer output timing

($T_A$ = –40 °C to +85 °C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0.0 V)

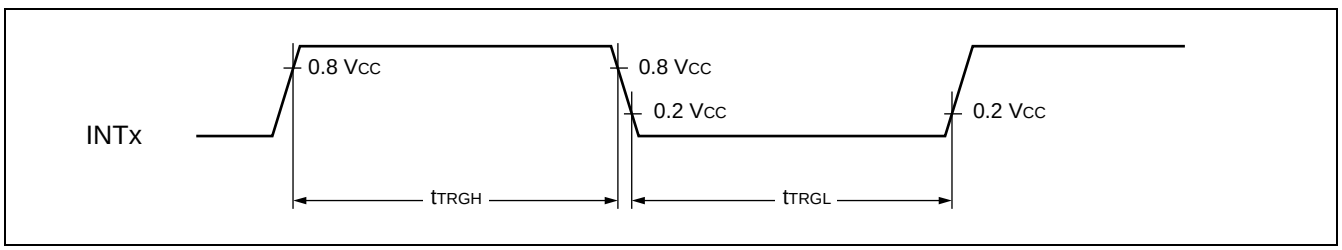
| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| CLK ↑ → TOUT change time<br>PPG0 to PPG3 change time | $t_{TO}$ | PPGx | — | 30 | — | ns | |




### (8) Trigger Input Timing

($T_A$ = –40 °C to +85 °C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TRGH}$<br>$t_{TRGL}$ | INTx | — | 5 $t_{CP}$ | — | ns | At normal operating |
| | | | | 1 | — | µs | At Stop mode |

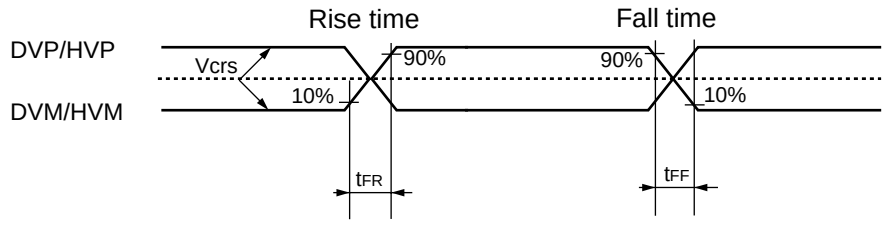


## 5. USB characteristics

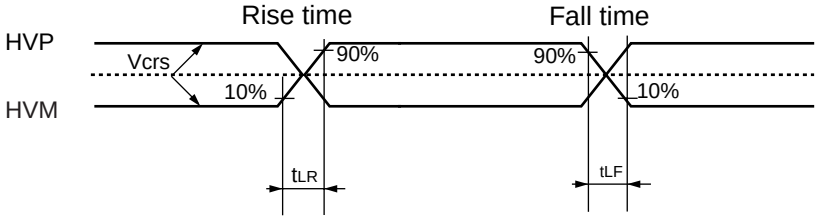
($T_A$ = 0 °C to +70 °C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Input characteristics | Input High level voltage | $V_{IH}$ | 2.0 | — | V | |
| | Input Low level voltage | $V_{IL}$ | — | 0.8 | V | |
| | Differential input sensitivity | $V_{DI}$ | 0.2 | — | V | |
| | Differential common mode range | $V_{CM}$ | 0.8 | 2.5 | V | |
| Output characteristics | Output High level voltage | $V_{OH}$ | 2.8 | 3.6 | V | $I_{OH}$ = –200 µA |
| | Output Low level voltage | $V_{OL}$ | 0.0 | 0.3 | V | $I_{OL}$ = 2 mA |
| | Cross over voltage | $V_{CRS}$ | 1.3 | 2.0 | V | |
| | Rise time | $t_{FR}$ | 4 | 20 | ns | Full Speed |
| | | $t_{LR}$ | 75 | 300 | ns | Low Speed |
| | Fall time | $t_{FF}$ | 4 | 20 | ns | Full Speed |
| | | $t_{LF}$ | 75 | 300 | ns | Low Speed |
| | Rising/falling time matching | $t_{RFM}$ | 90 | 111.11 | % | ($T_{FR}/T_{FF}$) |
| | | $t_{RLM}$ | 80 | 125 | % | ($T_{LR}/T_{LF}$) |
| | Output registance | $Z_{DRV}$ | 28 | 44 | Ω | Including Rs = 27 Ω |

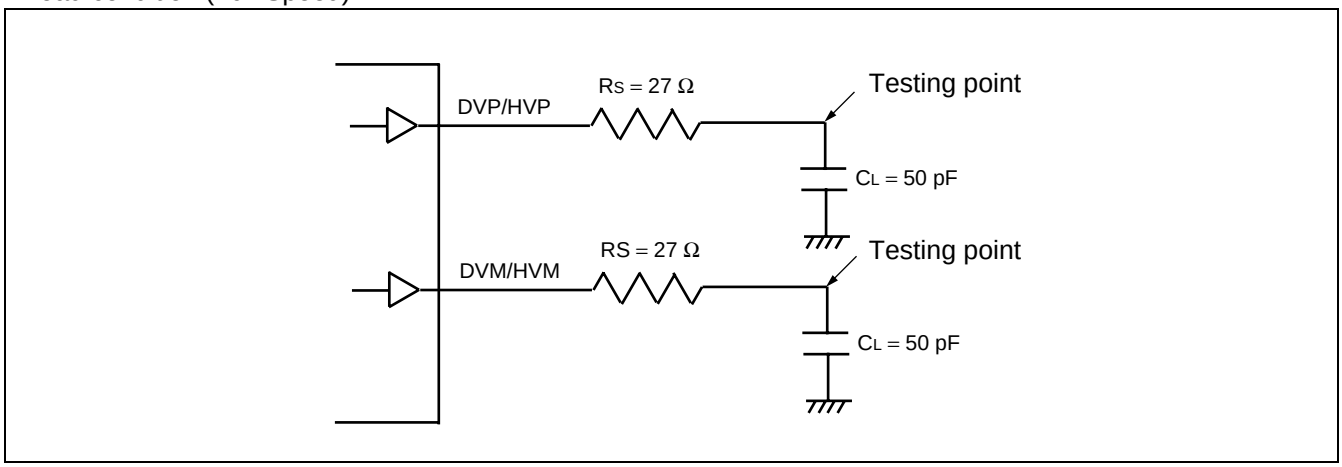
• Data signal timing (Full Speed)



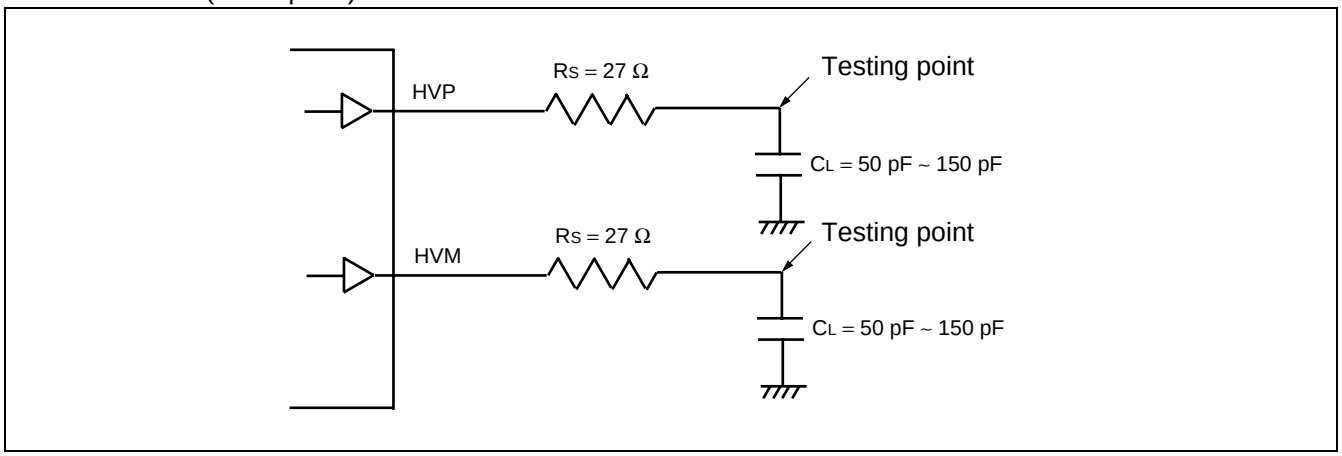

• Data signal timing (Low Speed)



• Load condition (Full Speed)




• Load condition (Low Speed)



## ■ ORDERING INFORMATION

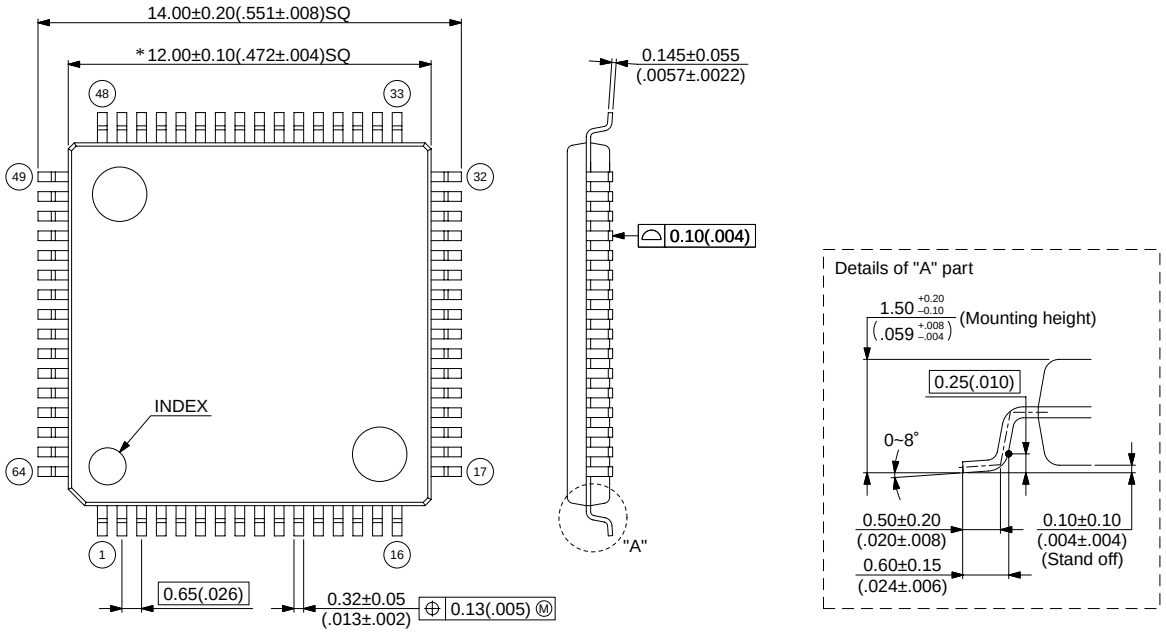
• MB90335 Series

| Part number | Package | Remarks |
|---|---|---|
| MB90F337PFM<br>MB90337PFM | 64-pin plastic LQFP<br>(FPT-64P-M09) | |

## ■ PACKAGE DIMENSION

64-pin plastic LQFP
(FPT-64P-M09)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.






Dimensions in mm (inches)
Note : The values in parentheses are reference values.

# MEMO

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