

4-bit shifter

74F350

FEATURES

- Shifts 4 bits of data to 0, 1, 2, 3 places under control of two select lines
- 3-State outputs for bus organized systems

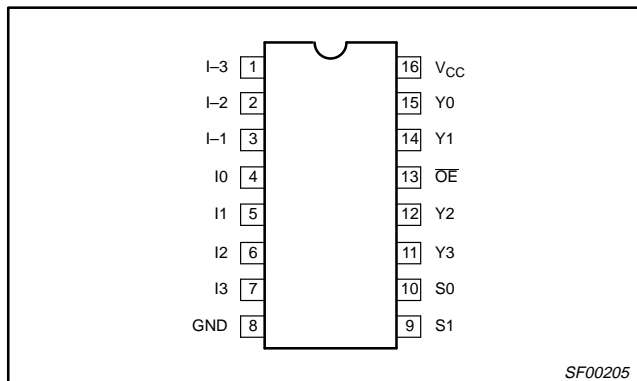
DESCRIPTION

The 74F350 is a combination logic circuit that shifts a 4-bit word from 0 to 3 places. No clocking is required as with shift registers. The 74F350 can be used to shift any number of bits any number of places up or down by suitable interconnection. Shifting can be:

1. Logical — with logic zeros filled in at either end of the shifting field.
2. Arithmetic — where the sign bit is extended during a shift down.
3. End around — where the data word forms a continuous loop.

The 3-State outputs are useful for bus interface applications or expansion to a larger number of shift positions in end around shifting. The active Low Output Enable (\overline{OE}) controls the state of the outputs. The outputs are in the high impedance "off" state when \overline{OE} is High, and they are active when \overline{OE} is Low.

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$
16-pin plastic DIP	N74F350N
16-pin plastic SO	N74F350D

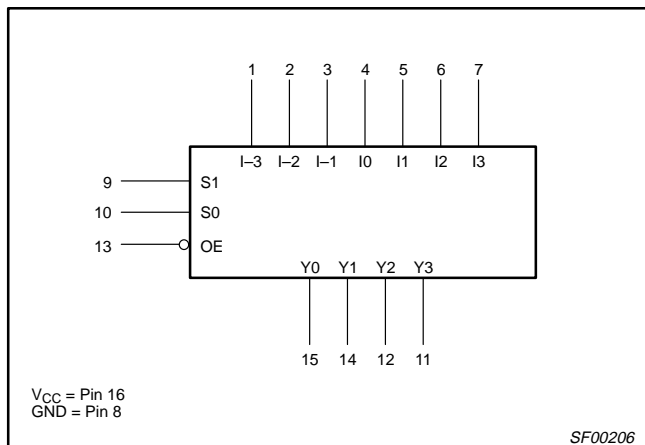
TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F350	5.2ns	24mA

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

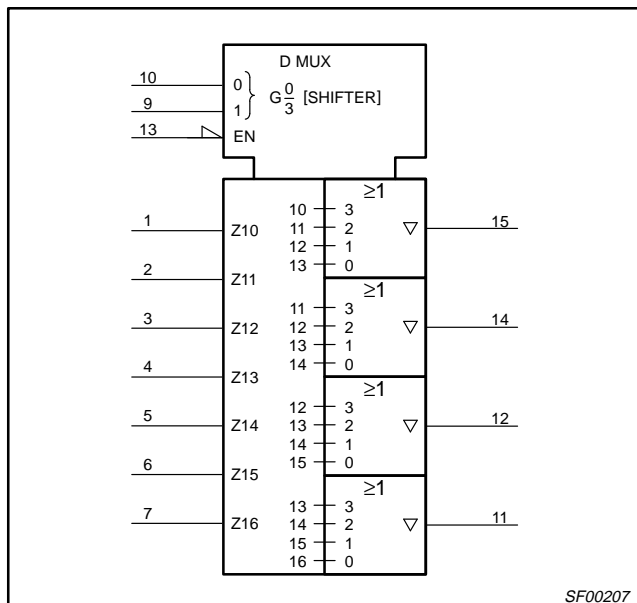
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I-n, In	Data inputs	1.0/2.0	20 μ A/1.2mA
S0, S1	Select inputs (active Low)	1.0/2.0	20 μ A/1.2mA
\overline{OE}	Output Enable input (active Low)	1.0/2.0	20 μ A/1.2mA
Y0 – Y3	Data outputs	150/40	3.0mA/24mA

NOTE: One (1.0) FAST unit load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



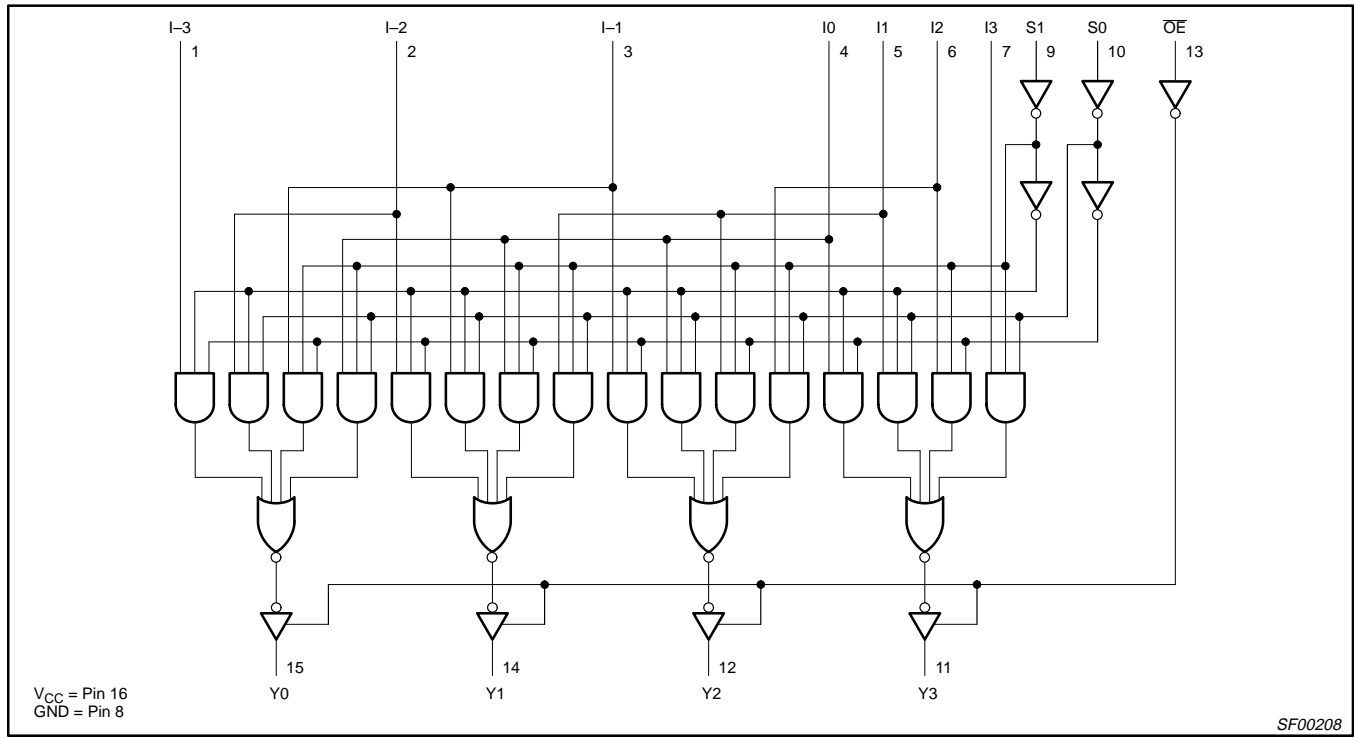
IEC/IEEE SYMBOL



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LOGIC DIAGRAM



FUNCTION TABLE

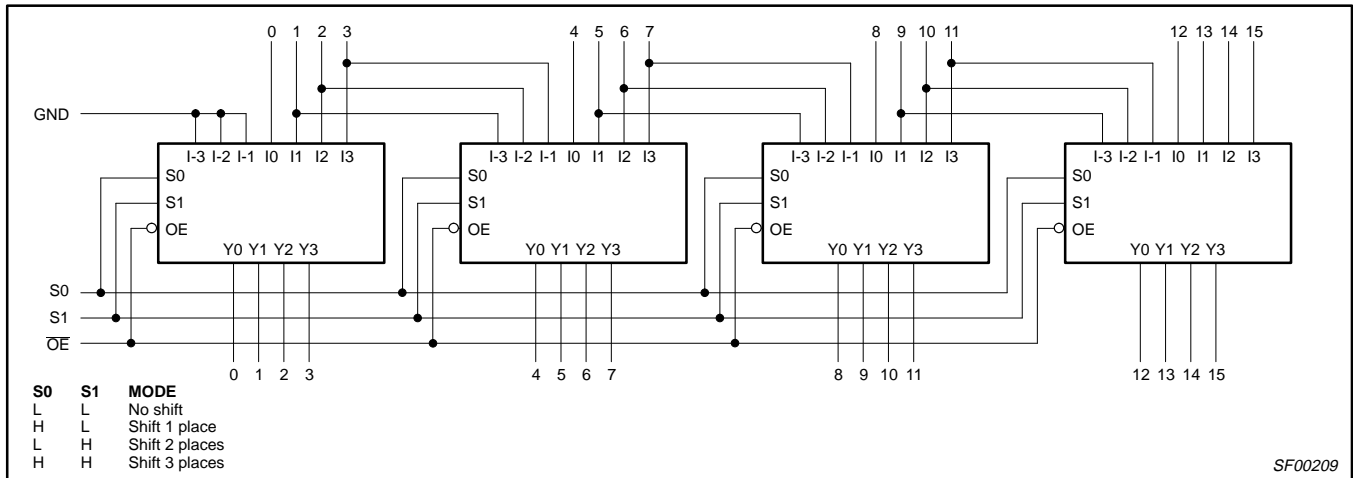
INPUTS										OUTPUTS			
OE	S1	S0	I3	I2	I1	I0	I-1	I-2	I-3	Y3	Y2	Y1	Y0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D3	D2	D1	D0	X	X	X	D3	D2	D1	D0
L	L	H	X	D2	D1	D0	D-1	X	X	D2	D1	D0	D-1
L	H	L	X	X	D1	D0	D-1	D-2	X	D1	D0	D-1	D-2
L	H	H	X	X	X	D0	D-1	D-2	D-3	D0	D-1	D-2	D-3

H = High voltage level
 L = Low voltage level
 X = Don't care
 Z = High impedance "off" state
 Dn = High or Low state of referenced In input

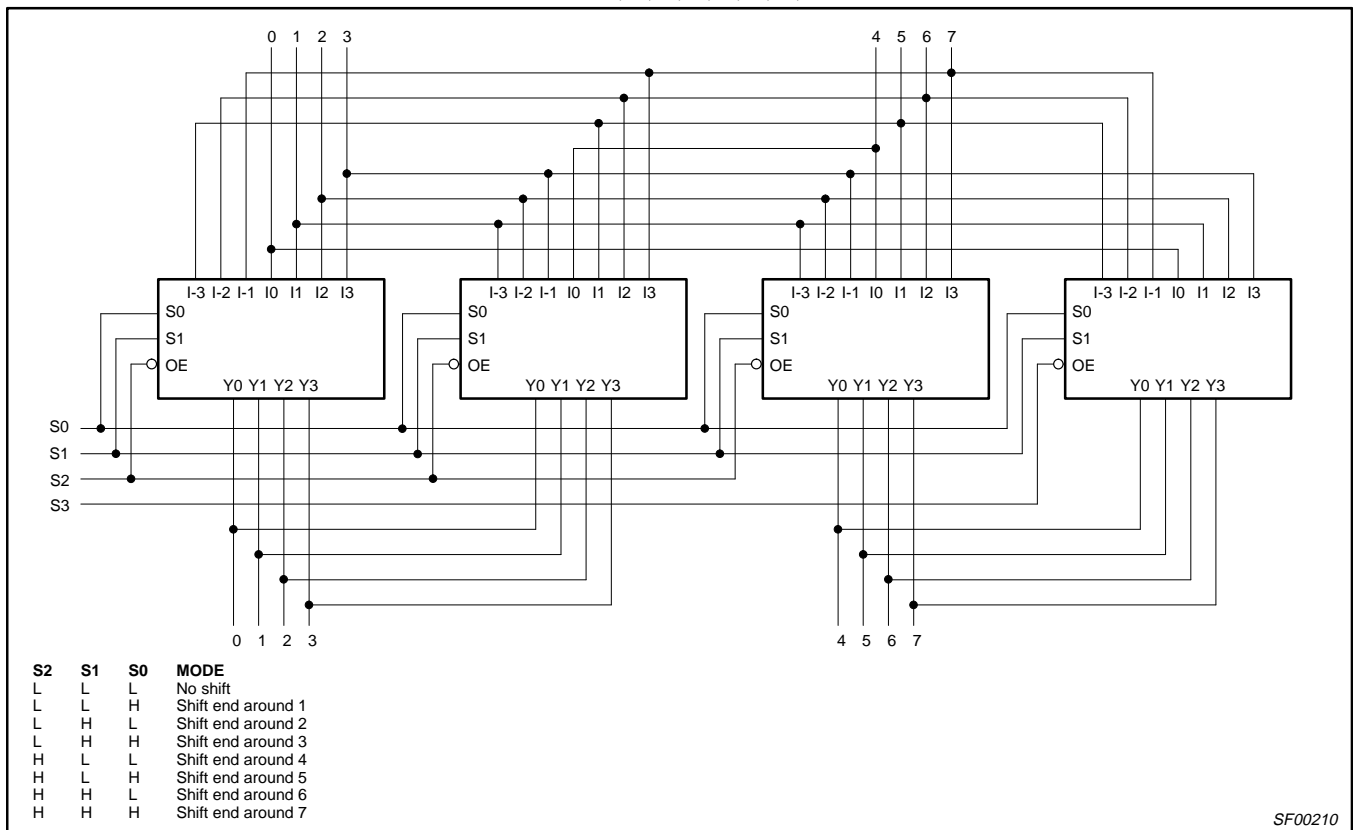
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APPLICATION FOR 16-BIT SHIFT UP 0, 1, 2, OR 3 PLACES



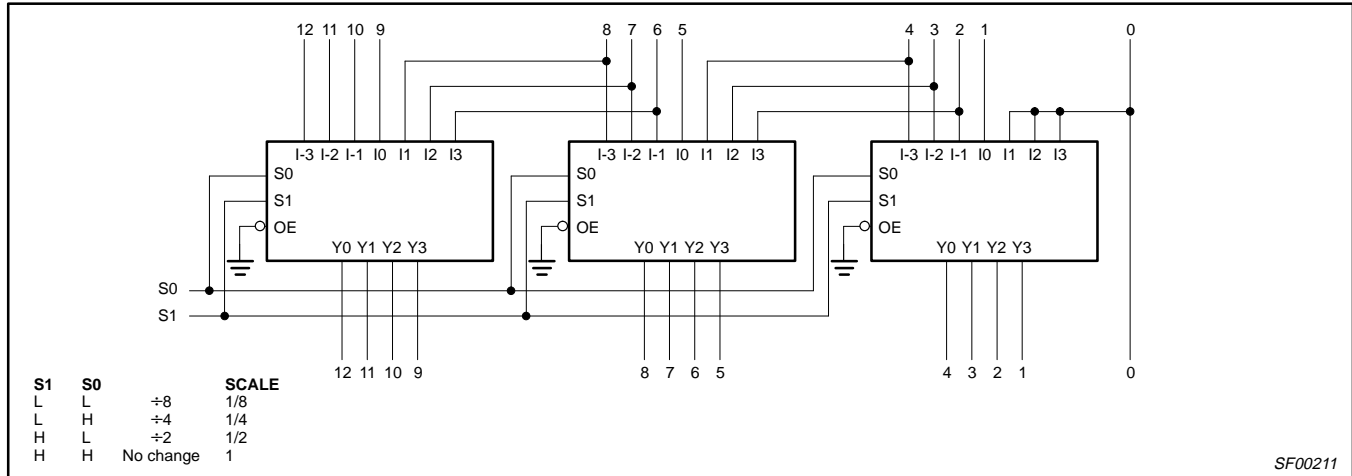
APPLICATION FOR 8-BIT END AROUND SHIFT 0, 1, 2, 3, 4, 5, 6, OR 7 PLACES



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APPLICATION FOR 13-BIT TWO'S COMPLEMENT SCALER



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	-0.5 to +7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in High output state	-0.5 to V _{CC}	V
I _{OUT}	Current applied to output in Low output state	48	mA
T _{amb}	Operating free-air temperature range	0 to +70	°C
T _{stg}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			-3	mA
I _{OL}	Low-level output current			24	mA
T _{amb}	Operating free-air temperature range	0		+70	°C

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT		
			MIN	TYP ²	MAX			
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = MAX	±10%V _{CC}	2.4		V		
		V _{IH} = MIN, I _{OH} = MAX	±5%V _{CC}	2.7	3.4			
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = MAX	±10%V _{CC}		0.35	0.50	V	
		V _{IH} = MIN, I _{OL} = MAX	±5%V _{CC}		0.35	0.50		
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-0.73	-1.2	V	
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V				100	μA	
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7V				20	μA	
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.5V				-1.2	mA	
I _{ozH}	Off-state output current, High-level voltage applied	V _{CC} = MAX, V _O = 2.7V				50	μA	
I _{ozL}	Off-state output current, Low-level voltage applied	V _{CC} = MAX, V _O = 0.5V				-50	μA	
I _{OS}	Short-circuit output current ³	V _{CC} = MAX				-60	-150	mA
I _{CC}	Supply current (total)	V _{CC} = MAX	I _{CCH}		22	35	mA	
			I _{CCL}		26	41	mA	
			I _{CCZ}		26	42	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

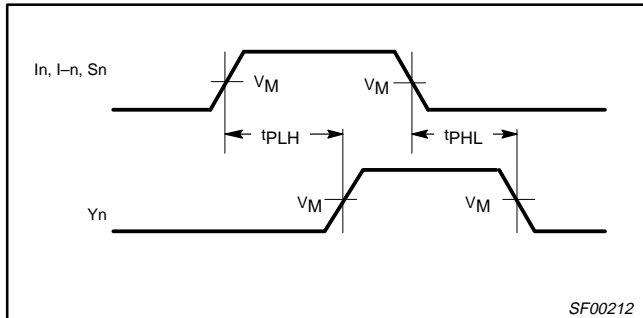
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V _{CC} = +5.0V T _{amb} = +25°C C _L = 50pF, R _L = 500Ω			V _{CC} = +5.0V ± 10% T _{amb} = 0°C to +70°C C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay In to Yn	Waveform 1	3.0 2.5	4.5 4.0	6.0 5.5	3.0 2.5	7.0 6.5	ns
t _{PLH} t _{PHL}	Propagation delay Sn to Yn	Waveform 1	4.0 3.0	7.8 6.5	10.0 8.5	4.0 3.0	11.0 9.5	ns
t _{PZH} t _{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	2.5 4.0	5.0 7.0	7.0 9.0	2.5 4.0	8.0 10.0	ns
t _{PHZ} t _{PLZ}	Output Disable time to High or Low level	Waveform 2 Waveform 3	2.0 2.0	3.9 4.0	5.5 5.5	2.0 2.0	6.5 6.5	ns

4-bit shifter

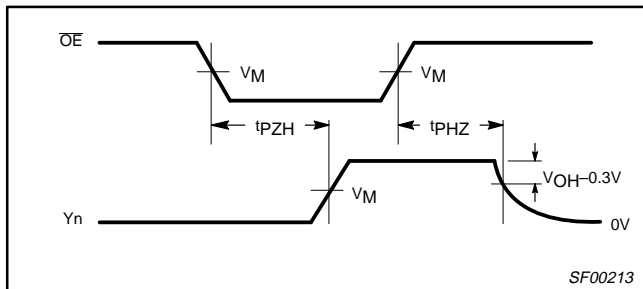
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AC WAVEFORMS

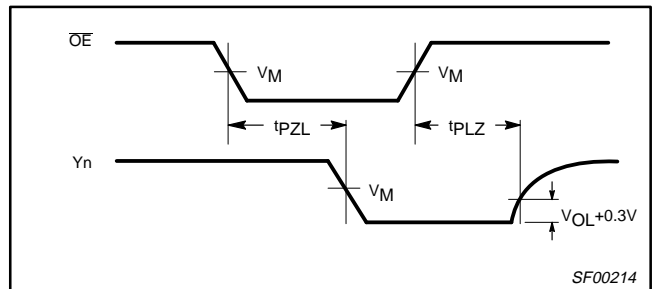
For all waveforms, $V_M = 1.5V$.



Waveform 1. Propagation Delay Data and Select to Output



Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS

Test Circuit for Open Collector Outputs

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128