

SEMICONDUCTORIM

April 1988 Revised August 1999

74F378

Parallel D-Type Register with Enable

General Description

The 74F378 is a 6-bit register with a buffered common Enable. This device is similar to the 74F174, but with common Enable rather than common Master Reset.

Features

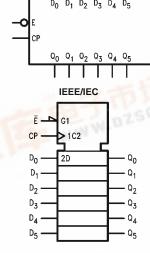
- 6-bit high-speed parallel register
- Positive edge-triggered D-type inputs
- Fully buffered common clock and enable inputs
- Input clamp diodes limit high-speed termination effects
- Full TTL and CMOS compatible

Ordering Code:

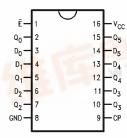
Order Number				
74F378SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow		
74F378SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide		
74F378PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide		

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Dia Nama	B tatio	U.L.	Input I _{IH} /I _{IL}		
Pin Names	Description	HIGH/LOW	Output I _{OH} /I _{OL}		
Ē	Enable Input (Active LOW)	1.0/1.0	20 μA/–0.6 mA		
D ₀ –D ₅	Data Inputs	1.0/1.0	20 μA/–0.6 mA		
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/–0.6 mA		
Q ₀ –Q ₅	Outputs	50/33.3	−1 mA/20 mA		

Functional Description

The 74F378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q inputs. The Clock (CP) and Enable (\overline{E}) inputs are common to all flip-flops.

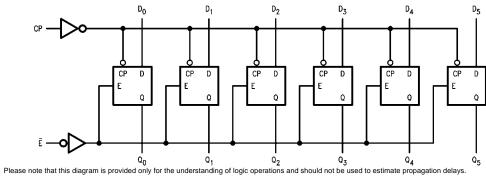
When the $\overline{\mathsf{E}}$ input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the E input is HIGH the register will retain the present data independent of the CP input.

Truth Table

	Output		
Ē	СР	D _n	Q _n
Н	\	Х	No Change
L	~	Н	Н
L	~	L	L

H = HIGH Voltage Level

Logic Diagram



L = LOW Voltage Level

X = Immaterial

^{∠ =} LOW-to-HIGH Clock Transition

Absolute Maximum Ratings(Note 1)

Recommended Operating Conditions

 $\begin{array}{ll} \mbox{Storage Temperature} & -65\mbox{°C to } +150\mbox{°C} \\ \mbox{Ambient Temperature under Bias} & -55\mbox{°C to } +125\mbox{°C} \\ \end{array}$

 $\begin{array}{lll} \mbox{Junction Temperature under Bias} & -55^{\circ}\mbox{C to } +150^{\circ}\mbox{C} \\ \mbox{V}_{\mbox{CC}} \mbox{ Pin Potential to Ground Pin} & -0.5\mbox{V to } +7.0\mbox{V} \\ \mbox{Input Voltage (Note 2)} & -0.5\mbox{V to } +7.0\mbox{V} \end{array}$

Input Current (Note 2)

-30 mA to +5.0 mA

Voltage Applied to Output

in HIGH State (with $V_{CC} = 0V$)

Standard Output -0.5V to V_{CC} 3-STATE Output -0.5V to +5.5V

Current Applied to Output

in LOW State (Max) $\qquad \qquad \text{twice the rated I}_{\text{OL}} \, (\text{mA})$

Free Air Ambient Temperature $0^{\circ}\text{C} \text{ to } +70^{\circ}\text{C}$ Supply Voltage +4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation

under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

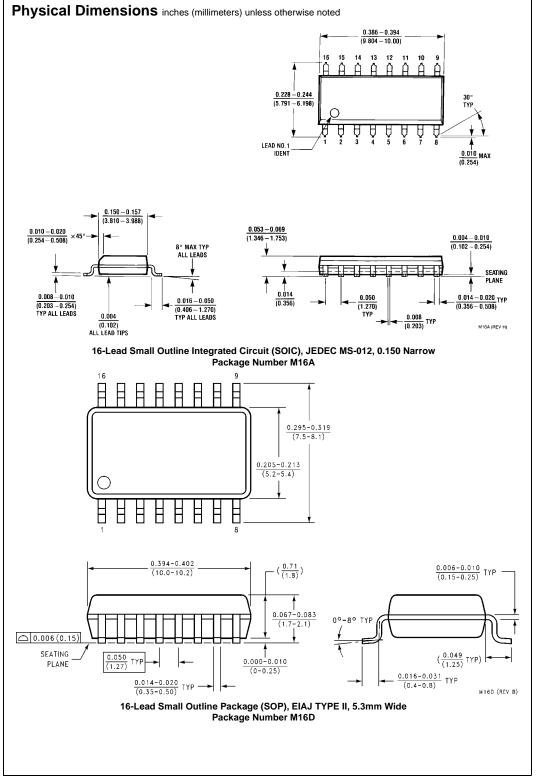
Symbol	Parameter		Min	Тур	Max	Units	v _{cc}	Conditions
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH	10% V _{CC}	2.5			V	Min	I _{OH} = -1 mA
	Voltage	5% V _{CC}	2.7			V	IVIII	$I_{OH} = -1 \text{ mA}$
V _{OL}	Output LOW	10% V _{CC}			0.5	V	Min	1 20 mA
	Voltage				0.5	V	IVIII	I _{OL} = 20 mA
I _{IH}	Input HIGH				5.0	^	Max	V _{IN} = 2.7V
	Current				5.0	μА	IVIAX	v _{IN} = 2.7 v
I _{BVI}	Input HIGH Current				7.0	^	Max	V 7.0V
	Breakdown Test				7.0	μА	IVIAX	V _{IN} = 7.0V
I _{CEX}	Output HIGH				50	^	Max	V - V
	Leakage Current				50	μА	IVIAX	$V_{OUT} = V_{CC}$
V _{ID}	Input Leakage		4.75			V	0.0	$I_{ID} = 1.9 \mu A$
	Test		4.75					All Other Pins Grounded
I _{OD}	Output Leakage				0.75	^	0.0	V _{IOD} = 150 mV
	Circuit Current				3.75	μА	0.0	All Other Pins Grounded
I _{IL}	Input LOW Current				-0.6	mA	Max	V _{IN} = 0.5V
los	Output Short-Circuit Current		-60		-150	mA	Max	V _{OUT} = 0V
I _{CCL}	Power Supply Current			30	45	mA	Max	V _O = LOW

AC Electrical Characteristics

Symbol	Parameter	$\begin{aligned} T_{A} &= +25^{\circ}\text{C} \\ V_{CC} &= +5.0\text{V} \\ C_{L} &= 50\text{ pF} \end{aligned}$			V _{CC} =	to +125°C +5.0V 50 pF	$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$ $C_L = 50$ pF		Units
		Min	Тур	Max	Min	Max	Min	Max	Į l
f _{MAX}	Maximum Input Frequency	80	100		70		80		MHz
t _{PLH}	Propagation Delay	3.0	5.5	7.5	3.0	10.0	3.0	8.5	20
t _{PHI}	CP to Q _n	3.5	6.0	8.5	3.5	10.5	3.5	9.5	ns

AC Operating Requirements

Symbol	Parameter	$T_A = +25$ °C $V_{CC} = +5.0V$		$T_A = -55^{\circ}C$ to $+125^{\circ}C$ $V_{CC} = +5.0V$		$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$		Units	
		Min	Max	Min	Max	Min	Max		
t _S (H)	Setup Time, HIGH or LOW	4.0		5.0		4.0			
t _S (L)	D _n to CP	4.0		5.0		4.0			
t _H (H)	Hold Time, HIGH or LOW	0		2.0		0		ns	
t _H (L)	D _n to CP	0		2.0		0			
t _S (H)	Setup Time, HIGH or LOW	6.0		4.5		6.0			
$t_S(L)$	E to CP	10.0		13.0		10.0			
t _H (H)	Hold Time, HIGH or LOW	0		0		0		ns	
$t_H(L)$	E to CP	0		0		0			
t _W (H)	CP Pulse Width	4.0		5.0		4.0		ns	
$t_W(L)$	HIGH or LOW	6.0		7.5		6.0		115	



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.780 0.090 (18.80 - 19.81)(2.286)14 13 12 11 INDEX AREA 0.250 ± 0.010 (6.350 ± 0.254) PIN NO. 1 IDENT PIN NO. 1 2 3 4 5 6 7 8 1 2 OPTION 01 OPTION 02 0.065 $\frac{0.130 \pm 0.005}{(3.302 \pm 0.127)}$ $\frac{0.060}{(1.524)}$ TYP 4° TYP 0.300 - 0.320 (1.651)OPTIONAL (7.620 - 8.128)0.145 - 0.200 (3.683 - 5.080)95° ± 5° $\frac{0.008 - 0.016}{(0.203 - 0.406)} \text{ TYP}$ 0.020 MIN 0.280 0.125 - 0.150 (3.175 - 3.810) (7.112) MIN 0.030 ± 0.015 (0.762 ± 0.381) 0.014 - 0.023 (0.325 +0.040 -0.015 0.100 ± 0.010 (0.356 - 0.584)(2.540 ± 0.254) TYP 0.050 ± 0.010 (1.270 ± 0.254) TYP N16E (REV F) (8.255 **+**1.016 **-**0.381

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com