



August 1995

54F/74F379 Quad Parallel Register with Enable

General Description

The 'F379 is a 4-bit register with buffered common Enable. This device is similar to the 'F175 but features the common Enable rather than common Master Reset.

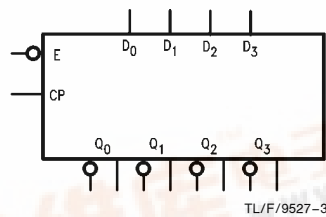
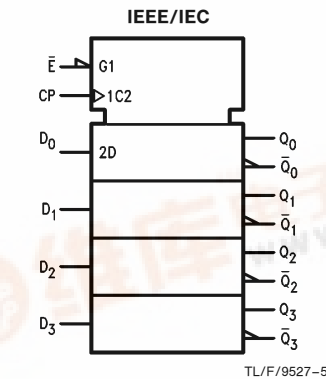
Features

- Edge triggered D-type inputs
- Buffered positive edge-triggered clock
- Buffered common enable input
- True and complement outputs
- Guaranteed 4000V minimum ESD protection

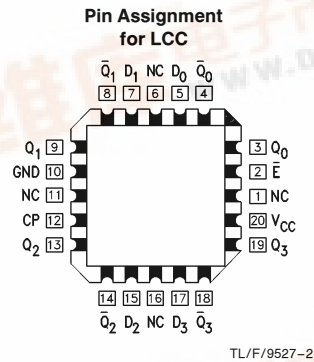
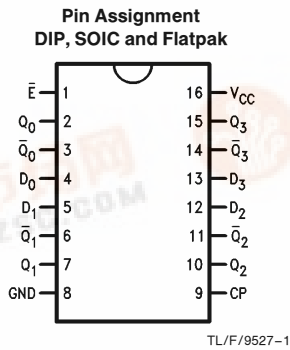
Commercial	Military	Package Number	Package Description
74F379PC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F379DM (QB)	J16A	16-Lead Ceramic Dual-In-Line
74F379SC (Note 1)		M16A	16-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F379SJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F379FM (QB)	W16A	16-Lead Cerpack
	54F379LM (QB)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Logic Symbols



Connection Diagrams



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54F/74F379 Quad Parallel Register with Enable



Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}
\bar{E}	Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
D ₀ -D ₃	Data Inputs	1.0/1.0	20 μ A/ -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μ A/ -0.6 mA
Q ₀ -Q ₃	Flip-Flop Outputs	50/33.3	-1 mA/20 mA
\bar{Q}_0 - \bar{Q}_3	Complement Outputs	50/33.3	-1 mA/20 mA

Functional Description

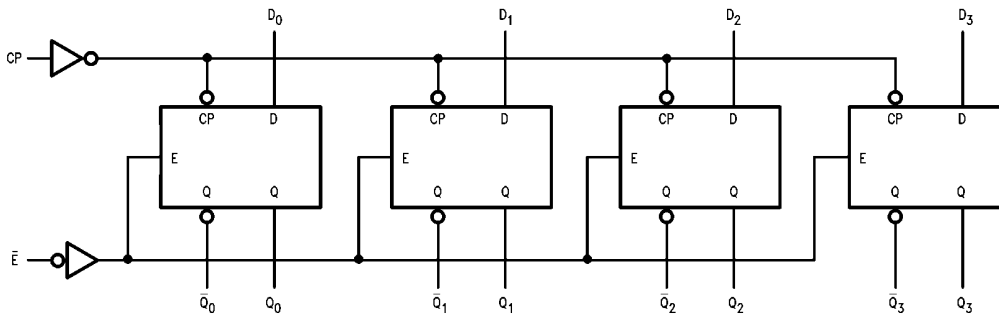
The 'F379 consists of four edge-triggered D-Type flip-flops with individual D inputs and Q and \bar{Q} outputs. The Clock (CP) and Enable (\bar{E}) inputs are common to all flip-flops. When the \bar{E} is input HIGH, the register will retain the present data independent of the CP input. The D_n and \bar{E} inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed.

Truth Table

Inputs			Outputs	
\bar{E}	CP	D _n	Q _n	\bar{Q}_n
H	—	X	NC	NC
L	—	H	H	L
L	—	L	L	H

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 — = LOW-to-HIGH Transition
 NC = No Change

Logic Diagram



TL/F/9527-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE® Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V _{CC}	Conditions
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage					V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage					V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC}	2.5			V	Min	I _{OH} = -1 mA
		74F 10% V _{CC}	2.5					
		74F 5% V _{CC}	2.7					
V _{OL}	Output LOW Voltage	54F 10% V _{CC}				V	Min	I _{OL} = 20 mA
		74F 10% V _{CC}						
I _{IH}	Input HIGH Current	54F	20.0			μA	Max	V _{IN} = 2.7V
		74F	5.0					
I _{BVI}	Input HIGH Current Breakdown Test	54F	100			μA	Max	V _{IN} = 7.0V
		74F	7.0					
I _{CEX}	Output HIGH Leakage Current	54F	250			μA	Max	V _{OUT} = V _{CC}
		74F	50					
V _{ID}	Input Leakage Test	74F	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F	3.75			μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current		-0.6			mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current		-60	-150		mA	Max	V _{OUT} = 0V
I _{CCL}	Power Supply Current		28	40		mA	Max	V _O = LOW

AC Electrical Characteristics

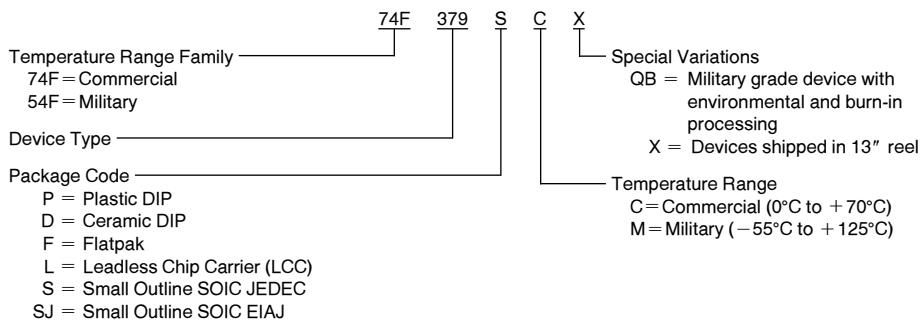
Symbol	Parameter	74F			54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	100	140		75		100	MHz	
t _{PLH}	Propagation Delay	3.5	5.0	6.5	3.0	8.5	3.5	7.5	ns
t _{PHL}	CP to Q _n , \bar{Q}_n	5.0	6.5	8.5	4.0	10.0	5.0	9.5	

AC Operating Requirements

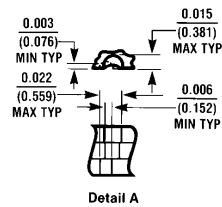
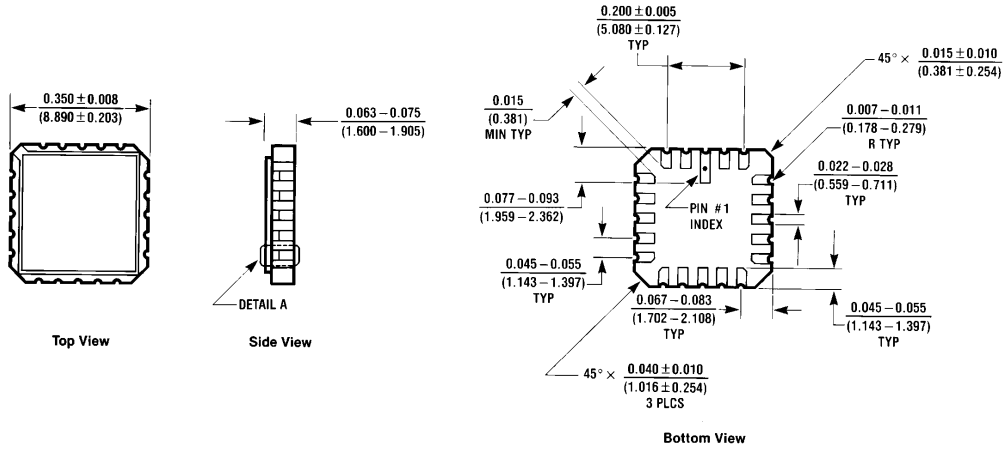
Symbol	Parameter	74F		54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V		T _A , V _{CC} = Mil		T _A , V _{CC} = Com		
		Min	Max	Min	Max	Min	Max	
t _s (H)	Setup Time, HIGH or LOW	3.0		4.0			3.0	ns
t _s (L)	D _n to CP	3.0		4.0			3.0	
t _h (H)	Hold Time, HIGH or LOW	1.0		2.0			1.0	ns
t _h (L)	D _n to CP	1.0		2.0			1.0	
t _s (H)	Setup Time, HIGH or LOW	6.0		8.0			6.0	ns
t _s (L)	\bar{E} to CP	6.0		8.0			6.0	
t _h (H)	Hold Time, HIGH or LOW	0		0			0	ns
t _h (L)	\bar{E} to CP	0		0			0	
t _w (H)	CP Pulse Width	4.0		5.0			4.0	ns
t _w (L)	HIGH or LOW	5.0		7.0			5.0	

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

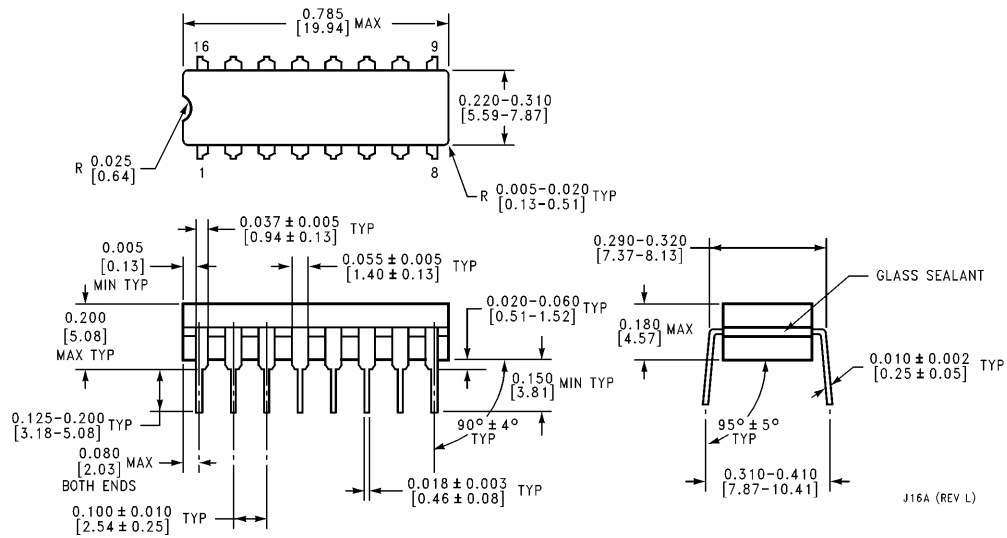


Physical Dimensions inches (millimeters)



20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

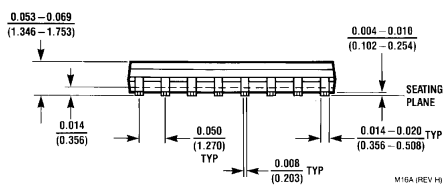
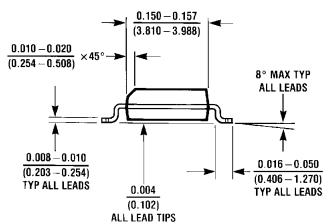
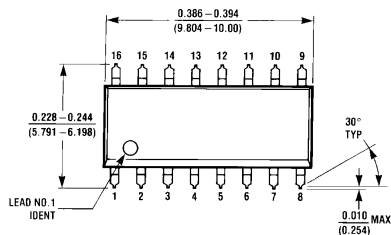
E20A (REV D)



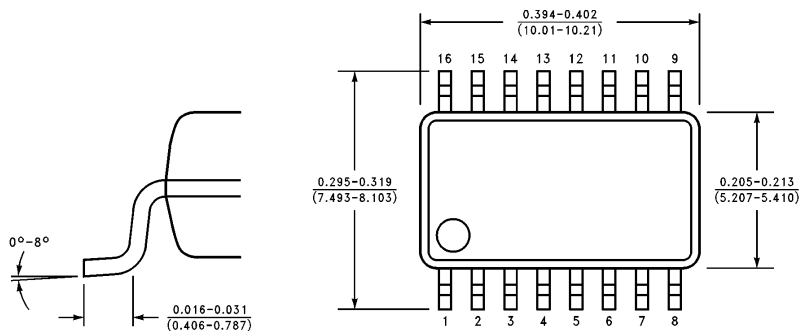
16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

J16A (REV L)

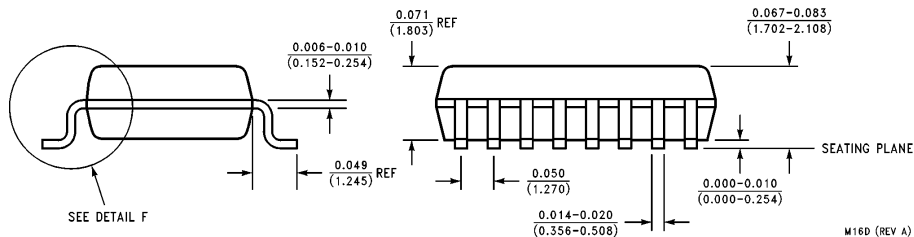
Physical Dimensions inches (millimeters) (Continued)



**16-Lead (0.150" Wide) Molded Small Outline Integrated Circuit (S)
NS Package Number M16A**

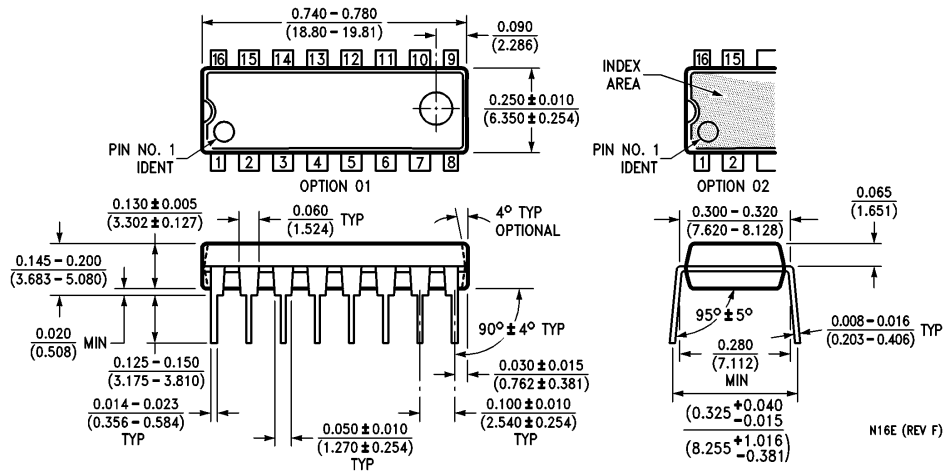


DETAIL F



**16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D**

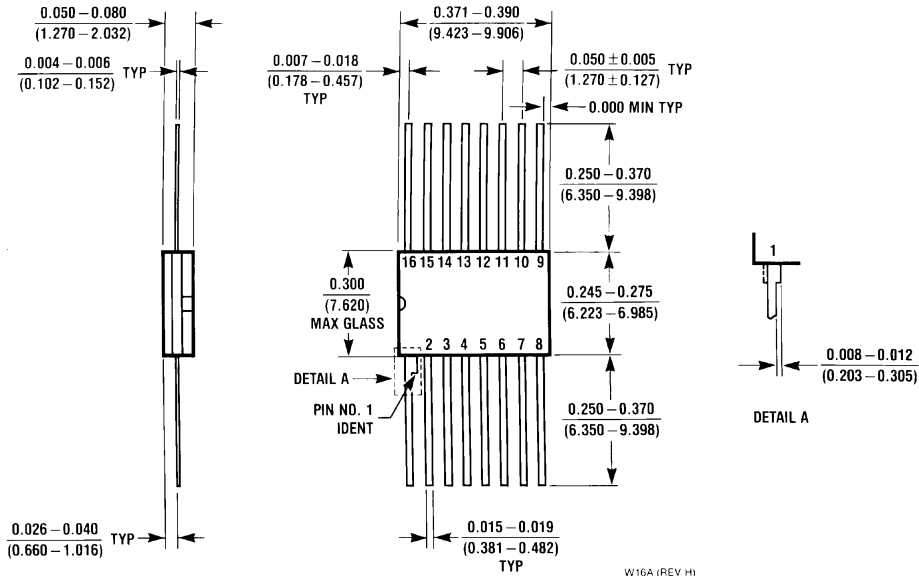
Physical Dimensions inches (millimeters) (Continued)



16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E

N16E (REV F)

Physical Dimensions inches (millimeters) (Continued)



**16-Lead Ceramic Flatpak (F)
NS Package Number W16A**

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408