

Quad serial adder/subtractor

74F385

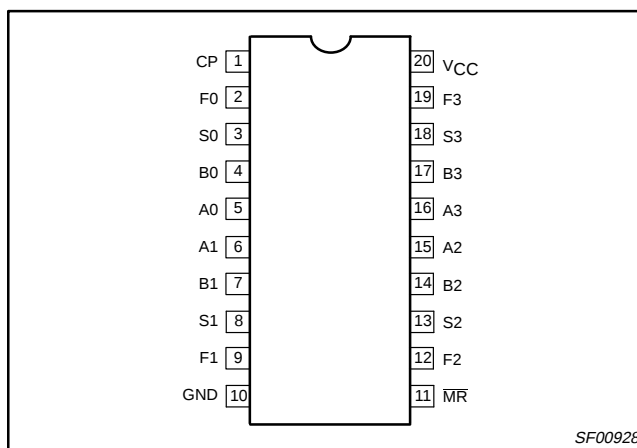
FEATURES

- Four independent adders/subtractors
- Two's complement arithmetic
- Synchronous operation
- Common Clear and Clock
- 74F385 is designed for use with serial multipliers in implementing digital filters and butterfly networks in fast Fourier transforms

DESCRIPTION

The 74F385 contains four independent adder/subtractor elements with common Clock and Master Reset. Each adder/subtractor contains a sum flip-flop and a carry flip-flop for synchronous operations. Flip-flop state changes occur on the rising edge of the Clock Pulse (CP) input signal. The Select (S) input should be Low for the Add (A plus B) mode and High for the Subtract (A minus B) mode. A Low signal on the asynchronous Master Reset ($\overline{\text{MR}}$) input clears the sum flip-flop and resets the Carry flip-flop to zero in the Add mode or presets it to one in the Subtract mode.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F385	140 MHz	55mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{\text{CC}} = 5\text{V} \pm 10\%$, $T_{\text{amb}} = 0^\circ\text{C to } +70^\circ\text{C}$
20-pin plastic DIP	N74F385N
20-pin plastic SO	N74F385D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A3	A operand inputs	1.0/1.0	20 μ A/0.6mA
B0 – B3	B operand inputs	1.0/1.0	20 μ A/0.6mA
S0 – S3	Function select inputs	1.0/1.0	20 μ A/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20 μ A/0.6mA
$\overline{\text{MR}}$	Asynchronous Master Reset input (active Low)	1.0/1.0	20 μ A/0.6mA
F0–F3	Sum or difference outputs	50/33	1.0mA/20mA

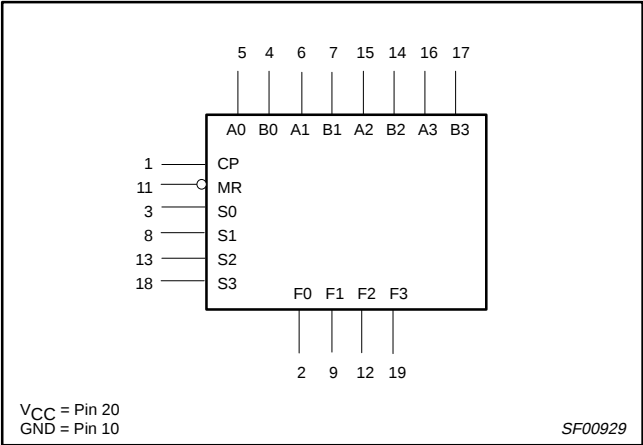
NOTE:

One (1.0) FAST unit load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

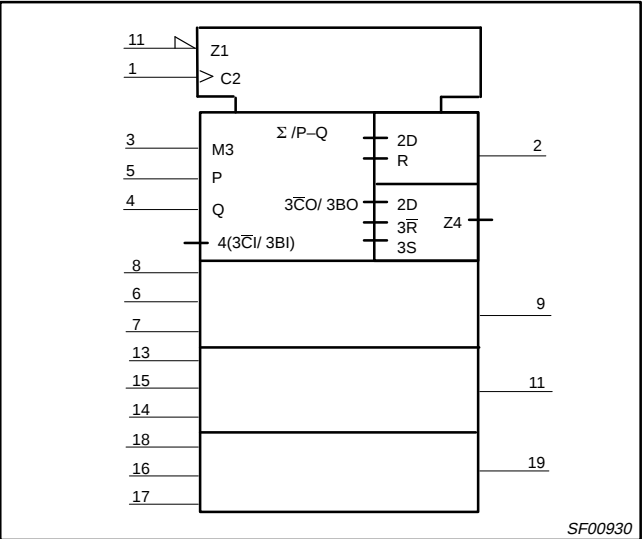
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LOGIC SYMBOL



IEC/IEEE SYMBOL



FUNCTION TABLE

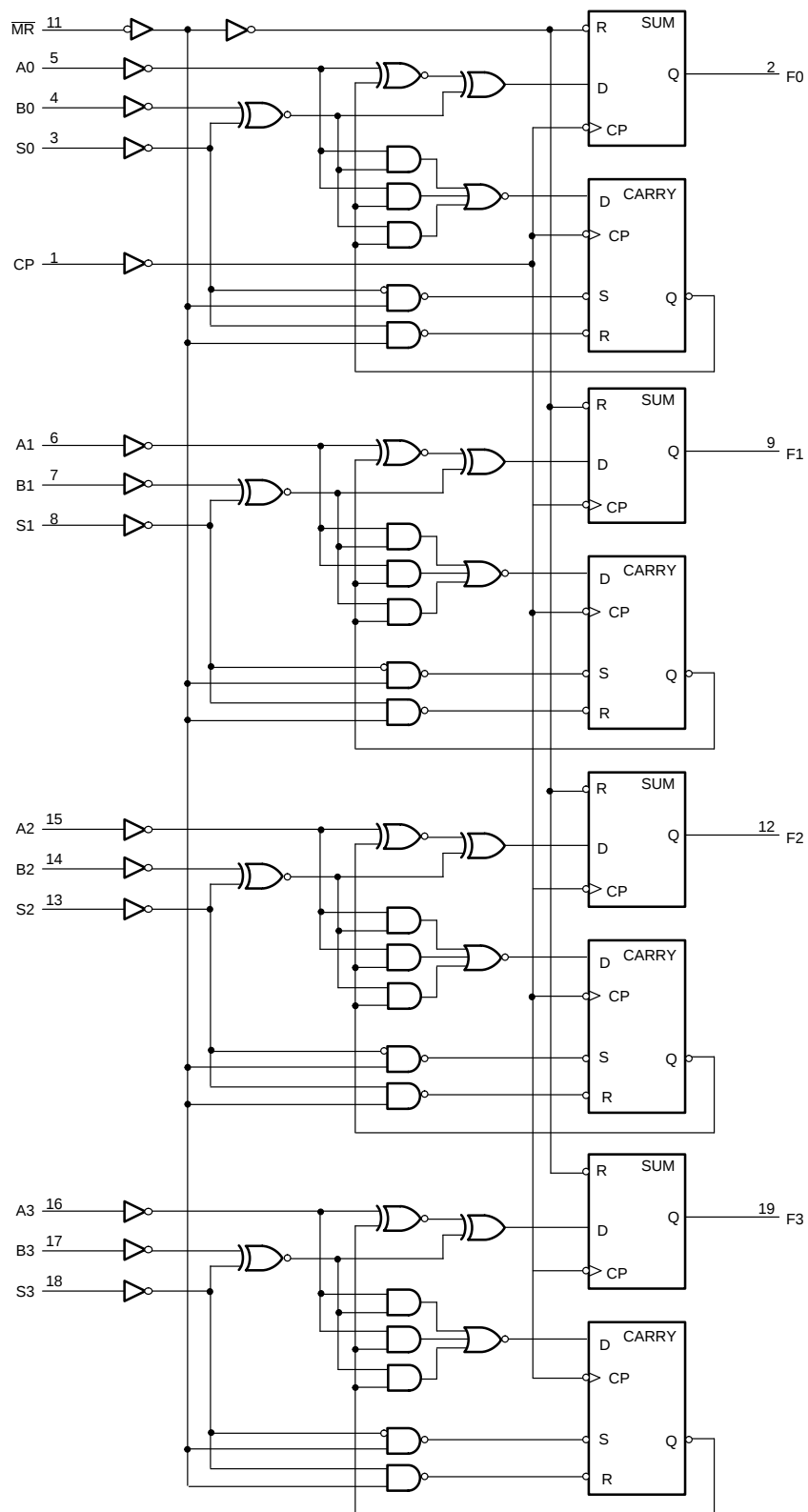
INPUTS				CARRY FLIP-FLOP STATE		OUTPUTS	OPERATING MODE
MR	S	A	B	Before↑	After↑	F	
L	L	X	X	L	L	L	Clear
L	H	X	X	H	H	L	
H	L	L	L	L	L	L	Add
H	L	L	L	H	L	H	
H	L	L	H	L	L	H	
H	L	L	H	H	H	L	
H	L	H	L	L	L	H	
H	L	H	L	H	H	L	
H	L	H	H	L	H	L	
H	L	H	H	H	H	H	
H	H	L	L	L	L	H	Subtract
H	H	L	L	H	H	L	
H	H	L	H	L	L	L	
H	H	L	H	H	L	H	
H	H	H	L	L	H	L	
H	H	H	L	H	H	H	
H	H	H	H	L	L	H	
H	H	H	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High Clock transition

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LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10

SF00931

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹		LIMITS			UNIT
				MIN	TYP ²	MAX	
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = MAX,	±10%V _{CC}	2.5			V
		V _{IH} = MIN, I _{OH} = MAX	±5%V _{CC}	2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = MAX,	±10%V _{CC}		0.35	0.50	V
		V _{IH} = MIN, I _{OL} = MAX	±5%V _{CC}		0.35	0.50	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			−0.73	−1.2	V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V				100	μA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7V				20	μA
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.5V				−20	μA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX		−60		−150	mA
I _{CC}	Supply current (total)	V _{CC} = MAX			55	80	mA

Notes:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_{amb} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS

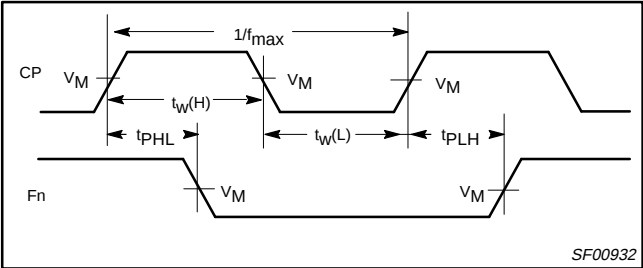
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f _{MAX}	Maximum clock frequency	Waveform 1	105	140		90		MHz
t _{PLH} t _{PHL}	Propagation delay, Cn to Fn	Waveform 1	3.0 3.5	5.0 5.5	8.0 9.0	2.5 3.5	9.0 10.0	ns
t _{PLH}	Propagation delay, $\overline{MR}$ to Fn	Waveform 2	4.0	6.5	9.5	4.0	10.5	ns

AC SETUP REQUIREMENTS

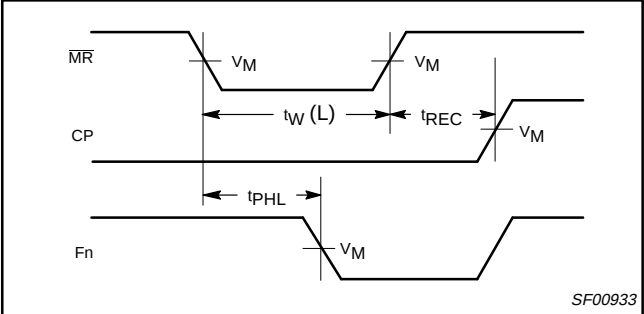
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _s (H) t _s (L)	Setup time, High or Low An, Bn or Sn to CP	Waveform 3	12.0 12.0			12.0 12.0		ns
t _h (H) t _h (L)	Hold time, High or Low An, Bn or Sn to CP	Waveform 3	0 0			0 0		ns
t _s (H) t _s (L)	CP Pulse width High or Low	Waveform 2	6.0 6.0			6.0 6.0		ns
t _w (L)	MR Pulse width Low	Waveform 2	6.0			6.0		ns
t _{REC} (L)	Recovery time MR to CP	Waveform 2	8.5			9.5		ns

AC WAVEFORMS

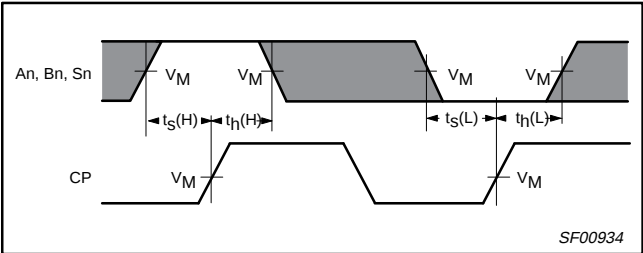
For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performances.



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 3. Data and Select Setup and Hold Times

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TEST CIRCUIT AND WAVEFORM

