

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4754V

LSI

18-element bar graph LCD driver

Product specification
File under Integrated Circuits, IC04

January 1995

18-element bar graph LCD driver

HEF4754V
LSI

DESCRIPTION

The HEF4754V drives an 18-element bar graph LCD in linear relation to the control voltage (V_c) in a pointer or thermometer mode.

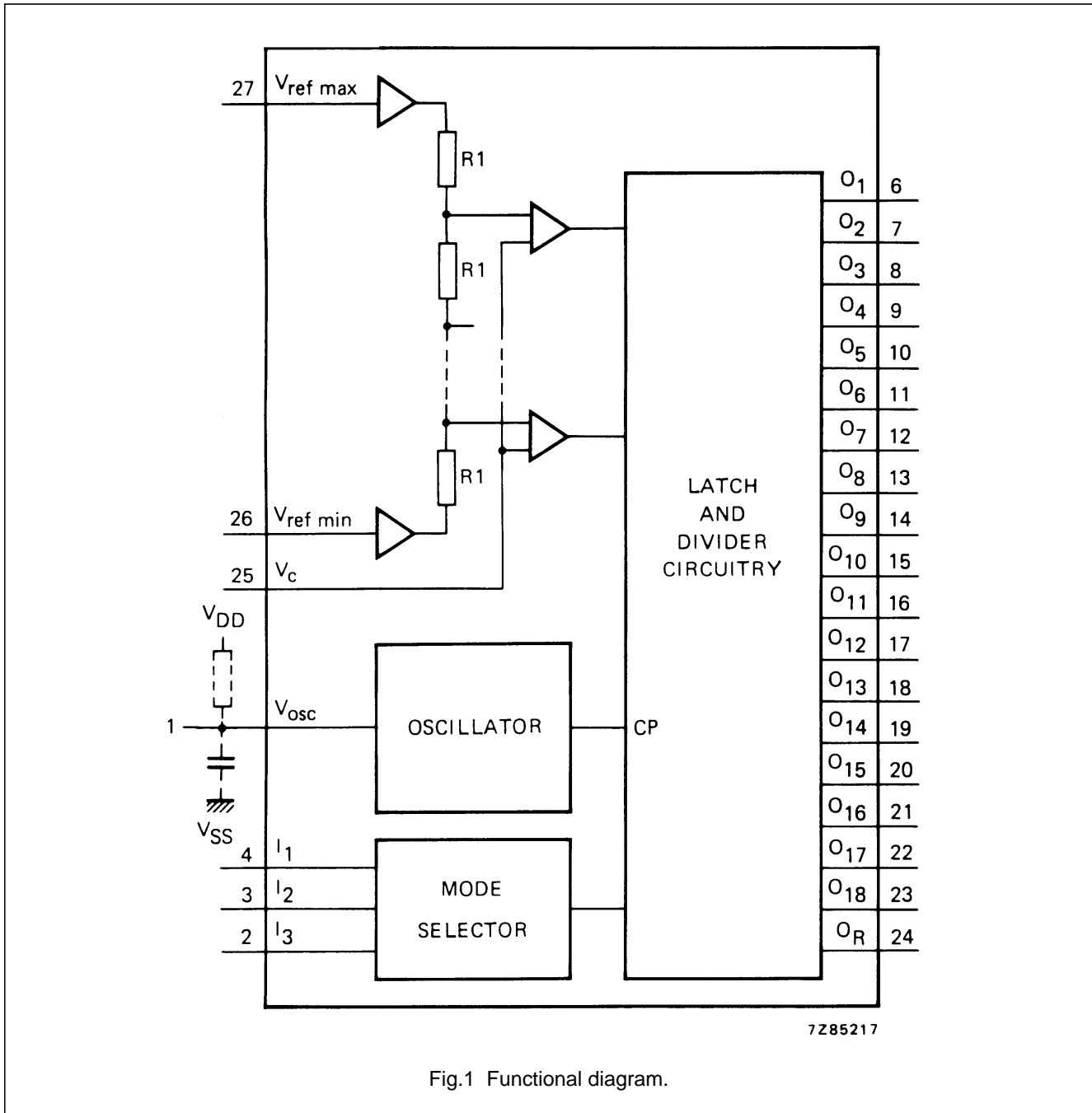


Fig.1 Functional diagram.

FAMILY DATA

See Family Specifications

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PINNING

- V_{OSC} oscillator terminal
- V_c control voltage input
- V_{ref min} | reference voltage inputs
- V_{ref max} |
- I₁ thermometer/pointer
(choice select input)
- I₂ peak value; reset/9 or 18 bars
(choice select input)
- I₃ reset; repetitively reset
(choice select input)
- O₁ to O₁₈ bar outputs
- O_R back plate output

HEF4754VP(N): 28-lead DIL; plastic
(SOT117-2)

HEF4754VD(F): 28-lead DIL; ceramic (cerdip)
(SOT135)

HEF4754VT(D): 28-lead SO; plastic
(SOT136-1)

(): Package Designator North America

FUNCTION TABLE

| I ₁ | I ₂ | I ₃ | MODE |
|----------------|----------------|----------------|---|
| L | L | X | pointer; 18 bars |
| L | H | X | pointer; 9 bars |
| H | L | X | thermometer; no peak value |
| H | H | L | thermometer; peak value, repetitively reset |
| H | H | H | thermometer; peak value, manually reset |

Note

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial

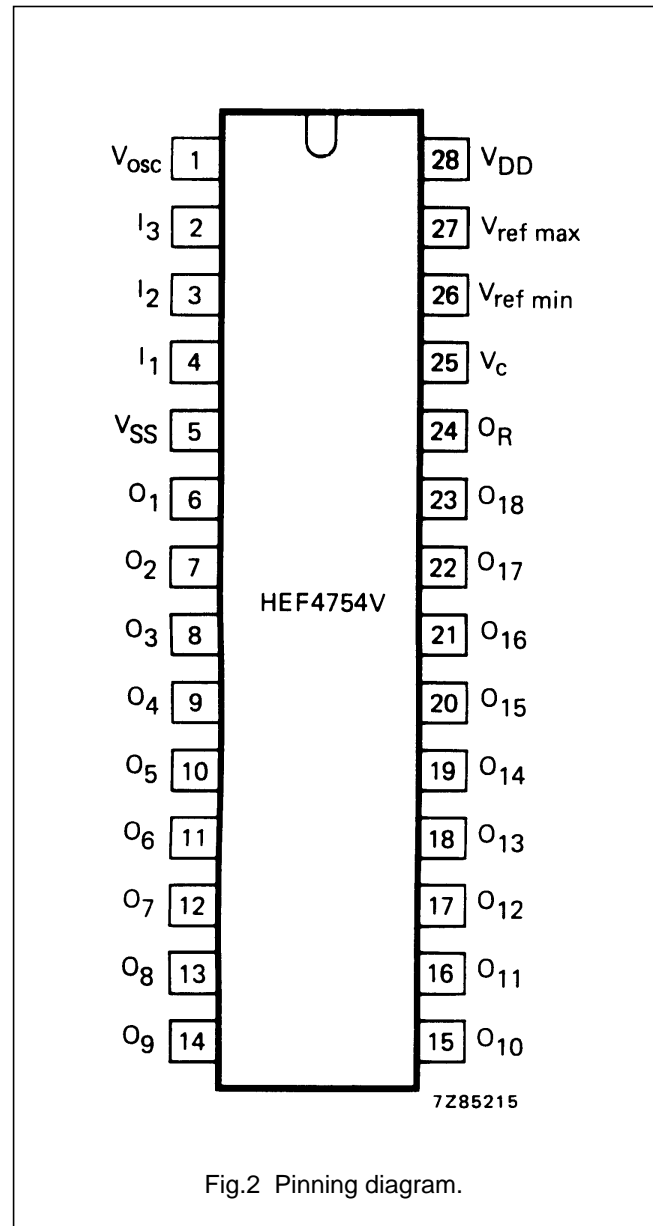


Fig.2 Pinning diagram.

18-element bar graph LCD driver

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GENERAL DESCRIPTION

The HEF4754V drives an 18-element bar graph LCD in linear relation to the control voltage (V_c) in a pointer or thermometer mode. The first bar lights up when V_c is smaller than $V_{T(\text{bar})2}$ (see equation [3] below).

In the pointer mode, the circuit can drive 9 or 18 bars; in the thermometer mode, the circuit also drives the peak value indication. This can be reset or repetitively reset, after 1,5 to 2 seconds.

The circuit has analogue and digital parts. The analogue part consists of 17 comparators, with their non-inverting inputs connected together and coupled to the control input V_c . The inverting inputs of the comparators are connected in succession to the nodes of an 18-part resistor divider.

The distance between the switching levels of the comparators is defined by the voltage difference across this divider. The extremities of the resistor divider are coupled via high-input amplifiers to the maximum reference voltage input and the minimum reference voltage input.

The digital part has one reference output (O_R) to drive the back plate, and 18 outputs (O_1 to O_{18}) to drive each bar. Three latches and some gates are incorporated for each bar output. An on-chip oscillator (1024 Hz) with external R and C drives the circuit. The outputs are driven at 64 Hz. The select inputs I_1 to I_3 are provided with an on-chip pull-up element, and they may therefore be left floating (equals HIGH state).

LINEARITY

$V_{DD} = 10 \text{ V}$; $V_{\text{ref max}} = 9,5 \text{ V}$; $V_{\text{ref min}} = 0,5 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$
 $\Delta V_1 = 250 \text{ mV}$ (this is the tolerance of the step voltage).

$$V_{\text{step}} = V_{\text{step}'''} + \Delta V_1 \quad [1]$$

$V_{\text{step}'}$ is the (internal) voltage drop across the resistor-ladder network.

$$V_{\text{step}'} = \frac{(V_{\text{ref max}} \pm \Delta V_2) - (V_{\text{ref min}} \pm \Delta V_2)}{18} \quad [2]$$

ΔV_2 is the maximum offset voltage spread of the on-chip voltage follower.

$\Delta V_2 = 250 \text{ mV}$.

The linearity is guaranteed for $V_{DD} > 10 \text{ V}$.

The monotony between $V_{DD} = 5 \text{ V}$ and 10 V is guaranteed. During ramping-up of the input voltage a maximum of two bars might be activated simultaneously.

ABSOLUTE VOLTAGE TRIGGER LEVEL

The absolute voltage trigger level at the V_c pin is $V_{T(\text{bar})n}$;

$$V_{T(\text{bar})n} = \{V_{\text{ref min}} \pm \Delta V_2^*\} + \{(n-1)V_{\text{step}'} \pm \Delta V_1\}, \text{ in which} \quad [3]$$

$n = \text{number of bars}; 2 \leq n \leq 18$.

For $n = 1$ (first bar) see text above.

Note

* For ΔV_2 the same sign (+ or -) should be used as in equation [2].

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LSI**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | |
|---------------------------------------|-----------|--------------------------|
| Supply voltage | V_{DD} | -0,5 to + 18 V |
| Voltage on any input | V_I | -0,5 to $V_{DD} + 0,5$ V |
| D.C. current into any input or output | $\pm I_I$ | max 10 mA |
| Storage temperature | T_{stg} | -25 to + 125 °C |
| Operating ambient temperature | T_{amb} | -20 to + 85 °C |

DC CHARACTERISTICS $V_{SS} = 0$ V

| | V_{DD} V | SYMBOL | T_{amb} (°C) | | | | | | | NOTES | |
|--|---------------|--------------|----------------|------|-------|------|------|------|------|---------|---|
| | | | -40 | | + 25 | | | + 85 | | | |
| | | | MIN. | MAX. | MIN. | TYP. | MAX. | MIN. | MAX. | | |
| Quiescent device current | 5 | I_{DD} | - | - | - | - | - | - | - | μ A | 1 |
| | 10 | | - | - | - | - | 1000 | - | - | μ A | |
| | 15 | | - | - | - | - | 1600 | - | - | μ A | |
| Input leakage current (except select inputs) | 5 | $\pm I_{IN}$ | - | - | - | - | 100 | - | - | nA | 2 |
| | 10 | | - | - | - | - | 100 | - | - | nA | |
| | 15 | | - | - | - | - | 100 | - | - | nA | |
| Input voltage HIGH select inputs | 5 | V_{IH} | 3,5 | - | 3,5 | - | - | 3,5 | - | V | |
| | 10 | | 7,0 | - | 7,0 | - | - | 7,0 | - | V | |
| | 15 | | 11,0 | - | 11,0 | - | - | 11,0 | - | V | |
| Input voltage LOW select inputs | 5 | V_{IL} | - | 1,5 | - | - | 1,5 | - | 1,5 | V | |
| | 10 | | - | 3,0 | - | - | 3,0 | - | 3,0 | V | |
| | 15 | | - | 4,0 | - | - | 4,0 | - | 4,0 | V | |
| Output voltage HIGH | 5 | V_{OH} | 4,99 | - | 4,99 | - | - | 4,95 | - | V | 3 |
| | 10 | | 9,99 | - | 9,99 | - | - | 9,95 | - | V | |
| | 15 | | - | - | 14,99 | - | - | - | - | V | |
| Output voltage LOW | 5 | V_{OL} | - | 0,01 | - | - | 0,01 | - | 0,05 | V | 3 |
| | 10 | | - | 0,01 | - | - | 0,01 | - | 0,05 | V | |
| | 15 | | - | 0,01 | - | - | 0,01 | - | 0,05 | V | |
| Output current HIGH | 5 | $-I_{OH}$ | 0,36 | - | 0,3 | - | - | 0,24 | - | mA | 4 |
| | 10 | | 0,80 | - | 0,7 | - | - | 0,56 | - | mA | |
| | 15 | | 3,0 | - | 2,8 | - | - | 2,60 | - | mA | |
| Output current LOW | 5 | I_{OL} | 0,34 | - | 0,3 | - | - | 0,24 | - | mA | 5 |
| | 10 | | 1,00 | - | 0,9 | - | - | 0,72 | - | mA | |
| | 15 | | 4,40 | - | 4,0 | - | - | 3,20 | - | mA | |
| Input voltage control input V_c | 5 | V_{IC} | - | - | 0 | - | 5 | - | - | V | 6 |
| | 10 | | - | - | 0 | - | 10 | - | - | V | |
| | 15 | | - | - | 0 | - | 15 | - | - | V | |

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| | V _{DD} V | SYMBOL | T _{amb} (°C) | | | | | | NOTES | | |
|----------------------------|----------------------|--------------------|-----------------------|------|------|------|------|------|-------|------|-------|
| | | | -40 | | + 25 | | | + 85 | | | |
| | | | MIN. | MAX. | MIN. | TYP. | MAX. | MIN. | | MAX. | |
| Max. input voltage | 5 | | – | – | 4,5 | – | 4,5 | – | – | V | 6 |
| V _{ref max} input | 10 | V _{IRmax} | – | – | 4,5 | – | 9,5 | – | – | V | |
| | 15 | | – | – | 4,5 | – | 14,5 | – | – | V | |
| Min. input voltage | 5 | | – | – | 0,5 | – | 0,5 | – | – | V | 6 |
| V _{ref min} input | 10 | V _{IRmin} | – | – | 0,5 | – | 5,5 | – | – | V | |
| | 15 | | – | – | 0,5 | – | 10,5 | – | – | V | |
| Operating supply current | 10 | I _{DD} | – | – | – | 750 | – | – | – | μA | Fig.3 |

Notes

1. V_{ref min} = 0,5 V; V_{ref max} = 9,5 V; V_{osc} = V_c = 0 V; I₁, I₂ and I₃ at V_{DD}.
2. Pin under test at V_{SS} or V_{DD}, all other inputs simultaneously at V_{SS} or V_{DD}.
3. I_O = 0; all inputs at V_{SS} or V_{DD}.
4. At V_{DD} = 5 V: V_{OH} = 4,5 V.
At V_{DD} = 10 V: V_{OH} = 9,5 V.
At V_{DD} = 15 V: V_{OH} = 13,5 V.
5. At V_{DD} = 5 V: V_{OL} = 0,4 V; inputs at V_{SS} or V_{DD}.
At V_{DD} = 10 V: V_{OL} = 0,5 V; inputs at V_{SS} or V_{DD}.
At V_{DD} = 15 V: V_{OL} = 1,5 V; inputs at V_{SS} or V_{DD}.
6. V_{ref min} + 4 V < V_{ref max}.

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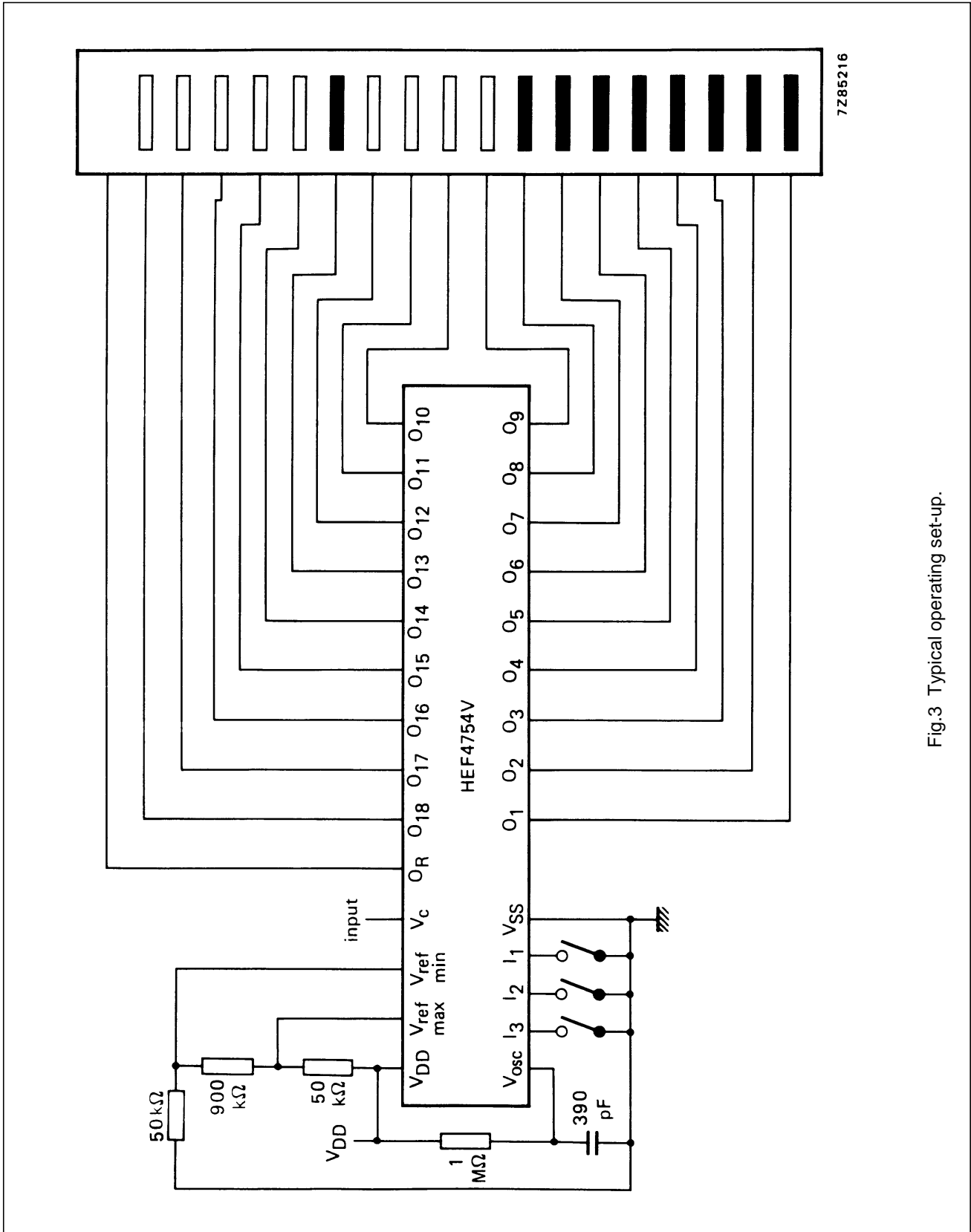


Fig.3 Typical operating set-up.