

International IR Rectifier

PD - 91386C

IRF5305S/L

HEXFET® Power MOSFET

- Advanced Process Technology
- Surface Mount (IRF5305S)
- Low-profile through-hole (IRF5305L)
- 175°C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

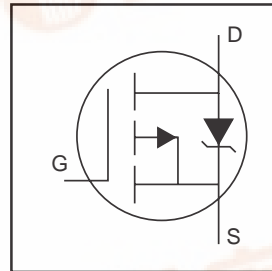
The through-hole version (IRF5305L) is available for low-profile applications.

Absolute Maximum Ratings

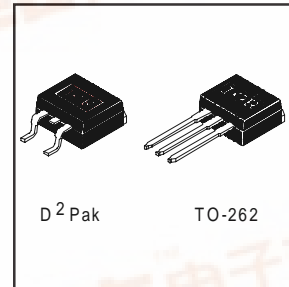
	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -10\text{V}^{\text{⑤}}$	-31	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -10\text{V}^{\text{⑤}}$	-22	
I_{DM}	Pulsed Drain Current ① ⑤	-110	
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation	3.8	W
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	110	W
	Linear Derating Factor	0.71	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ^{② ⑤}	280	mJ
I_{AR}	Avalanche Current ^①	-16	A
E_{AR}	Repetitive Avalanche Energy ^①	11	mJ
dv/dt	Peak Diode Recovery dv/dt ③ ⑤	-5.8	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)**	—	40	



$V_{DSS} = -55\text{V}$
$R_{DS(on)} = 0.06\Omega$
$I_D = -31\text{A}$



D²Pak

TO-262

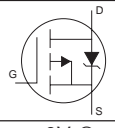
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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-55	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.034	—	V/°C	Reference to $25^\circ\text{C}, I_D = -1mA$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.06	Ω	$V_{GS} = -10V, I_D = -16A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	8.0	—	—	S	$V_{DS} = -25V, I_D = -16A$ ⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	$V_{DS} = -55V, V_{GS} = 0V$
		—	—	-250		$V_{DS} = -44V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	63	nC	$I_D = -16A$
Q_{gs}	Gate-to-Source Charge	—	—	13		$V_{DS} = -44V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	29		$V_{GS} = -10V$, See Fig. 6 and 13 ④ ⑤
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	$V_{DD} = -28V$
t_r	Rise Time	—	66	—		$I_D = -16A$
$t_{d(off)}$	Turn-Off Delay Time	—	39	—		$R_G = 6.8\Omega$
t_f	Fall Time	—	63	—		$R_D = 1.6\Omega$, See Fig. 10 ④ ⑤
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	1200	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	520	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	250	—		$f = 1.0\text{MHz}$, See Fig. 5 ⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-31	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-110		
V_{SD}	Diode Forward Voltage	—	—	-1.3	V	$T_J = 25^\circ\text{C}, I_S = -16A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	71	110	ns	$T_J = 25^\circ\text{C}, I_F = -16A$
Q_{rr}	Reverse Recovery Charge	—	170	250	nC	$di/dt = -100A/\mu s$ ④ ⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② $V_{DD} = -25V$, Starting $T_J = 25^\circ\text{C}$, $L = 2.1\text{mH}$
 $R_G = 25\Omega, I_{AS} = -16A$. (See Figure 12)
- ③ $I_{SD} \leq -16A, di/dt \leq -280A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ Uses IRF5305 data and test conditions

** When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

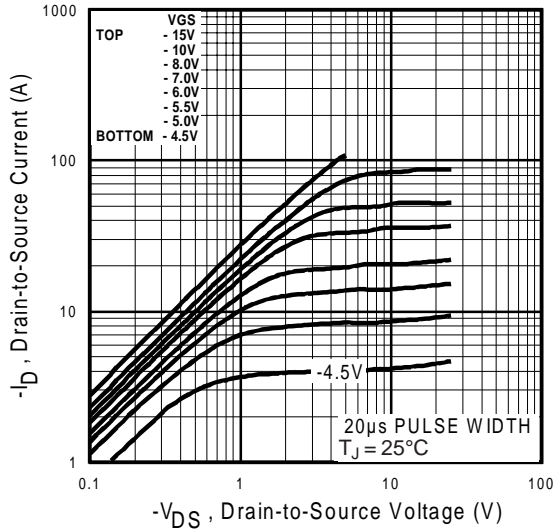


Fig 1. Typical Output Characteristics

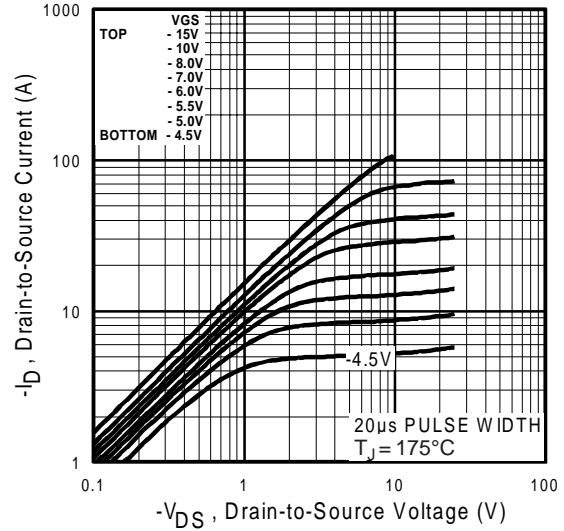


Fig 2. Typical Output Characteristics

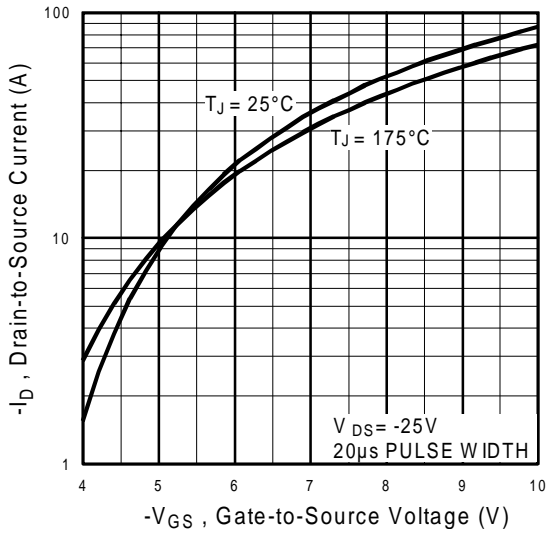


Fig 3. Typical Transfer Characteristics

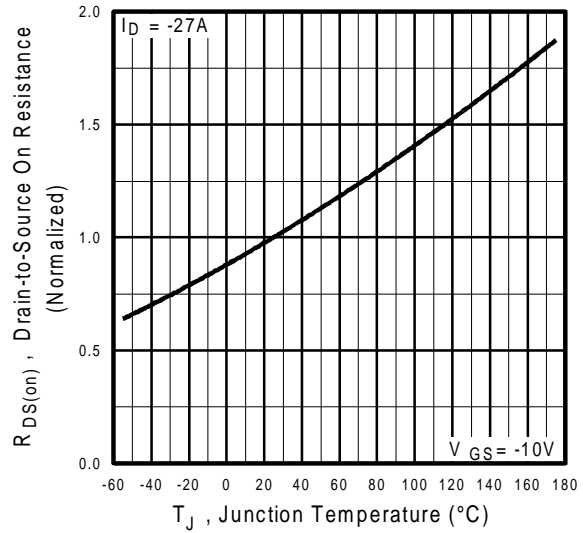


Fig 4. Normalized On-Resistance Vs. Temperature

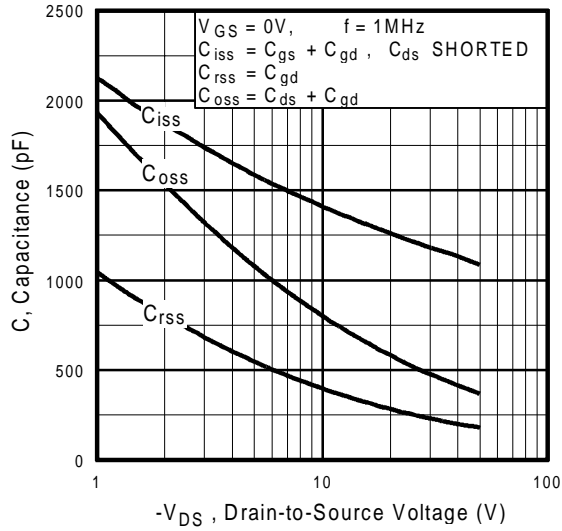


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

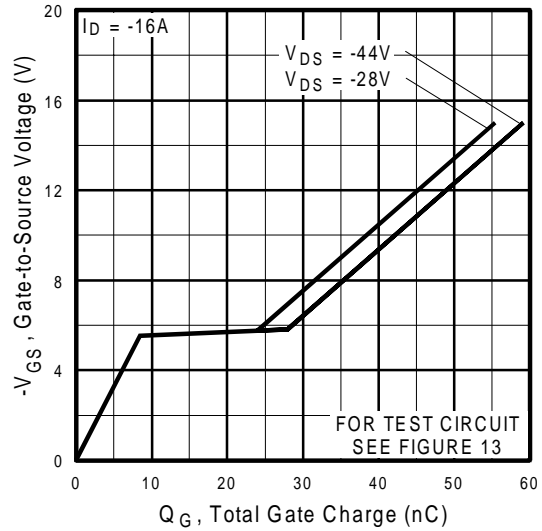


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

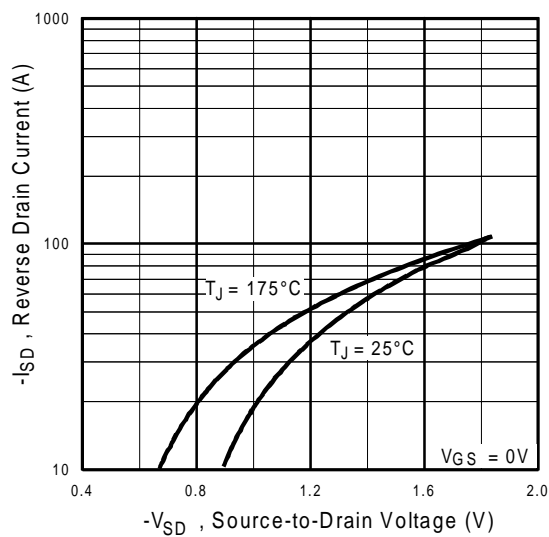


Fig 7. Typical Source-Drain Diode Forward Voltage

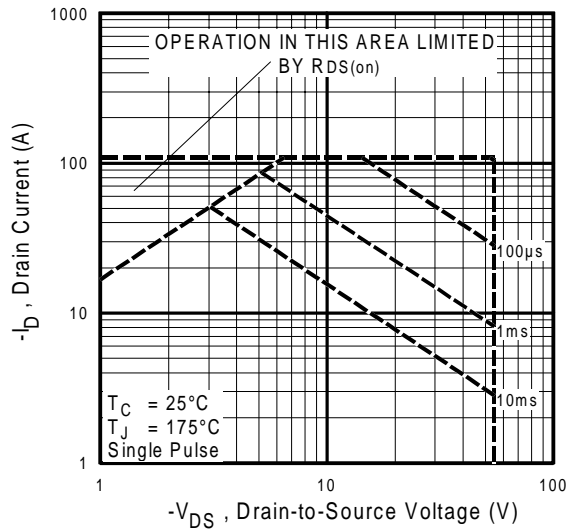


Fig 8. Maximum Safe Operating Area

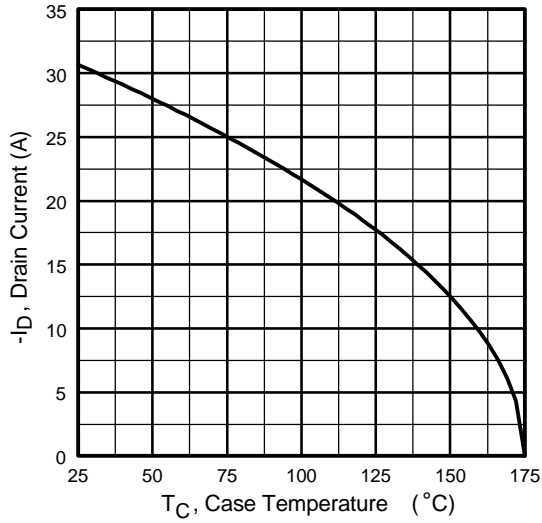


Fig 9. Maximum Drain Current Vs. Case Temperature

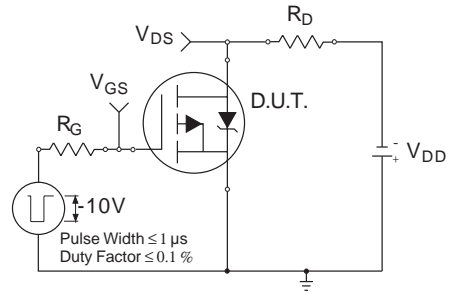


Fig 10a. Switching Time Test Circuit

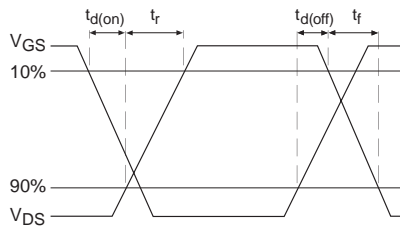


Fig 10b. Switching Time Waveforms

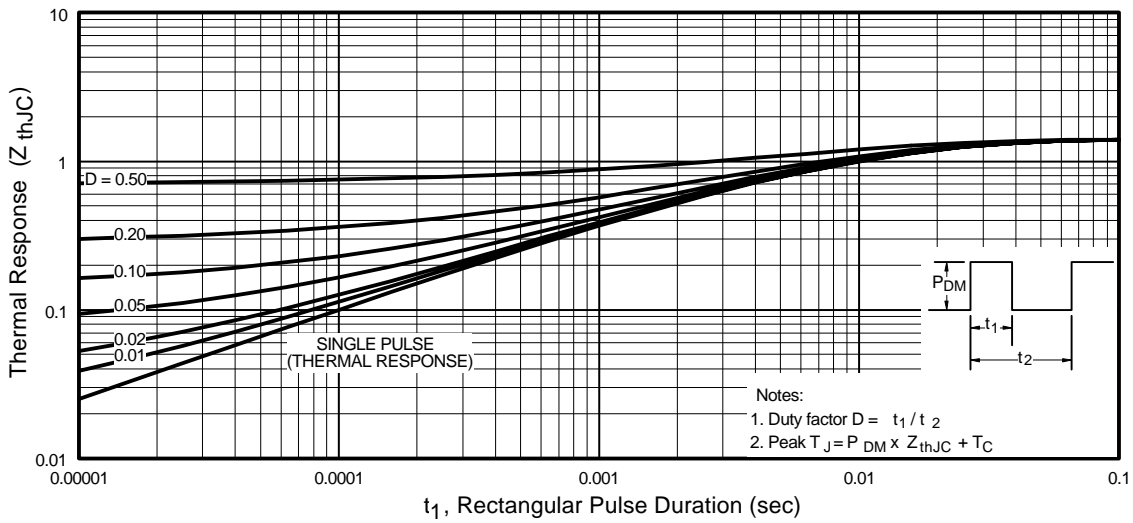


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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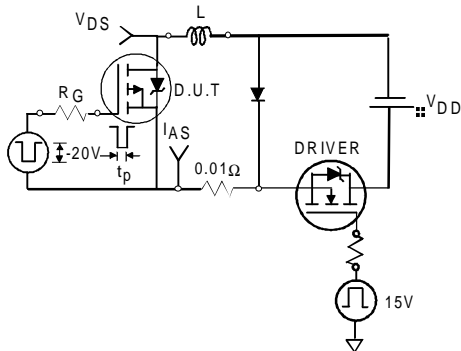


Fig 12a. Unclamped Inductive Test Circuit

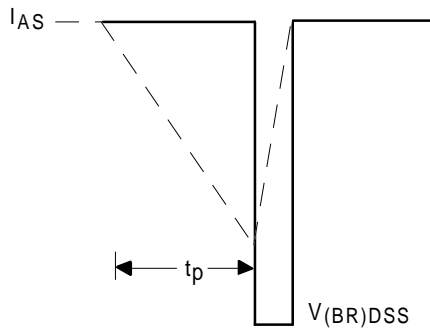


Fig 12b. Unclamped Inductive Waveforms

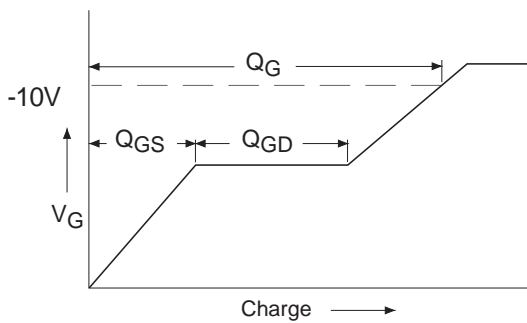


Fig 13a. Basic Gate Charge Waveform

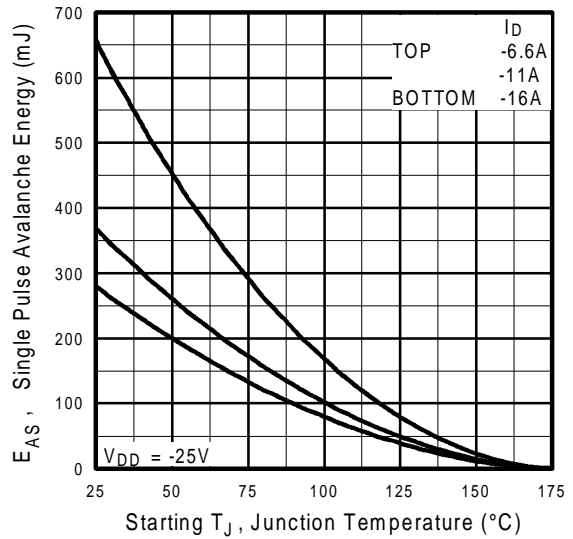


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

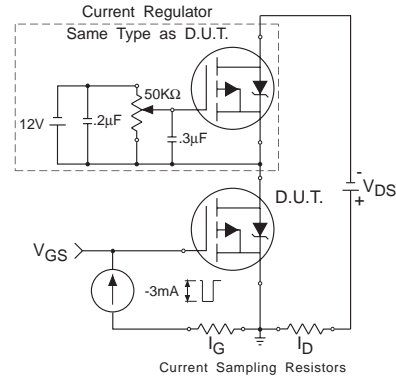
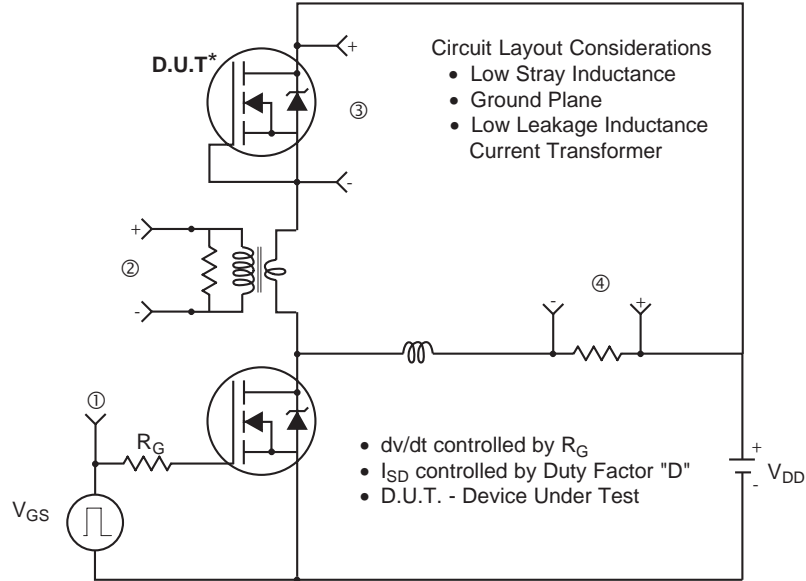
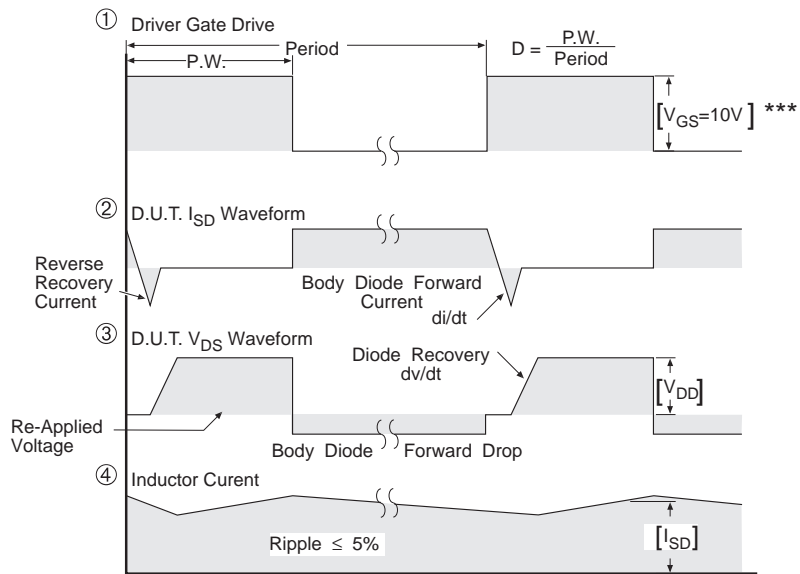


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



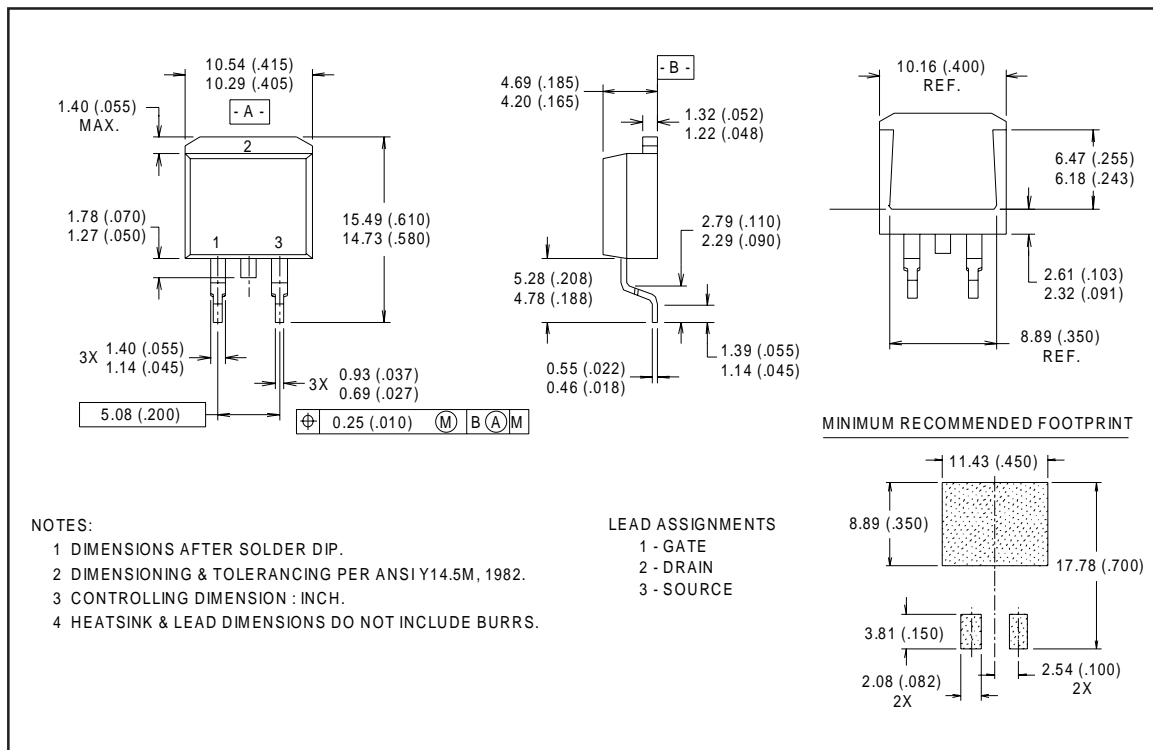
*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. For P-Channel HEXFETS

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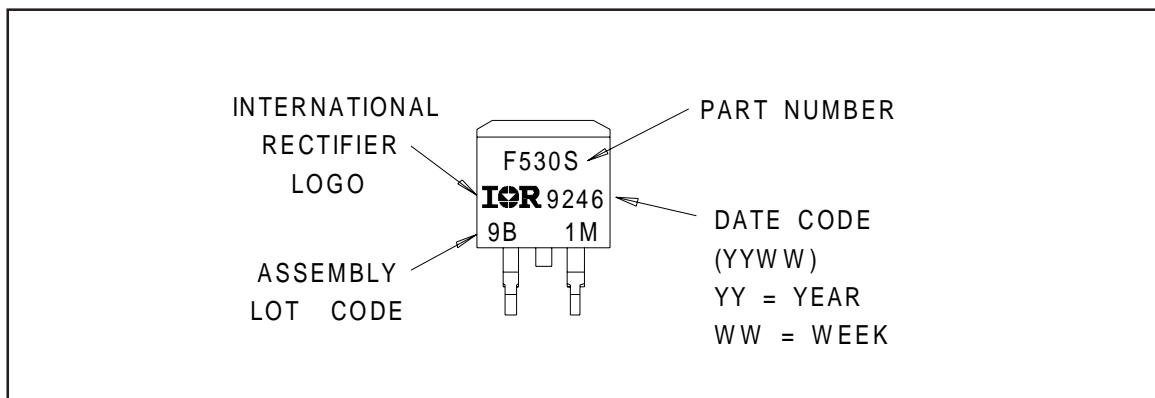
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D²Pak Package Outline



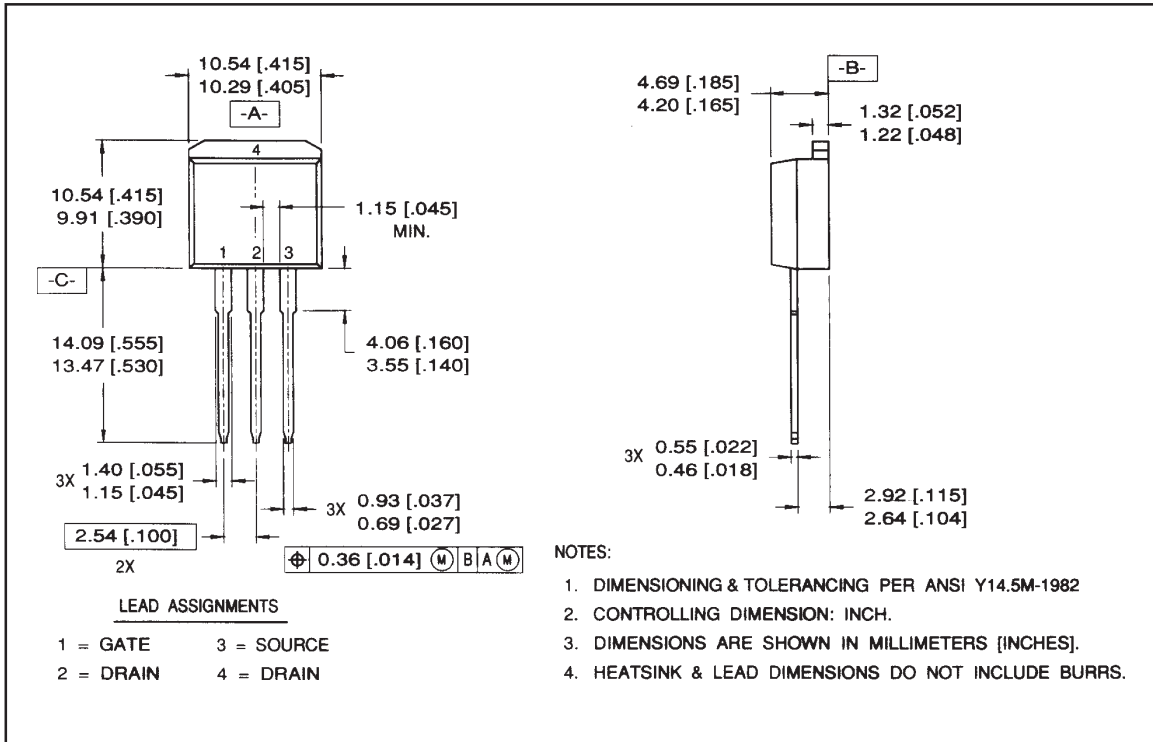
Part Marking Information

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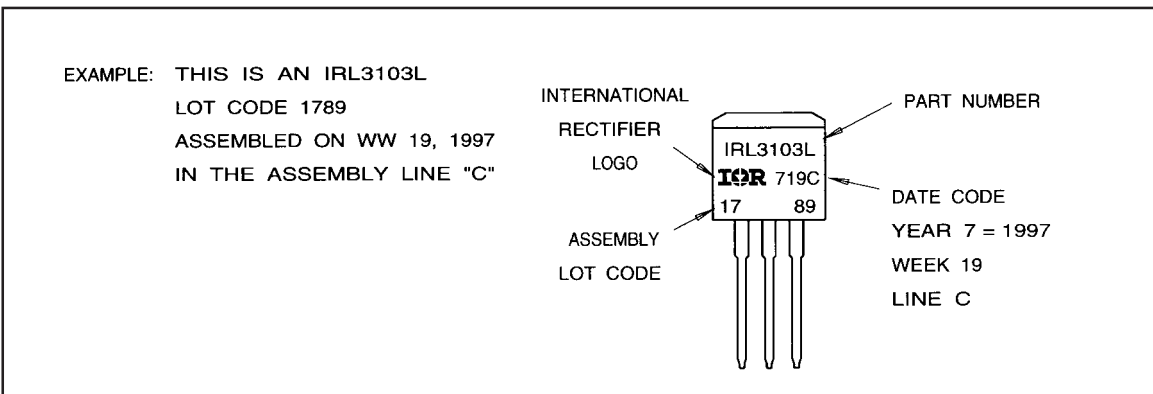
Package Outline

TO-262 Outline



Part Marking Information

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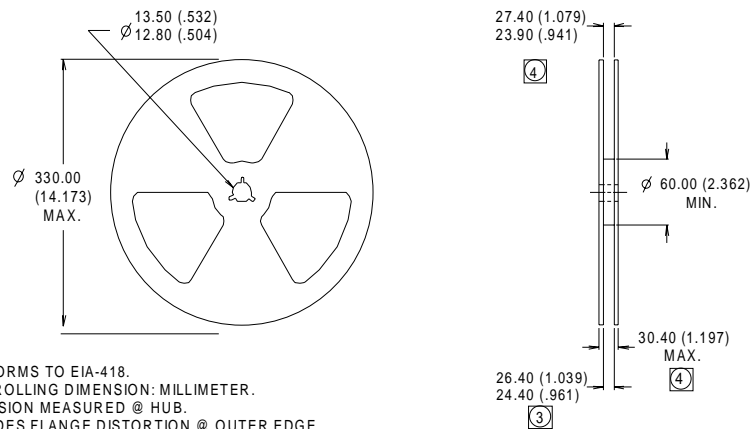
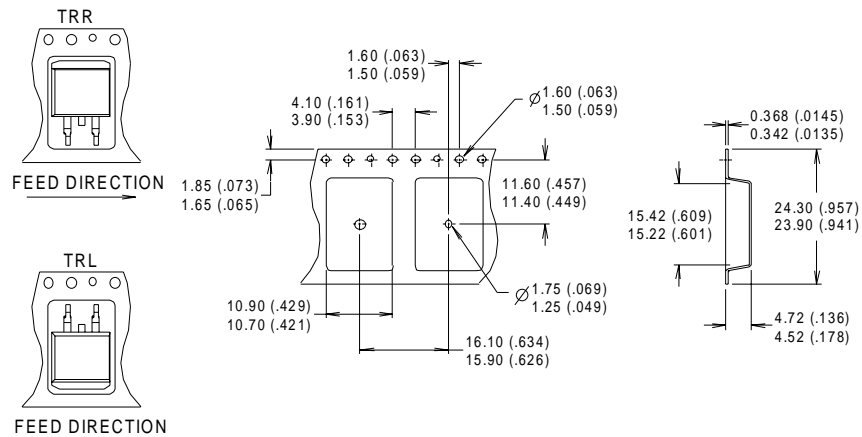


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Tape & Reel Information

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