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74F563 Octal D-Type Latch with 3-STATE Outputs

General Description

The 74F563 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (\overline{OE}) inputs.

This device is functionally identical to the 74F573, but has inverted outputs.

Features

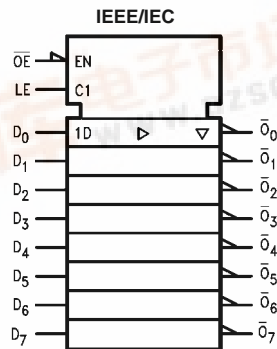
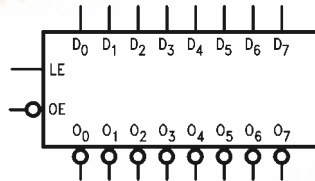
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 74F573

Ordering Code:

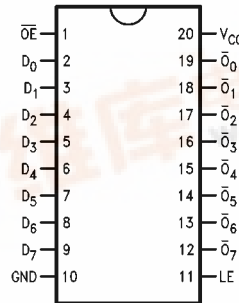
Order Number	Package Number	Package Description
74F563SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F563SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F563PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



74F563 Octal D-Type Latch with 3-STATE Outputs



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0 - D_7	Data Inputs	1.0/1.0	20 μ A/-0.6 mA
LE	Latch Enable Input (Active HIGH)	1.0/1.0	20 μ A/-0.6 mA
\overline{OE}	3-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μ A/-0.6 mA
\overline{O}_0 - \overline{O}_7	3-STATE Latch Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

Functional Description

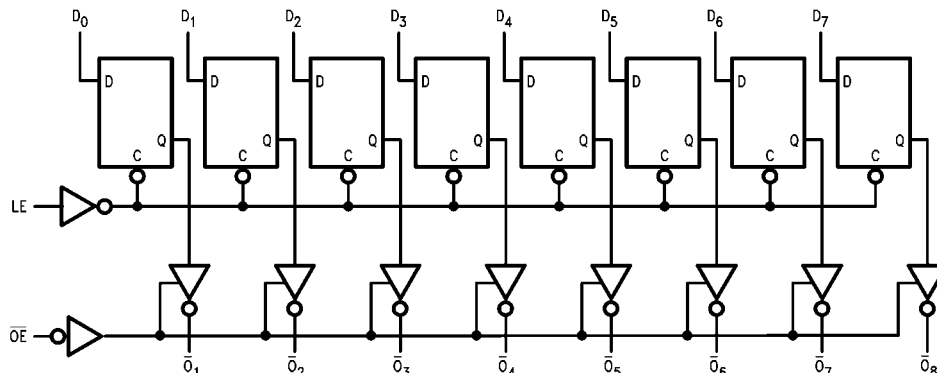
The 74F563 contains eight D-type latches with 3-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are in the bi-state mode. When \overline{OE} is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Function Table

Inputs			Internal	Output	Function
\overline{OE}	LE	D	Q	O	
H	X	X	X	Z	High Z
H	H	L	H	Z	High Z
H	H	H	L	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	H	H	Transparent
L	H	H	L	L	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I _{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

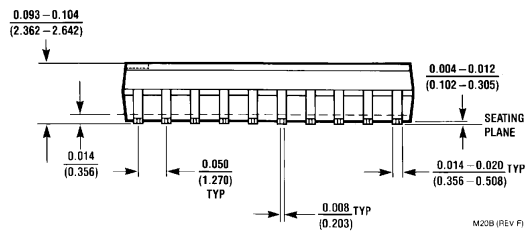
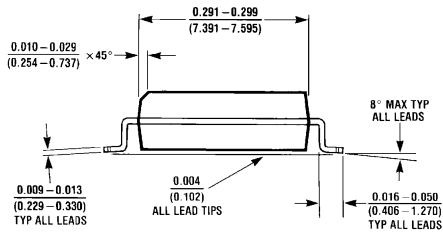
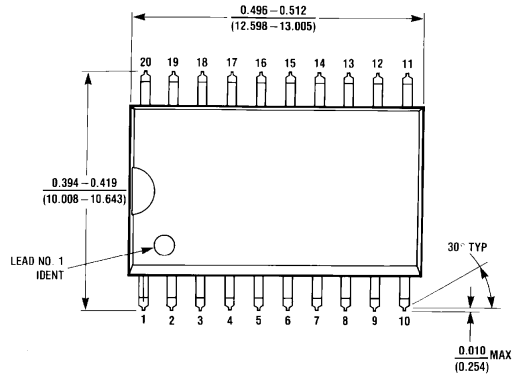
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC} 10% V _{CC} 5% V _{CC} 5% V _{CC}	2.5 2.4 2.7 2.7		V	Min	I _{OH} = -1 mA I _{OH} = -3 mA I _{OH} = -1 mA I _{OH} = -3 mA
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5	V	Min	I _{OL} = 24 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OZH}	Output Leakage Current			50	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current			-50	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V
I _{CC1}	Power Supply Current		40	61	mA	Max	V _O = LOW
I _{CC2}	Power Supply Current		40	61	mA	Max	V _O = HIGH Z

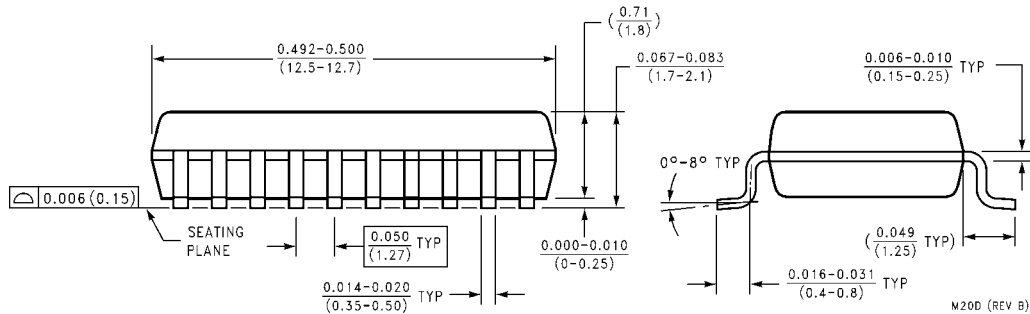
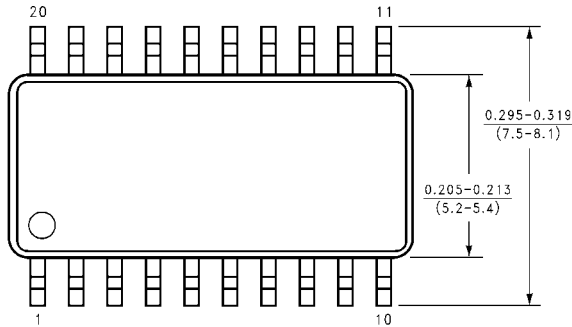
AC Electrical Characteristics									
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	3.5		8.5	3.0	10.5	3.0	9.5	ns
t_{PHL}	D_n to \overline{O}_n	2.5		6.5	2.0	7.5	2.0	7.0	
t_{PLH}	Propagation Delay	4.5		9.5	4.0	11.0	4.0	10.5	ns
t_{PHL}	LE to \overline{O}_n	3.0		7.0	2.5	7.5	2.5	7.0	
t_{PZH}	Output Enable Time	2.0		7.5	2.0	9.5	2.0	9.0	ns
t_{PZL}		3.0		8.5	2.5	10.0	1.5	9.5	
t_{PHZ}	Output Disable Time	1.5		5.5	1.5	7.0	1.5	6.5	
t_{PLZ}		1.5		5.5	1.5	5.5	1.5	5.5	
AC Operating Requirements									
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		Units	
		Min	Max	Min	Max	Min	Max		
$t_S(H)$	Setup Time, HIGH or LOW	2.0		2.0		2.0		ns	
$t_S(L)$	D_n to LE	2.0		2.0		2.0			
$t_H(H)$	Hold Time, HIGH or LOW	3.0		3.0		3.0		ns	
$t_H(L)$	D_n to LE	3.0		3.0		3.0			
$t_W(H)$	LE Pulse Width, HIGH	4.0		4.0		4.0		ns	

Physical Dimensions inches (millimeters) unless otherwise noted



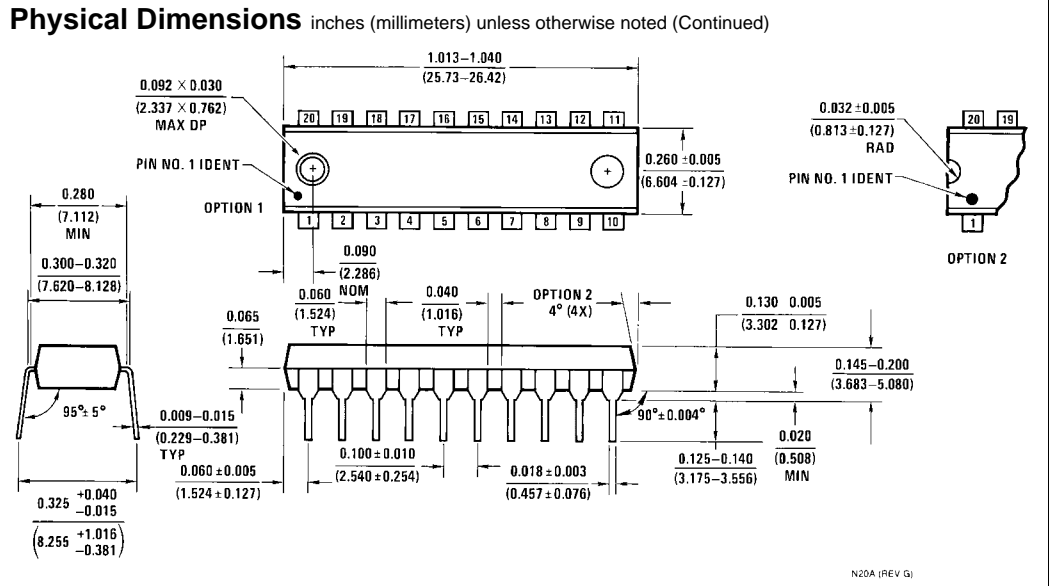
M20B (REV F)

**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B**



M20D (REV B)

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

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