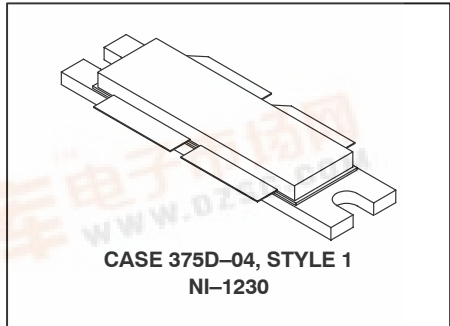


The RF Sub-Micron MOSFET Line  
**RF Power Field Effect Transistor**  
**N-Channel Enhancement-Mode Lateral MOSFET**



**1990 MHz, 38 W AVG.,  
 2 x W-CDMA, 28 V  
 LATERAL N-CHANNEL  
 RF POWER MOSFET**



Designed for W-CDMA base station applications with frequencies from 1930 to 1990 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

- Typical 2-carrier W-CDMA Performance for  $V_{DD} = 28$  Volts,  $I_{DQ} = 2 \times 800$  mA,  $f_1 = 1955$  MHz,  $f_2 = 1965$  MHz, Channel Bandwidth = 3.84 MHz, Adjacent Channels Measured over 3.84 MHz BW @  $f_1 - 5$  MHz and  $f_2 + 5$  MHz. Distortion Products Measured over a 3.84 MHz BW @  $f_1 - 10$  MHz and  $f_2 + 10$  MHz, Each Carrier Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.
  - Output Power — 38 Watts Avg.
  - Power Gain — 14 dB
  - Efficiency — 26%
  - IM3 — -37.5 dBc
  - ACPR — -41 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 1960 MHz, 120 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Qualified Up to a Maximum of 32  $V_{DD}$  Operation
- In Tape and Reel. R6 Suffix = 150 Units per 56 mm, 13 inch Reel.

**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	65	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	407 2.3	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	$T_J$	200	$^\circ\text{C}$
CW Operation	CW	120	Watts

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Case Temperature $80^\circ\text{C}$ , 120 W CW Case Temperature $80^\circ\text{C}$ , 38 W CW	$R_{\theta JC}$	0.43 0.43	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

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## ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)
Charge Device Model	C7 (Minimum)

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS (1)

Zero Gate Voltage Drain Leakage Current (V <sub>DS</sub> = 65 Vdc, V <sub>GS</sub> = 0 Vdc)	I <sub>DSS</sub>	—	—	10	μA <sub>dc</sub>
Zero Gate Voltage Drain Leakage Current (V <sub>DS</sub> = 28 Vdc, V <sub>GS</sub> = 0)	I <sub>DSS</sub>	—	—	1	μA <sub>dc</sub>
Gate–Source Leakage Current (V <sub>GS</sub> = 5 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	—	—	1	μA <sub>dc</sub>

### ON CHARACTERISTICS (1)

Gate Threshold Voltage (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 200 μA <sub>dc</sub> )	V <sub>GS(th)</sub>	2.5	2.7	3.5	Vdc
Gate Quiescent Voltage (V <sub>DS</sub> = 28 Vdc, I <sub>D</sub> = 850 mA <sub>dc</sub> )	V <sub>GS(Q)</sub>	—	3.6	—	Vdc
Drain–Source On–Voltage (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 2 Adc)	V <sub>DS(on)</sub>	—	0.26	0.3	Vdc
Forward Transconductance (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 2 Adc)	g <sub>fs</sub>	—	5	—	S

### DYNAMIC CHARACTERISTICS (1)

Reverse Transfer Capacitance (V <sub>DS</sub> = 28 Vdc ± 30 mV(rms) <sub>ac</sub> @ 1 MHz, V <sub>GS</sub> = 0 Vdc)	C <sub>rss</sub>	—	1.7	—	pF
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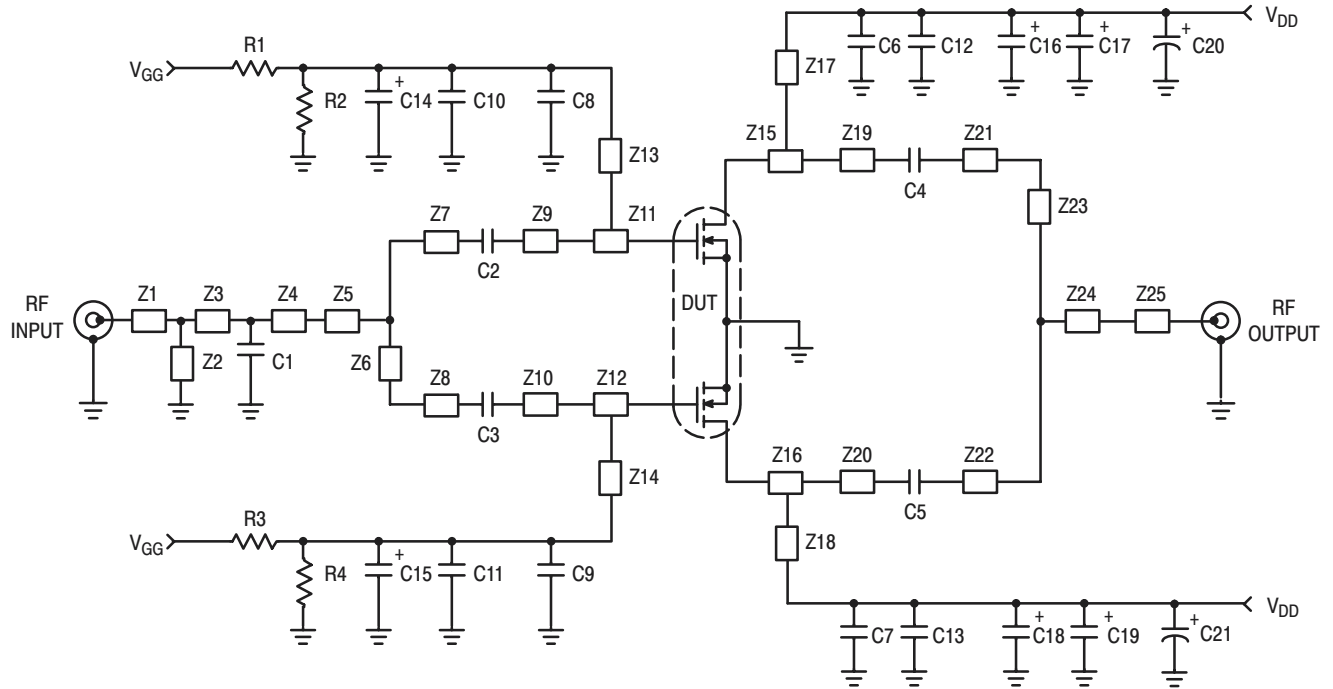
### FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2) 2–carrier W–CDMA, 3.84 MHz Channel Bandwidth Carriers, ACPR and IM3 measured in 3.84 MHz Bandwidth. Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.

Common–Source Amplifier Power Gain (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 38 W Avg., I <sub>DQ</sub> = 2 x 800 mA, f <sub>1</sub> = 1932.5 MHz, f <sub>2</sub> = 1942.5 MHz and f <sub>1</sub> = 1977.5 MHz, f <sub>2</sub> = 1987.5 MHz)	G <sub>ps</sub>	12.5	14	—	dB
Drain Efficiency (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 38 W Avg., I <sub>DQ</sub> = 2 x 800 mA, f <sub>1</sub> = 1932.5 MHz, f <sub>2</sub> = 1942.5 MHz and f <sub>1</sub> = 1977.5 MHz, f <sub>2</sub> = 1987.5 MHz)	η	23	26	—	%
Third Order Intermodulation Distortion (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 38 W Avg., I <sub>DQ</sub> = 2 x 800 mA, f <sub>1</sub> = 1932.5 MHz, f <sub>2</sub> = 1942.5 MHz and f <sub>1</sub> = 1977.5 MHz, f <sub>2</sub> = 1987.5 MHz; IM3 measured over 3.84 MHz BW @ f <sub>1</sub> –10 MHz and f <sub>2</sub> +10 MHz referenced to carrier channel power.)	IM3	—	–37.5	–35	dBc
Adjacent Channel Power Ratio (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 38 W Avg., I <sub>DQ</sub> = 2 x 800 mA, f <sub>1</sub> = 1932.5 MHz, f <sub>2</sub> = 1942.5 MHz and f <sub>1</sub> = 1977.5 MHz, f <sub>2</sub> = 1987.5 MHz; ACPR measured over 3.84 MHz BW @ f <sub>1</sub> –5 MHz and f <sub>2</sub> +5 MHz.)	ACPR	—	–41	–38	dBc
Input Return Loss (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 38 W Avg., I <sub>DQ</sub> = 2 x 800 mA, f <sub>1</sub> = 1932.5 MHz, f <sub>2</sub> = 1942.5 MHz and f <sub>1</sub> = 1977.5 MHz, f <sub>2</sub> = 1987.5 MHz)	IRL	—	–16	–9	dB

(1) Each side of device measured separately. Part is internally matched both on input and output.

(2) Measurements made with device in push–pull configuration.

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Z1	0.081" x 1.126" Microstrip	Z11, Z12	0.341" x 0.945" Microstrip
Z2	0.079" x 0.138" Microstrip	Z13, Z14	0.035" x 0.913" Microstrip
Z3	0.081" x 0.091" Microstrip	Z15, Z16	0.581" x 0.823" Microstrip
Z4	0.081" x 0.117" Microstrip	Z17, Z18	0.059" x 1.057" Microstrip
Z5, Z24	0.134" x 0.874" Microstrip	Z19, Z20	0.081" x 0.046" Microstrip
Z6, Z23	0.081" x 2.269" Microstrip	Z21, Z22	0.081" x 0.126" Microstrip
Z7, Z8	0.081" x 0.118" Microstrip	Z25	0.081" x 0.793" Microstrip
Z9, Z10	0.081" x 0.079" Microstrip	PCB	Taconic TLX8-0300, 0.030", $\epsilon_r = 2.55$

**Figure 1. MRF5P20180 Test Circuit Schematic**

**Table 1. MRF5P20180 Test Circuit Component Designations and Values**

Part	Description	Value, P/N or DWG	Manufacturer
C1	1.8 pF 100B Chip Capacitor	100B1R8BW	ATC
C2, C3, C4, C5, C6, C7	10 pF 100B Chip Capacitors	100B100GW	ATC
C8, C9	6.8 pF 100B Chip Capacitors	100B6R8CW	ATC
C10, C11, C12, C13	10 nF 200B Chip Capacitors	200B103MW	ATC
C14, C15, C16, C17, C18, C19	22 $\mu$ F, 35 V Tantalum Capacitors	TAJE226M035	AVX
C20, C21	220 $\mu$ F, 63 V Electrolytic Capacitors	13668221	Philips
R1, R2, R3, R4	10 k $\Omega$ Chip Resistors (1206)		

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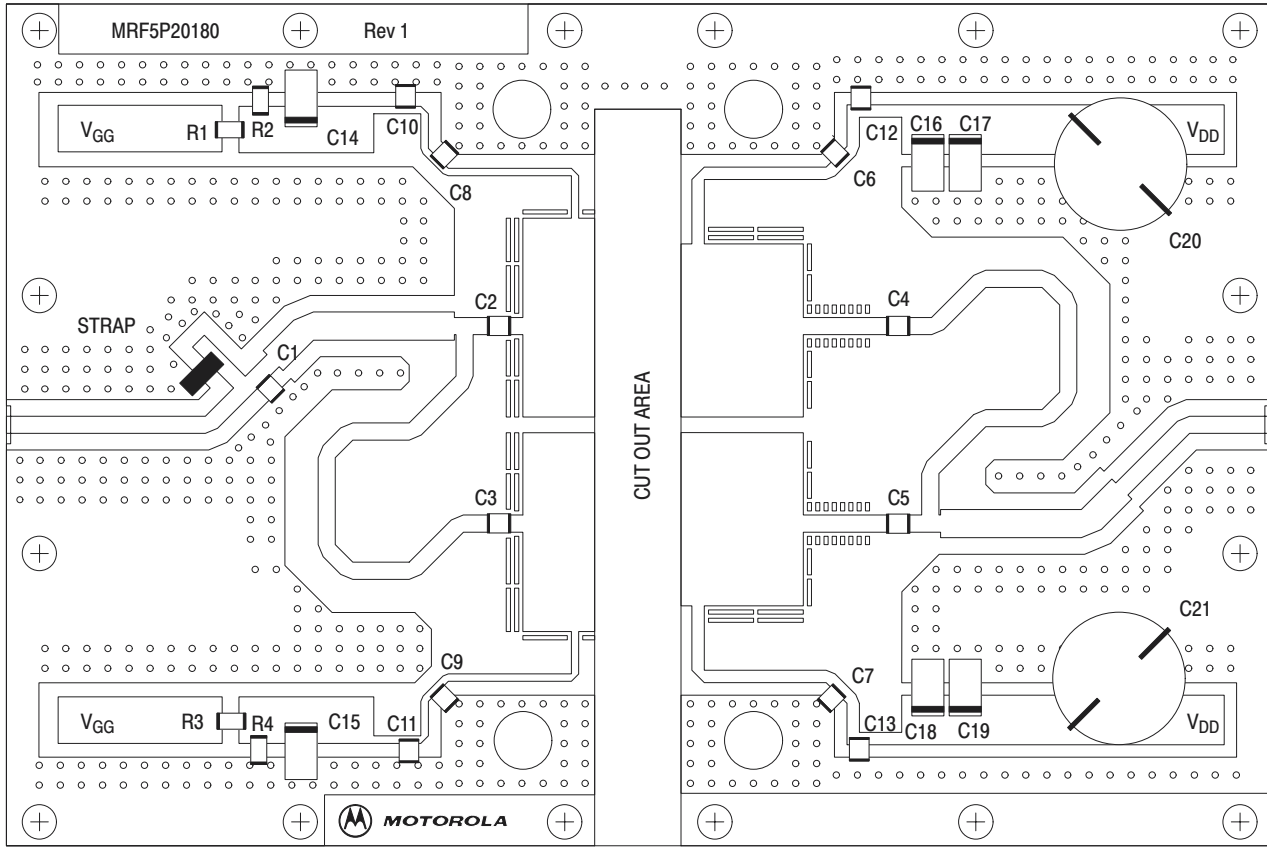


Figure 2. MRF5P20180 Test Circuit Component Layout

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## TYPICAL CHARACTERISTICS

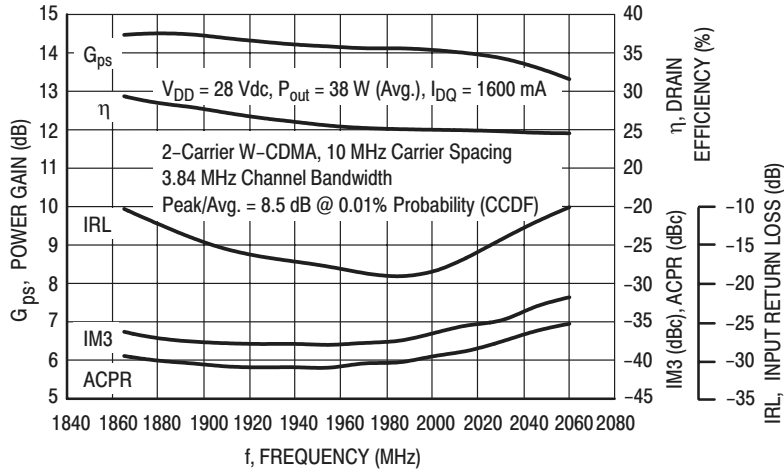


Figure 3. 2-Carrier W-CDMA Broadband Performance

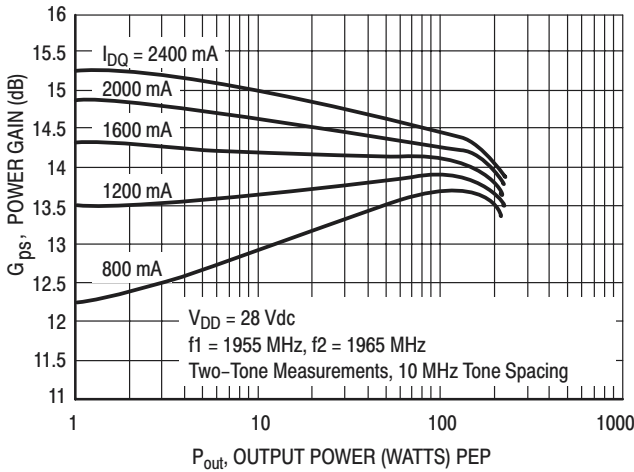


Figure 4. Two-Tone Power Gain versus Output Power

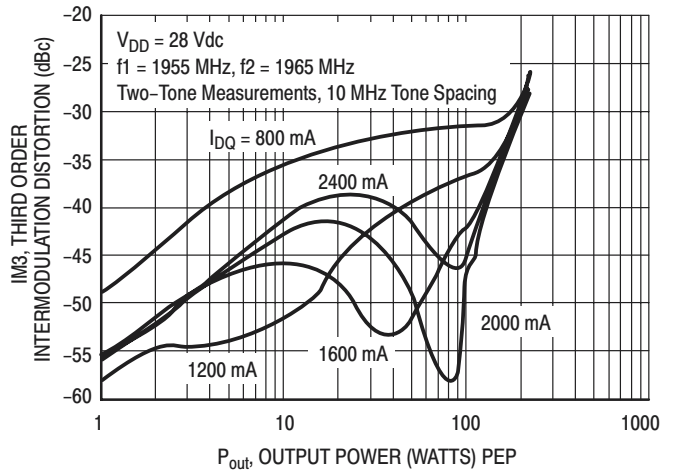


Figure 5. Third Order Intermodulation Distortion versus Output Power

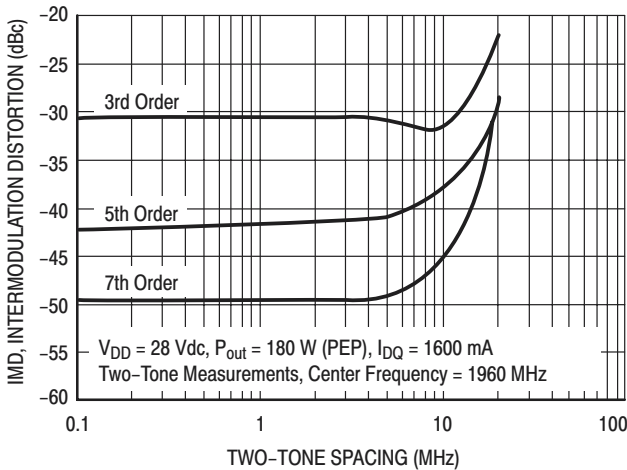


Figure 6. Intermodulation Distortion Products versus Tone Spacing

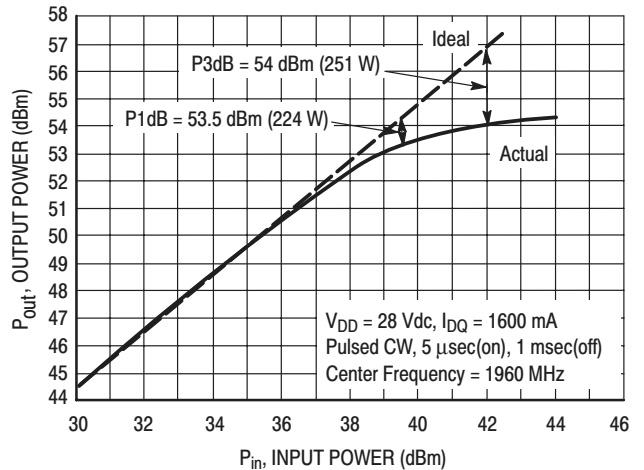
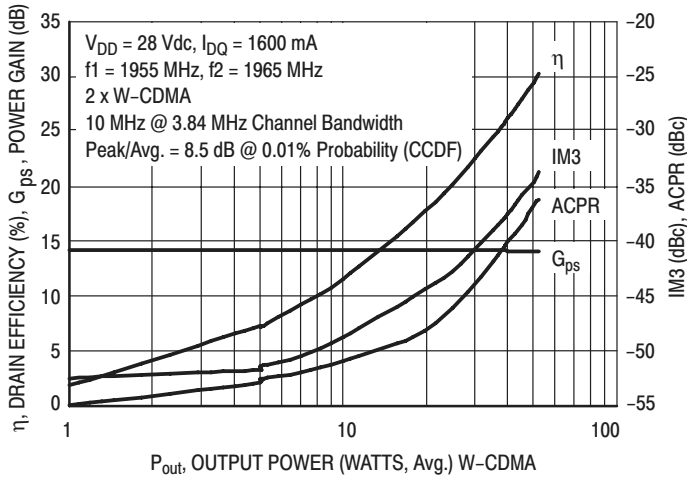


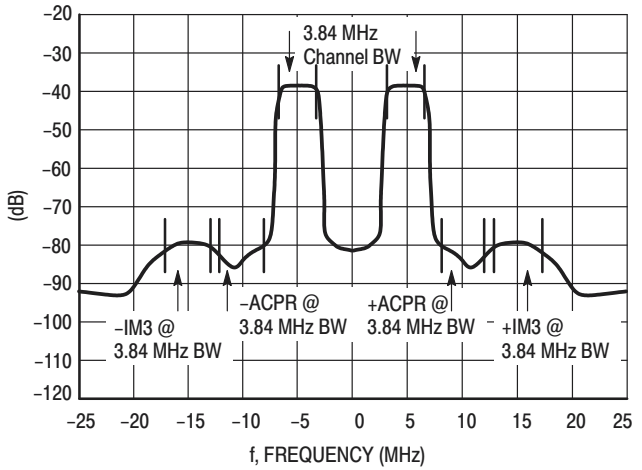
Figure 7. Pulse CW Output Power versus Input Power

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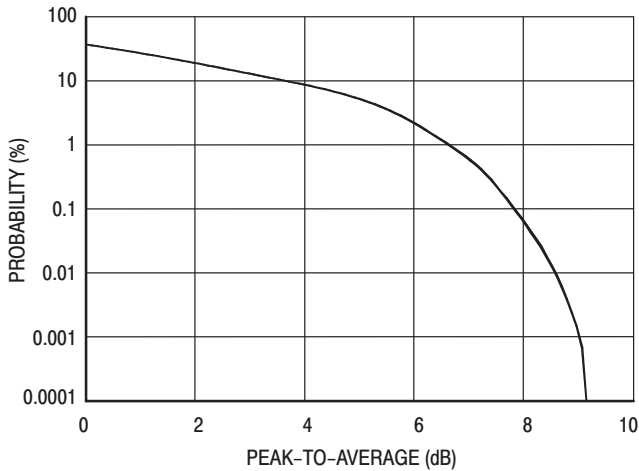
## TYPICAL CHARACTERISTICS



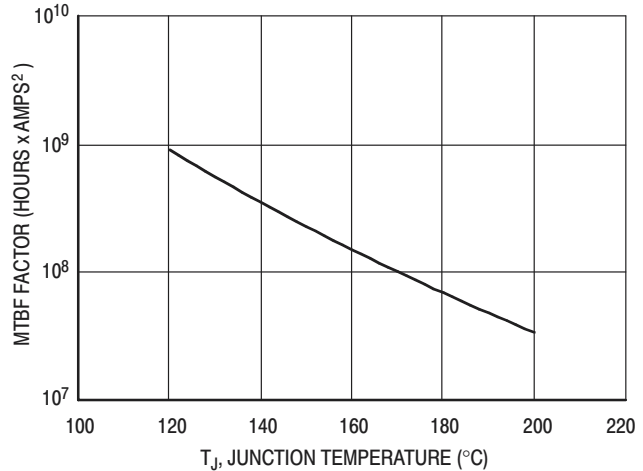
**Figure 8. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power**



**Figure 9. 2-Carrier W-CDMA Spectrum**



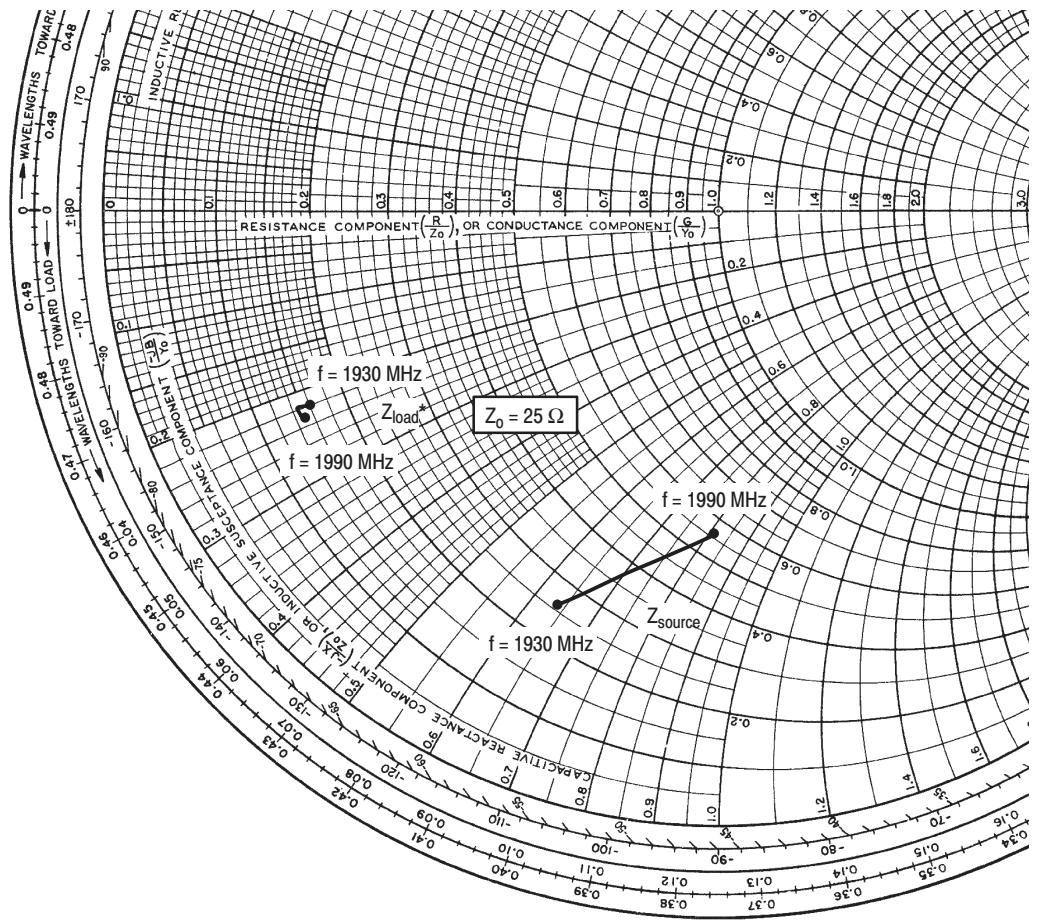
**Figure 10. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 67% Clipping, Single Carrier Test Signal**



This above graph displays calculated MTBF in hours x ampere<sup>2</sup> drain current. Life tests at elevated temperatures have correlated to better than  $\pm 10\%$  of the theoretical prediction for metal failure. Divide MTBF factor by  $I_D^2$  for MTBF in a particular application.

**Figure 11. MTBF Factor versus Junction Temperature**

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$V_{DD} = 28 \text{ V}$ ,  $I_{DQ} = 2 \times 800 \text{ mA}$ ,  $P_{out} = 38 \text{ W Avg.}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
1930	$6.54 - j16.04$	$4.06 - j5.56$
1960	$9.70 - j17.92$	$3.70 - j5.48$
1990	$13.88 - j20.46$	$3.64 - j5.76$

$Z_{source}$  = Test circuit impedance as measured from gate to gate, balanced configuration.

$Z_{load}$  = Test circuit impedance as measured from drain to drain, balanced configuration.

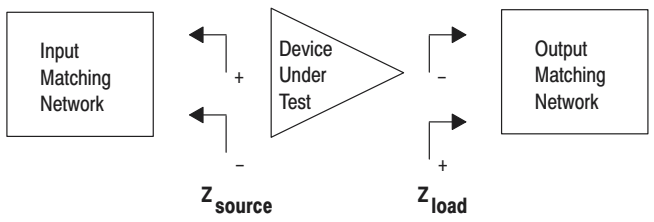
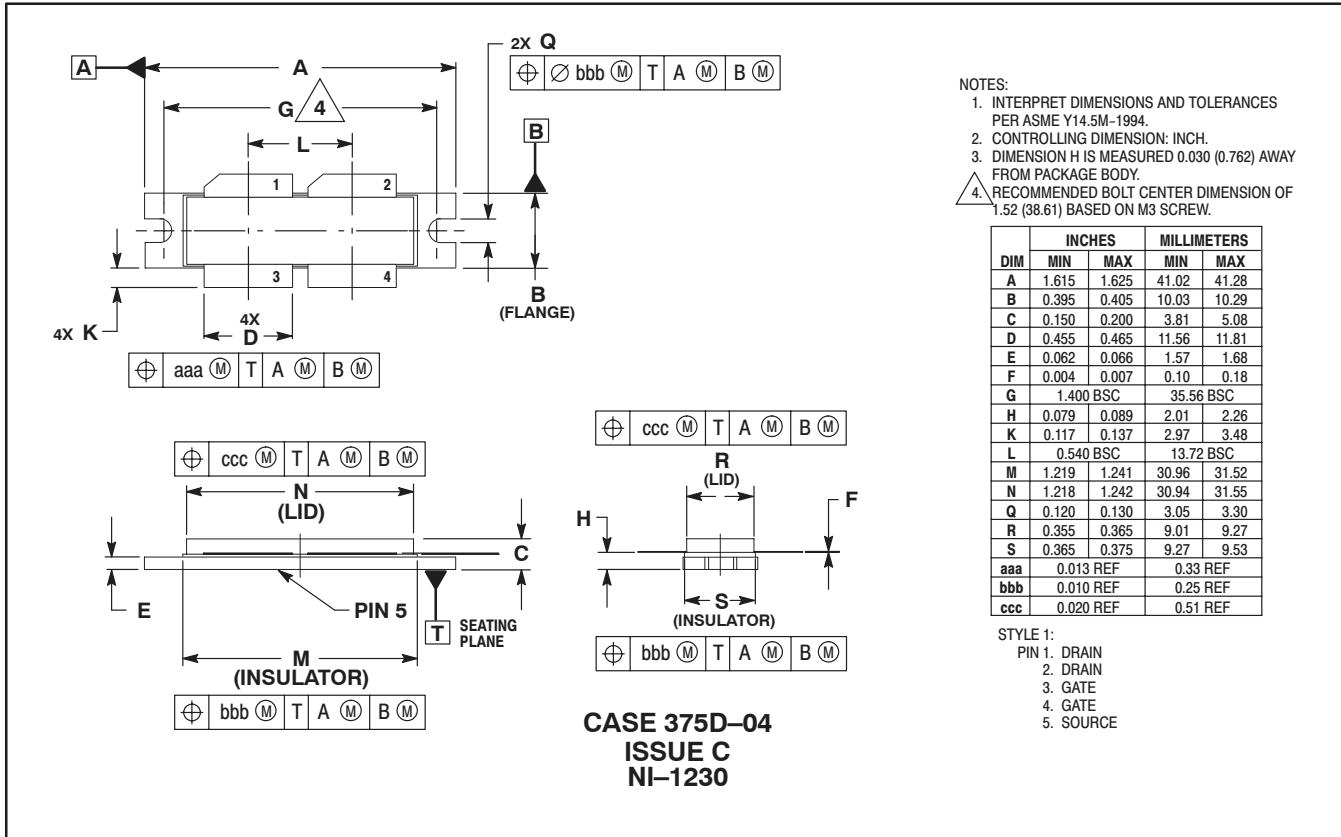


Figure 12. Series Equivalent Input and Output Impedance

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## PACKAGE DIMENSIONS



- NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
  4. RECOMMENDED BOLT CENTER DIMENSION OF 1.52 (38.61) BASED ON M3 SCREW.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.615	1.625	41.02	41.28
B	0.395	0.405	10.03	10.29
C	0.150	0.200	3.81	5.08
D	0.455	0.465	11.56	11.81
E	0.062	0.066	1.57	1.68
F	0.004	0.007	0.10	0.18
G	1.400	BSC	35.56	BSC
H	0.079	0.089	2.01	2.26
K	0.117	0.137	2.97	3.48
L	0.540	BSC	13.72	BSC
M	1.219	1.241	30.96	31.52
N	1.218	1.242	30.94	31.55
Q	0.120	0.130	3.05	3.30
R	0.355	0.365	9.01	9.27
S	0.365	0.375	9.27	9.53
aaa	0.013	REF	0.33	REF
bbb	0.010	REF	0.25	REF
ccc	0.020	REF	0.51	REF

- STYLE 1:
- PIN 1. DRAIN
  2. DRAIN
  3. GATE
  4. GATE
  5. SOURCE

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