

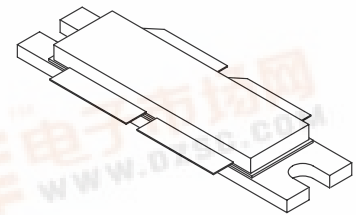
The RF Sub-Micron MOSFET Line  
**RF Power Field Effect Transistor**  
**N-Channel Enhancement-Mode Lateral MOSFET**

**MRF5P21240R6**

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

- Typical 2-carrier W-CDMA Performance for  $V_{DD} = 28$  Volts,  $I_{DQ} = 2 \times 1100$  mA,  $f_1 = 2135$  MHz,  $f_2 = 2145$  MHz, Channel Bandwidth = 3.84 MHz, Adjacent Channels Measured over 3.84 MHz BW @  $f_1 - 5$  MHz and  $f_2 + 5$  MHz. Distortion Products Measured over a 3.84 MHz BW @  $f_1 - 10$  MHz and  $f_2 + 10$  MHz, Each Carrier Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.
  - Output Power — 52 Watts Avg.
  - Power Gain — 13 dB
  - Efficiency — 24%
  - IM3 — -36 dBc
  - ACPR — -39 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 28 Vdc,  $f = 2140$  MHz, 180 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R6 Suffix = 150 Units per 56 mm, 13 inch Reel.

**2170 MHz, 52 W AVG.,  
 2 x W-CDMA, 28 V  
 LATERAL N-CHANNEL  
 RF POWER MOSFET**



**CASE 375D-04, STYLE 1  
 NI-1230**

**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	65	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	500 2.86	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	$T_J$	200	$^\circ\text{C}$
CW Operation	CW	180	Watts

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Case Temperature $55^\circ\text{C}$ , 180 W CW Case Temperature $45^\circ\text{C}$ , 52 W CW	$R_{\theta JC}$	0.35 0.40	$^\circ\text{C}/\text{W}$

**NOTE – CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

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## ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)
Charge Device Model	C6 (Minimum)

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS (1)

Zero Gate Voltage Drain Leakage Current (V <sub>DS</sub> = 65 Vdc, V <sub>GS</sub> = 0 Vdc)	I <sub>DSS</sub>	—	—	10	μA <sub>dc</sub>
Zero Gate Voltage Drain Leakage Current (V <sub>DS</sub> = 28 Vdc, V <sub>GS</sub> = 0 Vdc)	I <sub>DSS</sub>	—	—	1	μA <sub>dc</sub>
Gate–Source Leakage Current (V <sub>GS</sub> = 5 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	—	—	1	μA <sub>dc</sub>

### ON CHARACTERISTICS (1)

Gate Threshold Voltage (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 300 μA <sub>dc</sub> )	V <sub>GS(th)</sub>	2	2.8	4	Vdc
Gate Quiescent Voltage (V <sub>DS</sub> = 28 Vdc, I <sub>D</sub> = 1100 mA <sub>dc</sub> )	V <sub>GS(Q)</sub>	3	3.8	5	Vdc
Drain–Source On–Voltage (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 3 Adc)	V <sub>DS(on)</sub>	—	0.26	0.3	Vdc
Forward Transconductance (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 3 Adc)	g <sub>fs</sub>	—	7.5	—	S

### DYNAMIC CHARACTERISTICS (1)

Reverse Transfer Capacitance (V <sub>DS</sub> = 28 Vdc, V <sub>GS</sub> = 0, f = 1 MHz)	C <sub>rss</sub>	—	2.75	—	pF
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### FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2)

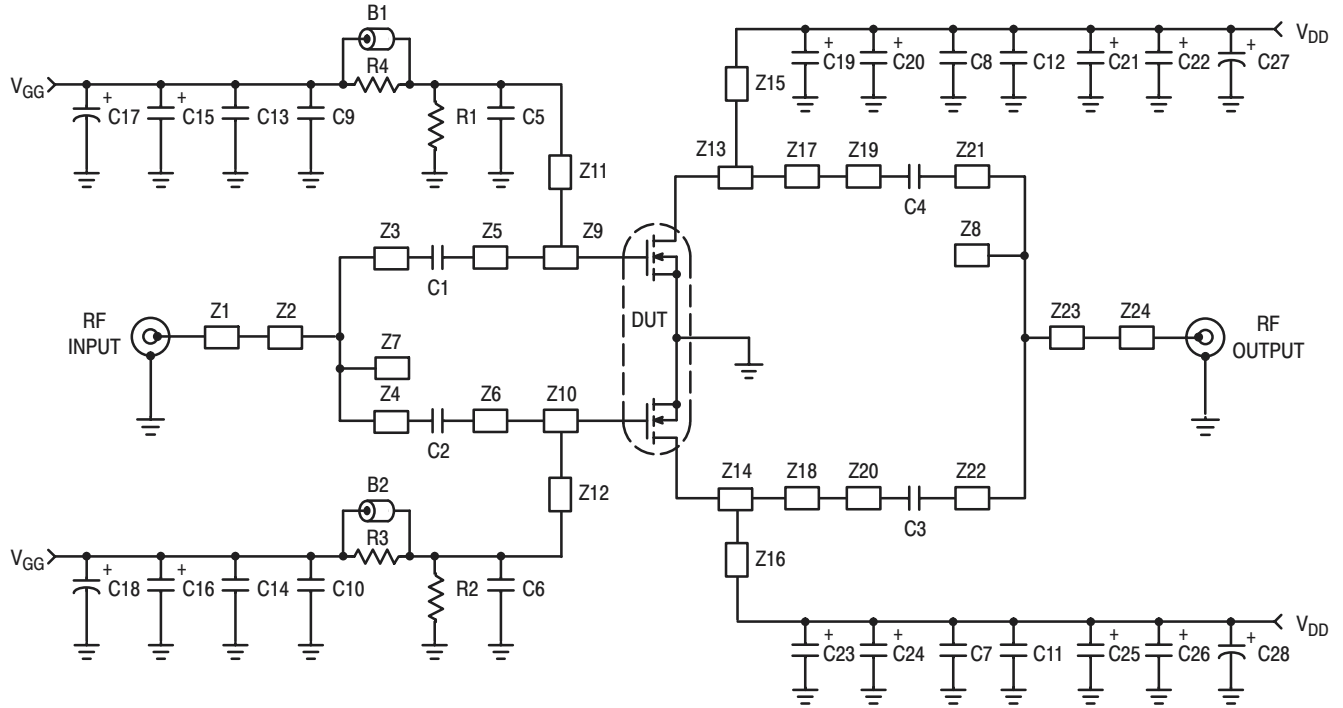
2–Carrier W–CDMA, 3.84 MHz Channel Bandwidth Carriers. Each carrier has Peak/Avg. ratio = 8.5 dB @ 0.01% Probability on CCDF.

Common–Source Amplifier Power Gain (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 52 W Avg., I <sub>DQ</sub> = 2 x 1100 mA, f <sub>1</sub> = 2112.5 MHz, f <sub>2</sub> = 2122.5 MHz and f <sub>1</sub> = 2157.5 MHz, f <sub>2</sub> = 2167.5 MHz)	G <sub>ps</sub>	12	13	—	dB
Drain Efficiency (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 52 W Avg., I <sub>DQ</sub> = 2 x 1100 mA, f <sub>1</sub> = 2112.5 MHz, f <sub>2</sub> = 2122.5 MHz and f <sub>1</sub> = 2157.5 MHz, f <sub>2</sub> = 2167.5 MHz)	η	22.5	24	—	%
Third Order Intermodulation Distortion (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 52 W Avg., I <sub>DQ</sub> = 2 x 1100 mA, f <sub>1</sub> = 2112.5 MHz, f <sub>2</sub> = 2122.5 MHz and f <sub>1</sub> = 2157.5 MHz, f <sub>2</sub> = 2167.5 MHz; IM3 measured over 3.84 MHz BW @ f <sub>1</sub> –10 MHz and f <sub>2</sub> +10 MHz)	IM3	—	–36	–34	dBc
Adjacent Channel Power Ratio (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 52 W Avg., I <sub>DQ</sub> = 2 x 1100 mA, f <sub>1</sub> = 2112.5 MHz, f <sub>2</sub> = 2122.5 MHz and f <sub>1</sub> = 2157.5 MHz, f <sub>2</sub> = 2167.5 MHz; ACPR measured over 3.84 MHz BW @ f <sub>1</sub> – 5 MHz and f <sub>2</sub> +5 MHz.)	ACPR	—	–39	–37	dBc
Input Return Loss (V <sub>DD</sub> = 28 Vdc, P <sub>out</sub> = 52 W Avg., I <sub>DQ</sub> = 2 x 1100 mA, f <sub>1</sub> = 2112.5 MHz, f <sub>2</sub> = 2122.5 MHz and f <sub>1</sub> = 2157.5 MHz, f <sub>2</sub> = 2167.5 MHz)	IRL	—	–12	–9	dB

(1) Each side of device measured separately. Part is internally matched both on input and output.

(2) Measurements made with device in push–pull configuration.

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Z1	0.898" x 0.080" Microstrip	Z11, Z12	1.270" x 0.058" Microstrip
Z2, Z23	0.775" x 0.136" Microstrip	Z13, Z14	0.250" x 0.500" Microstrip
Z3, Z22	0.060" x 0.080" Microstrip	Z15, Z16	0.850" x 0.150" Microstrip
Z4, Z21	1.867" x 0.080" Microstrip	Z17, Z18	0.535" x 0.390" Microstrip
Z5, Z6	0.443" x 0.080" Microstrip	Z19, Z20	0.218" x 0.080" Microstrip
Z7, Z8	0.100" x 0.080" Microstrip	Z24	0.825" x 0.080" Microstrip
Z9, Z10	0.490" x 0.540" Microstrip	PCB	Arlon GX-0300-55-22, 0.030", $\epsilon_r = 2.55$

**Figure 1. MRF5P21240R6 Test Circuit Schematic**

**Table 1. MRF5P21240R6 Test Circuit Component Designations and Values**

Part	Description	Value, P/N or DWG	Manufacturer
B1, B2	Short Ferrite Beads	2743019447	Fair Rite
C1, C2, C3, C4	18 pF Chip Capacitors	100B180JCA500X	ATC
C5, C6, C7, C8	6.8 pF Chip Capacitors	100B6R8JCA500X	ATC
C9, C10, C11, C12	0.1 $\mu$ F Chip Capacitors	CDR33BX104AKWS	Kemet
C13, C14	1000 pF Chip Capacitors	100B102JCA500X	ATC
C15, C16	4.7 $\mu$ F Tantalum Capacitors	T491C475M050	Kemet
C17, C18	10 $\mu$ F Electrolytic Capacitors	EEV-HB1H100P	Panasonic
C19, C20, C21, C22 C23, C24, C25, C26	22 $\mu$ F Tantalum Capacitors	T491X226K035AS4394	Kemet
C27, C28	100 $\mu$ F Electrolytic Capacitors	517D107M050BB6A	Sprague
R1, R2	1.0 k $\Omega$ , 1/8 W Chip Resistors		
R3, R4	10 $\Omega$ , 1/8 W Chip Resistors		

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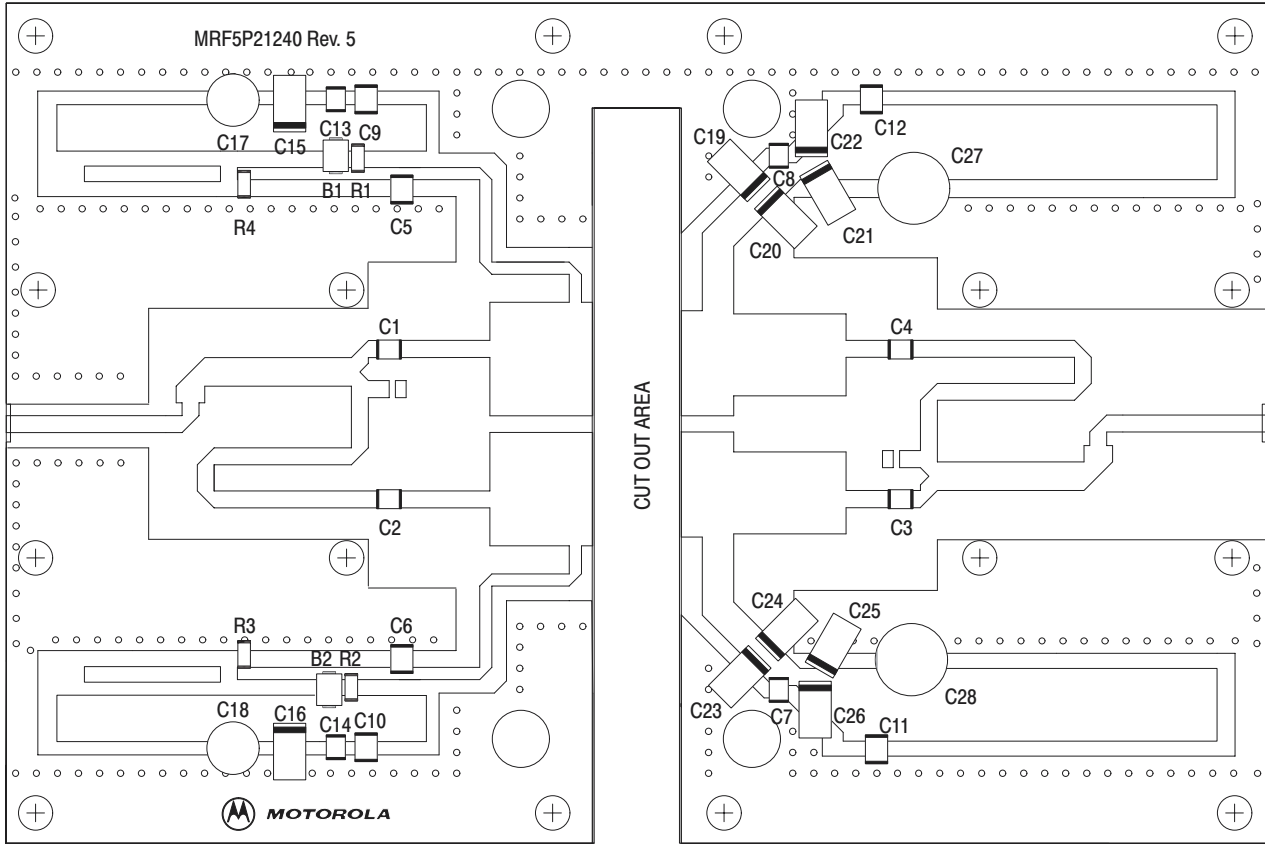


Figure 2. MRF5P21240R6 Test Circuit Component Layout

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## TYPICAL CHARACTERISTICS

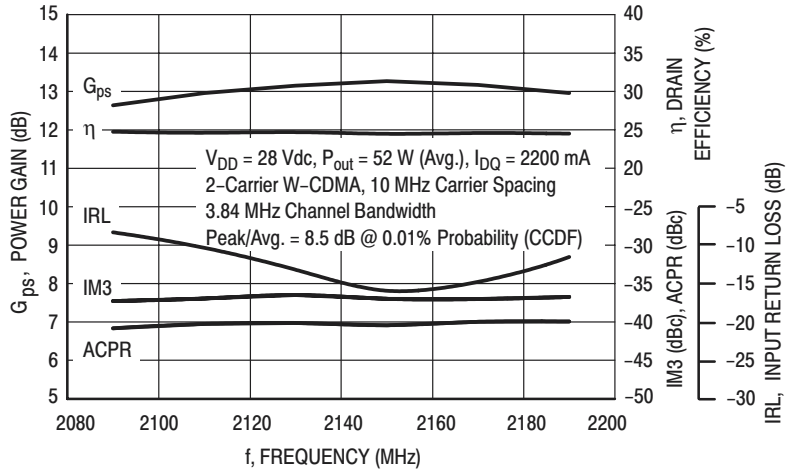


Figure 3. 2-Carrier W-CDMA Broadband Performance

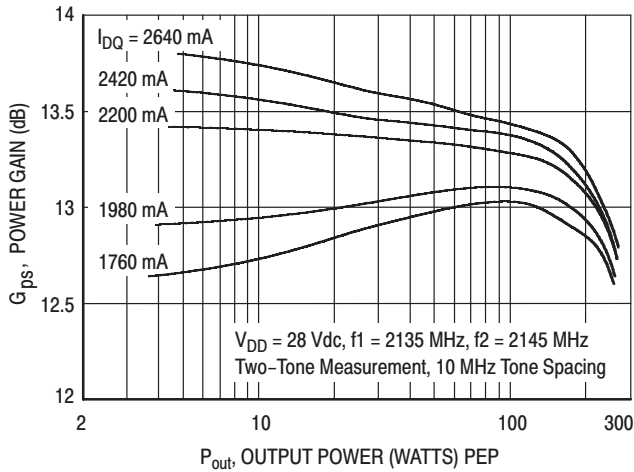


Figure 4. Two-Tone Power Gain versus Output Power

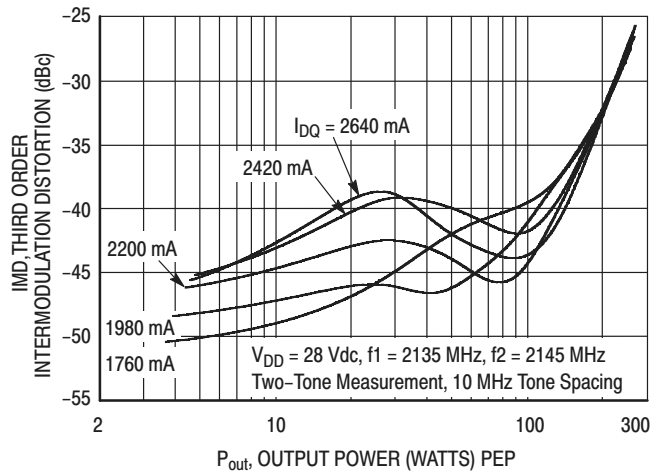


Figure 5. Third Order Intermodulation Distortion versus Output Power

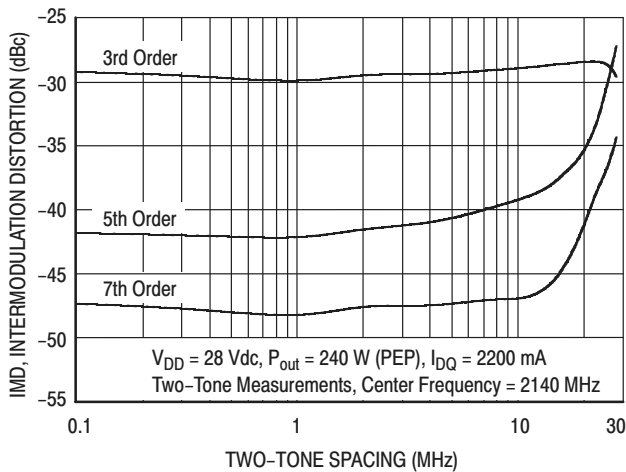


Figure 6. Intermodulation Distortion Products versus Tone Spacing

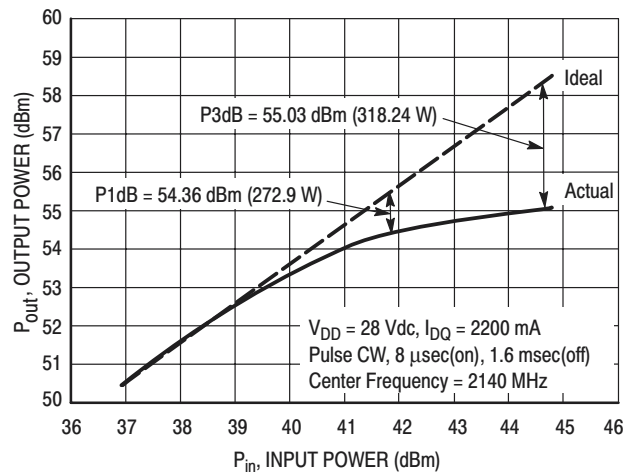
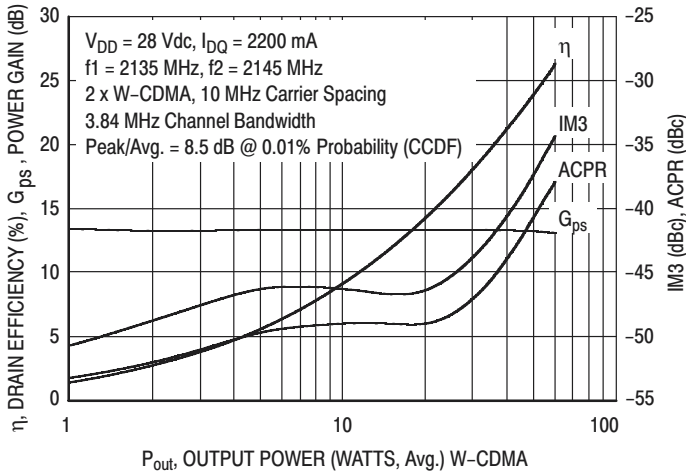


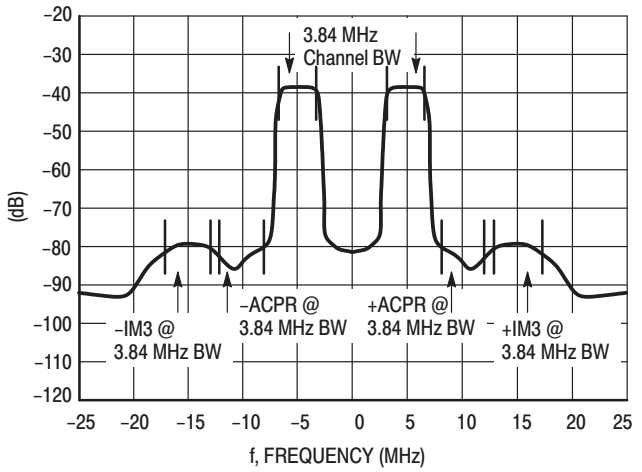
Figure 7. Pulse CW Output Power versus Input Power

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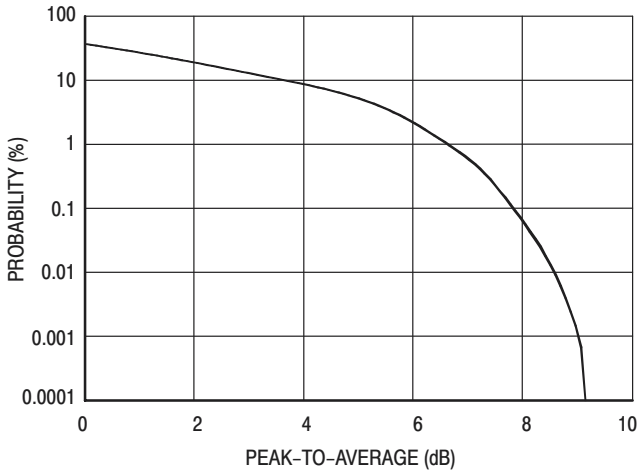
## TYPICAL CHARACTERISTICS



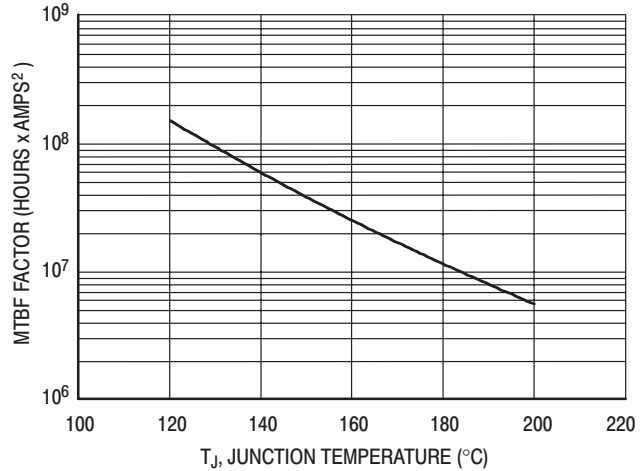
**Figure 8. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power**



**Figure 9. 2-Carrier W-CDMA Spectrum**



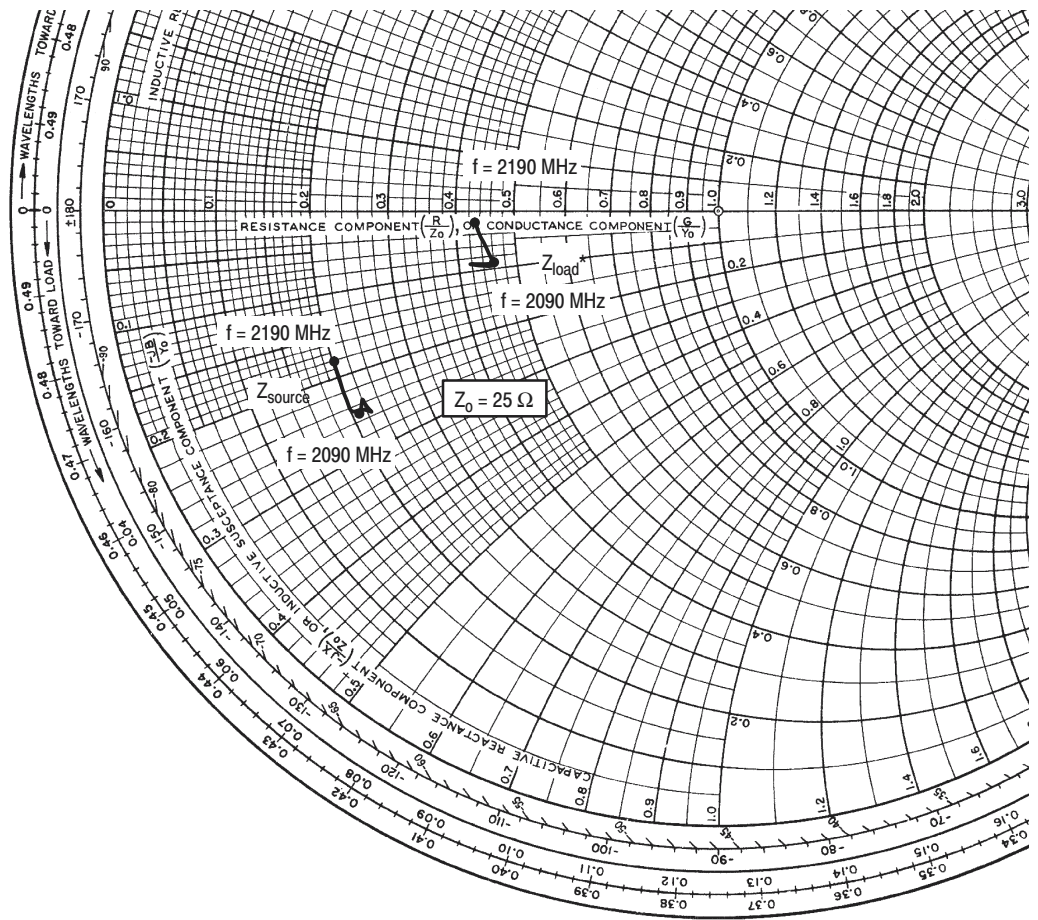
**Figure 10. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 67% Clipping, Single Carrier Test Signal**



This above graph displays calculated MTBF in hours x ampere<sup>2</sup> drain current. Life tests at elevated temperatures have correlated to better than  $\pm 10\%$  of the theoretical prediction for metal failure. Divide MTBF factor by  $I_D^2$  for MTBF in a particular application.

**Figure 11. MTBF Factor versus Junction Temperature**

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$V_{DD} = 28\text{ V}$ ,  $I_{DQ} = 2 \times 1100\text{ mA}$ ,  $P_{out} = 52\text{ W Avg.}$

f MHz	Z <sub>source</sub> Ω	Z <sub>load</sub> Ω
2090	5.33 – j6.21	11.42 – j2.25
2110	5.44 – j5.88	10.45 – j2.16
2130	5.40 – j6.16	11.28 – j2.14
2150	5.12 – j6.06	11.38 – j2.14
2170	4.96 – j5.25	11.04 – j1.25
2190	4.98 – j4.47	10.73 – j0.40

Z<sub>source</sub> = Test circuit impedance as measured from gate to gate, balanced configuration.

Z<sub>load</sub> = Test circuit impedance as measured from drain to drain, balanced configuration.

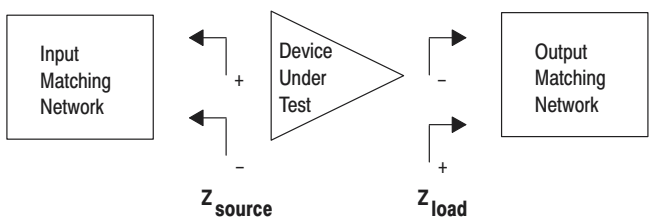
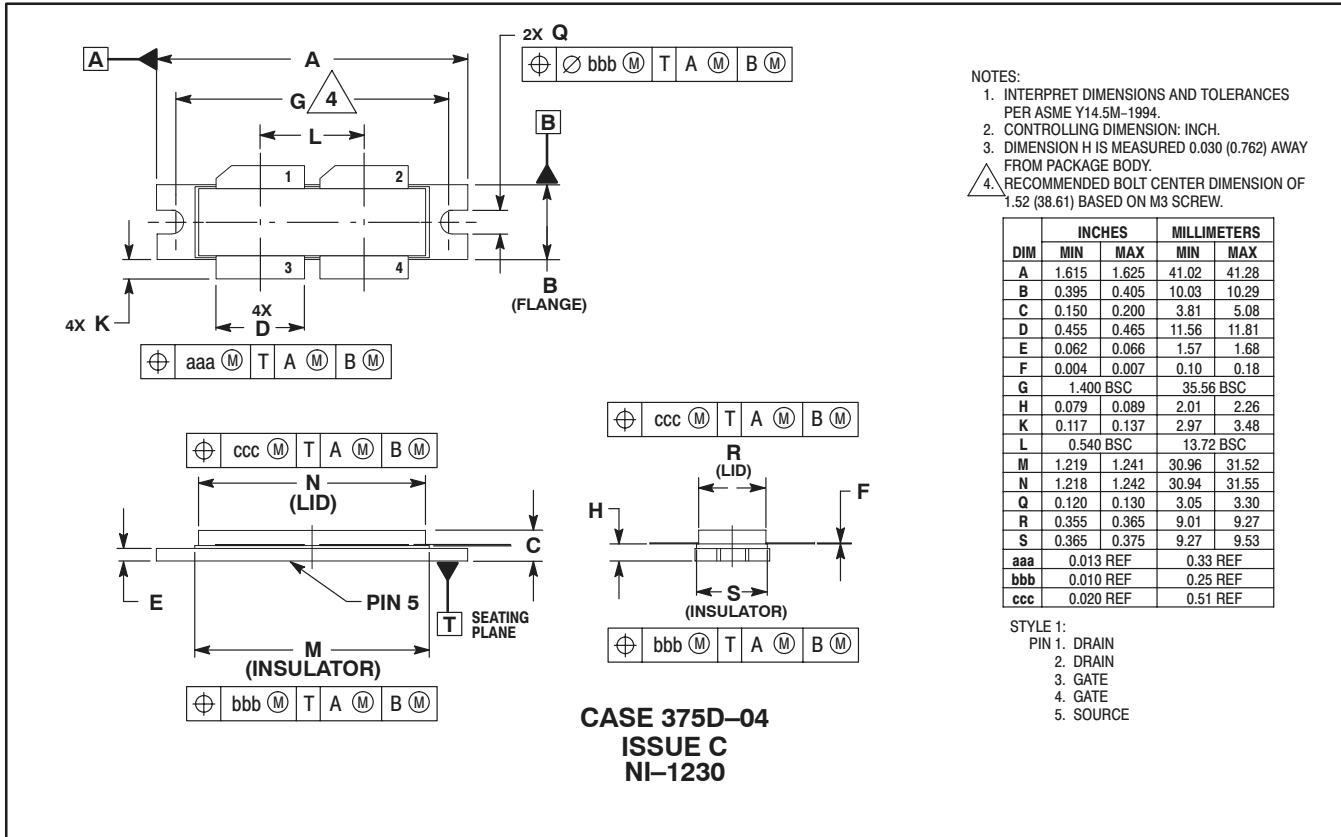


Figure 12. Series Equivalent Source and Load Impedance

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## PACKAGE DIMENSIONS



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