intersil

HUF76143P3, HUF76143S3S

75A, 30V, 0.0055 Ohm, N-Channel, Logic Level UltraFET Power MOSFETs

These N-Channel power MOSFETs are manufactured using the innovative UltraFET™ process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA76143.

Ordering Information

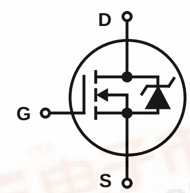
PART NUMBER	PACKAGE	BRAND
HUF76143P3	TO-220AB	76143P
HUF76143S3S	TO-263AB	76143S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF76143S3ST.

Features

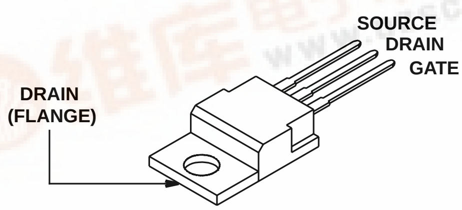
- Logic Level Gate Drive
- 75A, 30V
- Ultra Low On-Resistance, $r_{DS(ON)} = 0.0055\Omega$
- Temperature Compensating PSPICE® Model
- Temperature Compensating SABER© Mode
- Thermal Impedance SPICE Model
- Thermal Impedance SABER Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

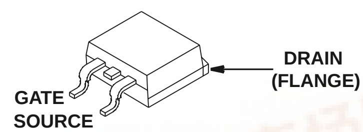


Packaging

JEDEC TO-220AB



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	30	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	30	V
Gate to Source Voltage	V_{GS}	±16	V
Drain Current			
Continuous ($T_C = 25^oC$, V_{GS} = 10V) (Figure 2)	I_D	75	A
Continuous ($T_C = 100^oC$, V_{GS} = 5V)	I_D	75	A
Continuous ($T_C = 100^oC$, V_{GS} = 4.5V) (Figure 2)	I_D	75	A
Pulsed Drain Current	I_{DM}	Figure 4	
Pulsed Avalanche Rating	E_{AS}	Figures 6, 17, 18	
Power Dissipation	P_D	225	W
Derate Above 25^oC		1.8	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-40 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS						
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 12)	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 25V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 25V, V_{GS} = 0V, $T_C = 150^oC$	-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±16V	-	-	±100	nA
ON STATE SPECIFICATIONS						
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA (Figure 11)	1	-	3	V
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 75A, V_{GS} = 10V (Figures 9, 10)	-	0.0052	0.0055	Ω
		I_D = 75A, V_{GS} = 5V (Figure 9)	-	0.0063	0.0075	Ω
		I_D = 75A, V_{GS} = 4.5V (Figure 9)	-	0.0068	0.0085	Ω
THERMAL SPECIFICATIONS						
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)	-	-	0.55	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220 and TO-263	-	-	62	$^oC/W$
SWITCHING SPECIFICATIONS (V_{GS} = 4.5V)						
Turn-On Time	t_{ON}	V_{DD} = 15V, $I_D \cong$ 75A, R_L = 0.2Ω, V_{GS} = 4.5V, R_{GS} = 2.5Ω (Figures 15, 21, 22)	-	-	250	ns
Turn-On Delay Time	$t_{d(ON)}$		-	22	-	ns
Rise Time	t_r		-	145	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	30	-	ns
Fall Time	t_f		-	18	-	ns
Turn-Off Time	t_{OFF}		-	-	72	ns

Electrical Specifications
$T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
SWITCHING SPECIFICATIONS (V_{GS} = 10V)							
Turn-On Time	t_{ON}	V_{DD} = 15V, $I_D \cong$ 75A, R_L = 0.2Ω, V_{GS} = 10V, R_{GS} = 2.5Ω (Figures 16, 21, 20)		-	-	105	ns
Turn-On Delay Time	$t_{d(ON)}$			-	14	-	ns
Rise Time	t_r			-	55	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	40	-	ns
Fall Time	t_f			-	18	-	ns
Turn-Off Time	t_{OFF}			-	-	87	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 15V, $I_D \cong$ 75A, R_L = 0.2Ω, $I_{g(REF)}$ = 1.0mA (Figures 14, 19, 20)	-	95	114	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0V to 5V		-	50	60	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 1V		-	3.8	4.6	nC
Gate to Source Gate Charge	Q_{gs}			-	11.70	-	nC
Gate to Drain “Miller” Charge	Q_{gd}			-	22.00	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 13)		-	3900	-	pF
Output Capacitance	C_{OSS}			-	1600	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	270	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 75A	-	-	1.25	V
Reverse Recovery Time	t_{rr}	I_{SD} = 75A, dI_{SD}/dt = 100A/μs	-	-	90	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 75A, dI_{SD}/dt = 100A/μs	-	-	170	nC

Typical Performance Curves

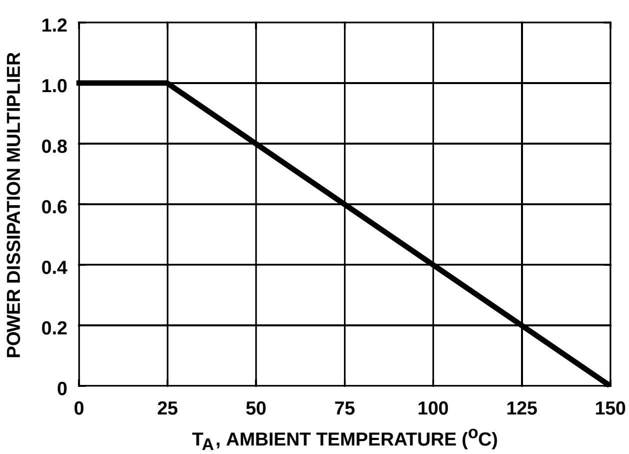


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

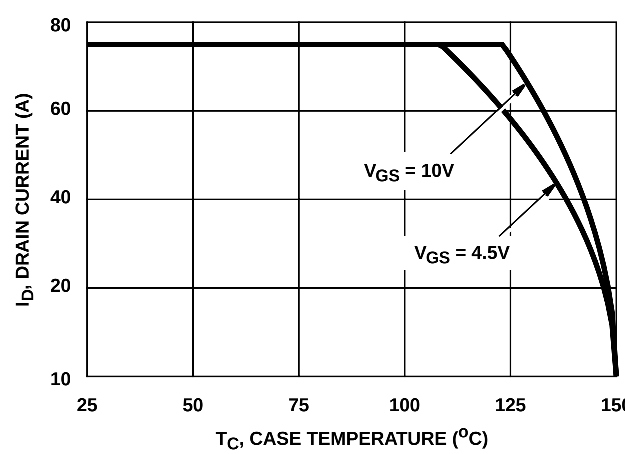


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

Typical Performance Curves (Continued)

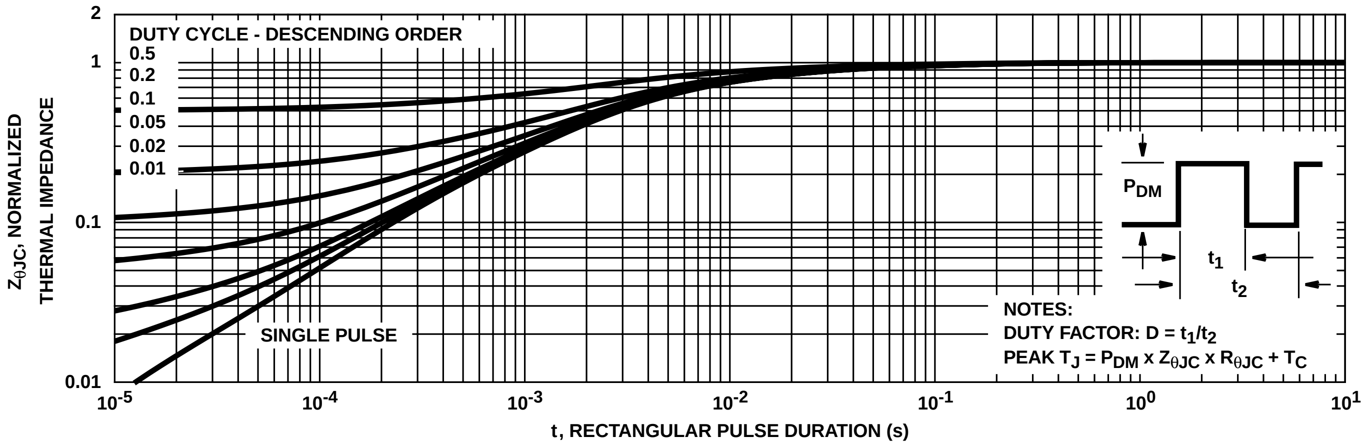


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

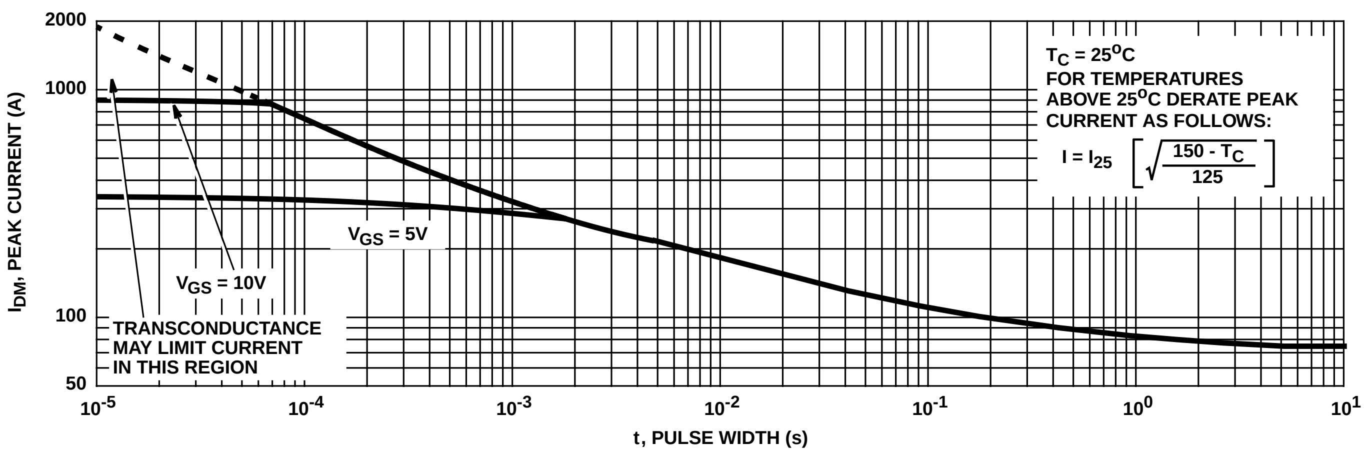


FIGURE 4. PEAK CURRENT CAPABILITY

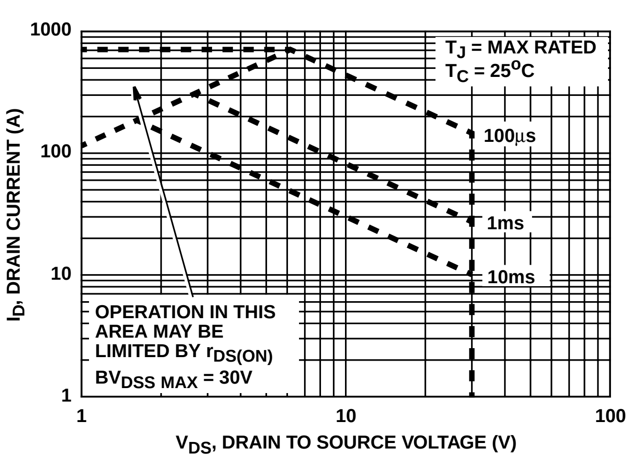
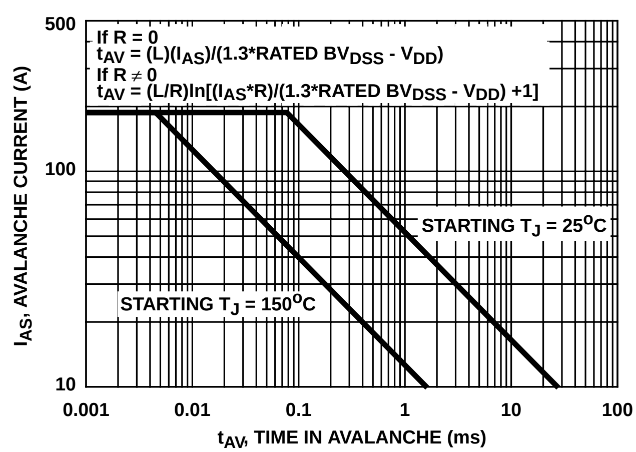


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

Typical Performance Curves **(Continued)**

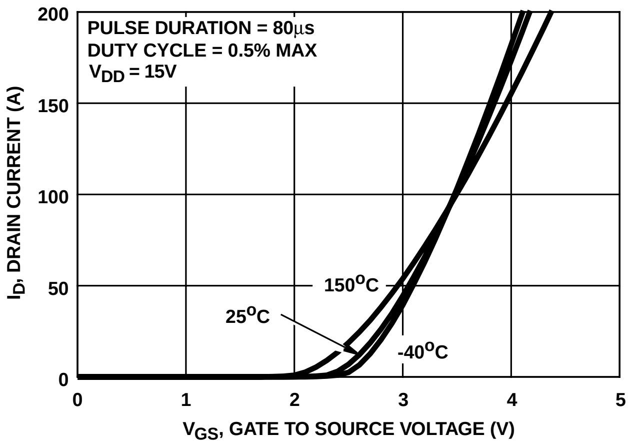


FIGURE 7. TRANSFER CHARACTERISTICS

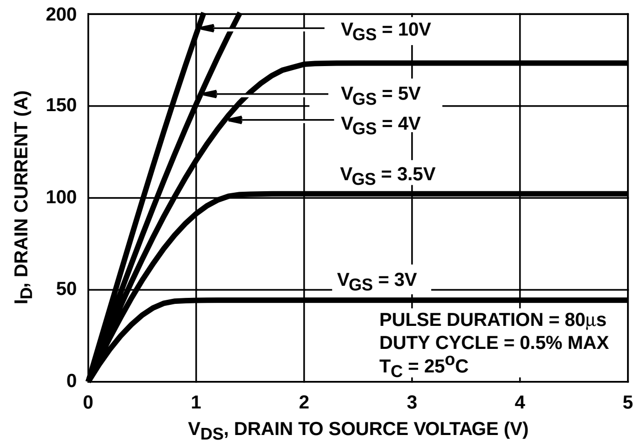


FIGURE 8. SATURATION CHARACTERISTICS

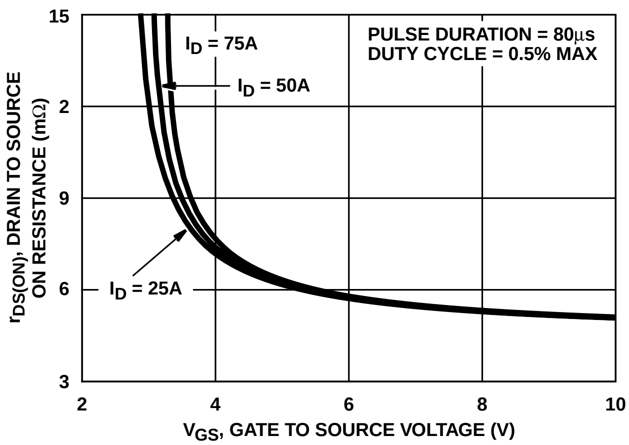


FIGURE 9. SOURCE TO DRAIN ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

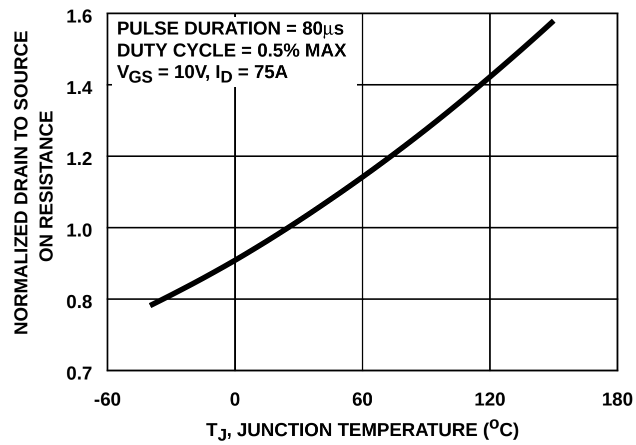


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

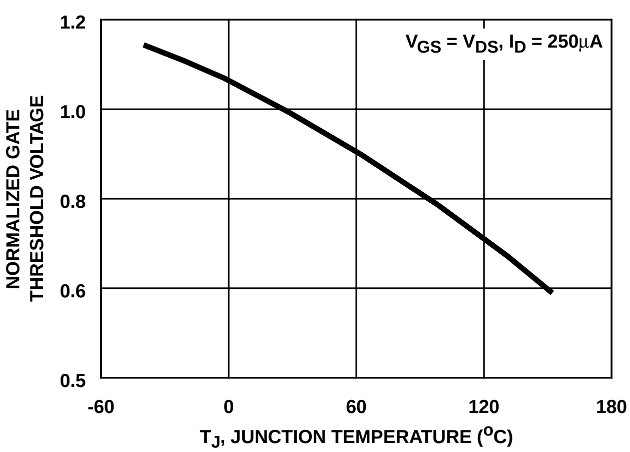


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

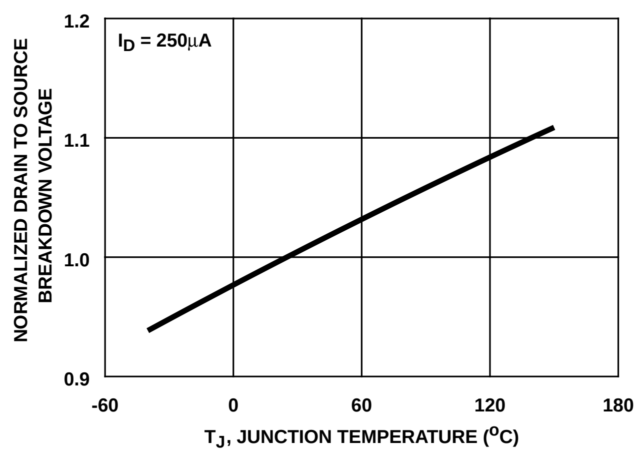


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

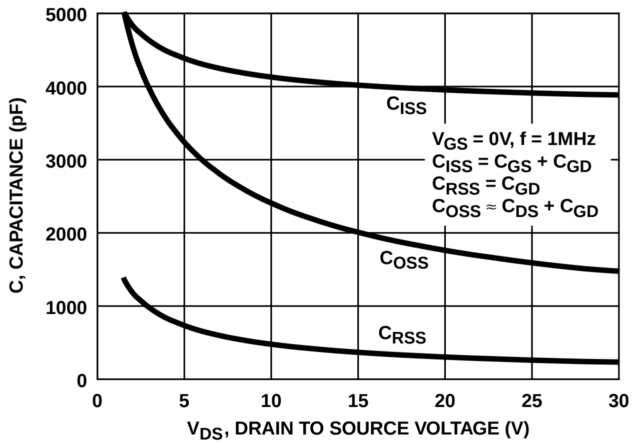
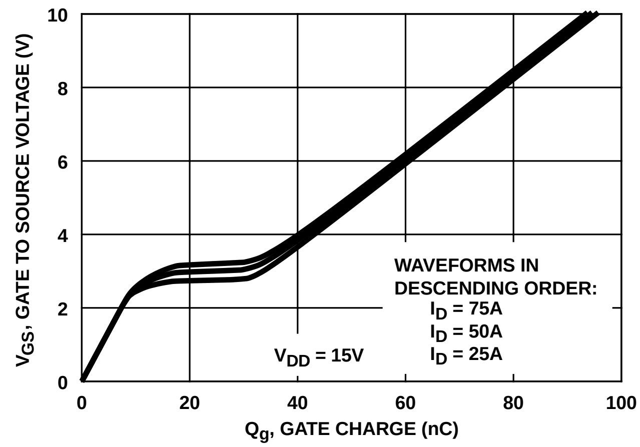


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes 7254 and 7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

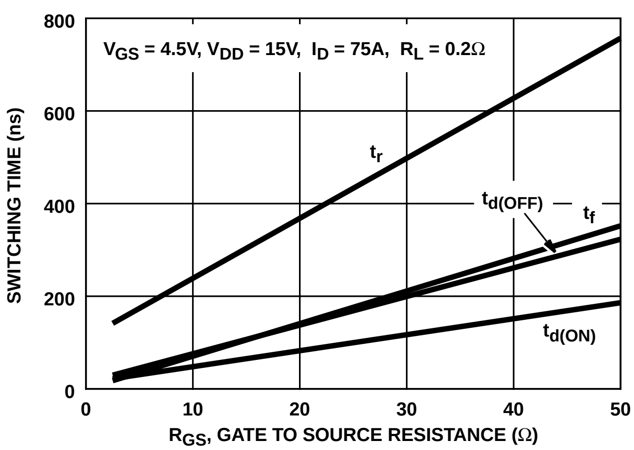


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

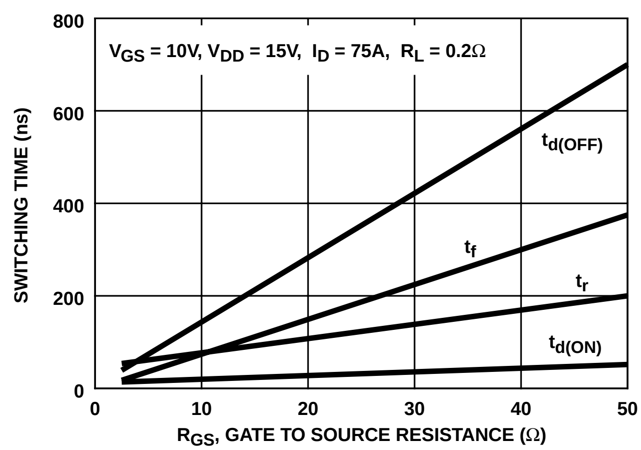


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

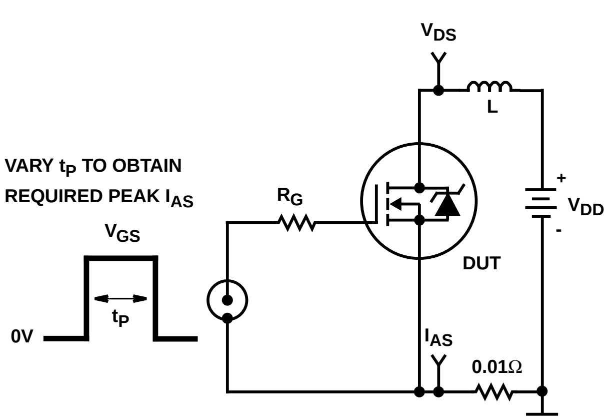


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

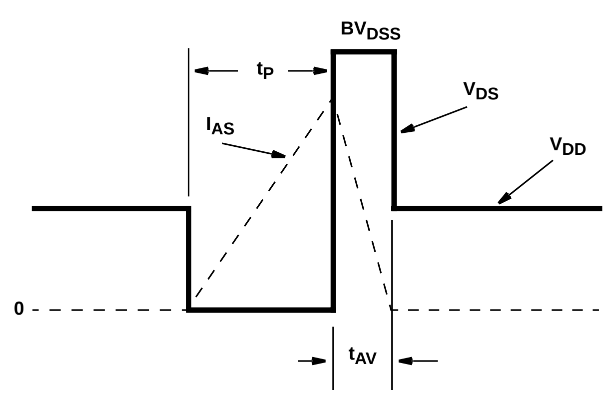


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

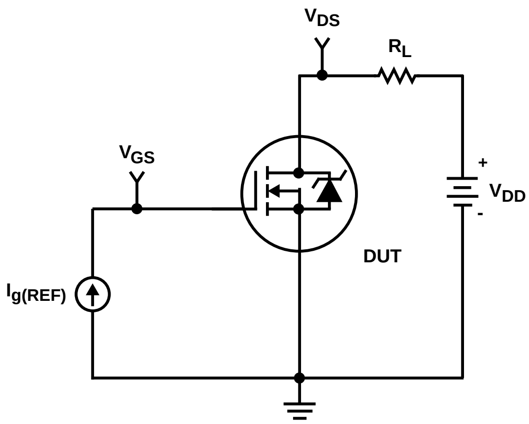


FIGURE 19. GATE CHARGE TEST CIRCUIT

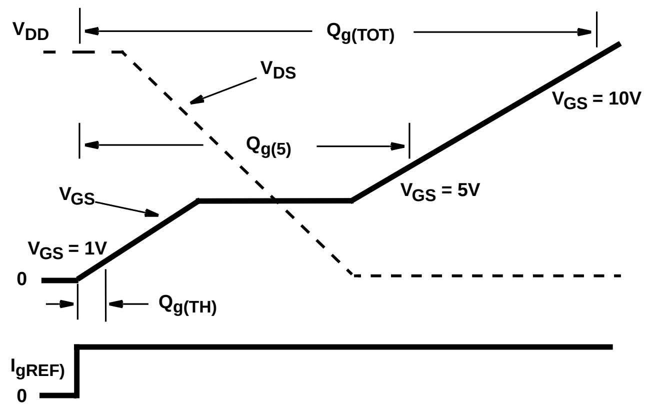


FIGURE 20. GATE CHARGE WAVEFORMS

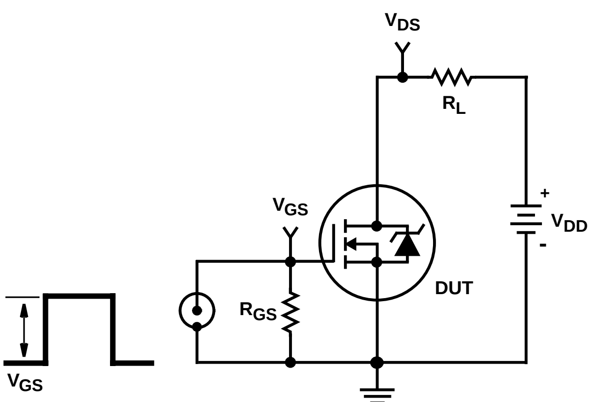


FIGURE 21. SWITCHING TIME TEST CIRCUIT

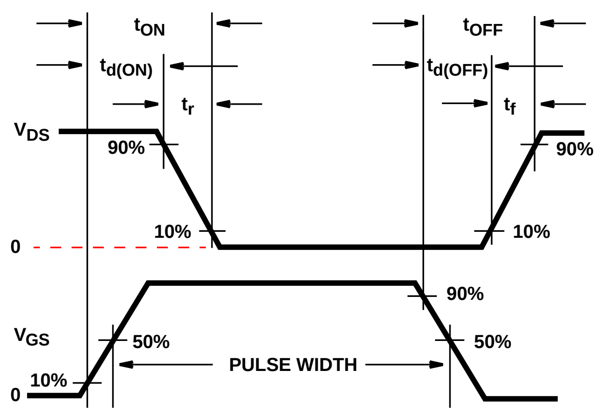
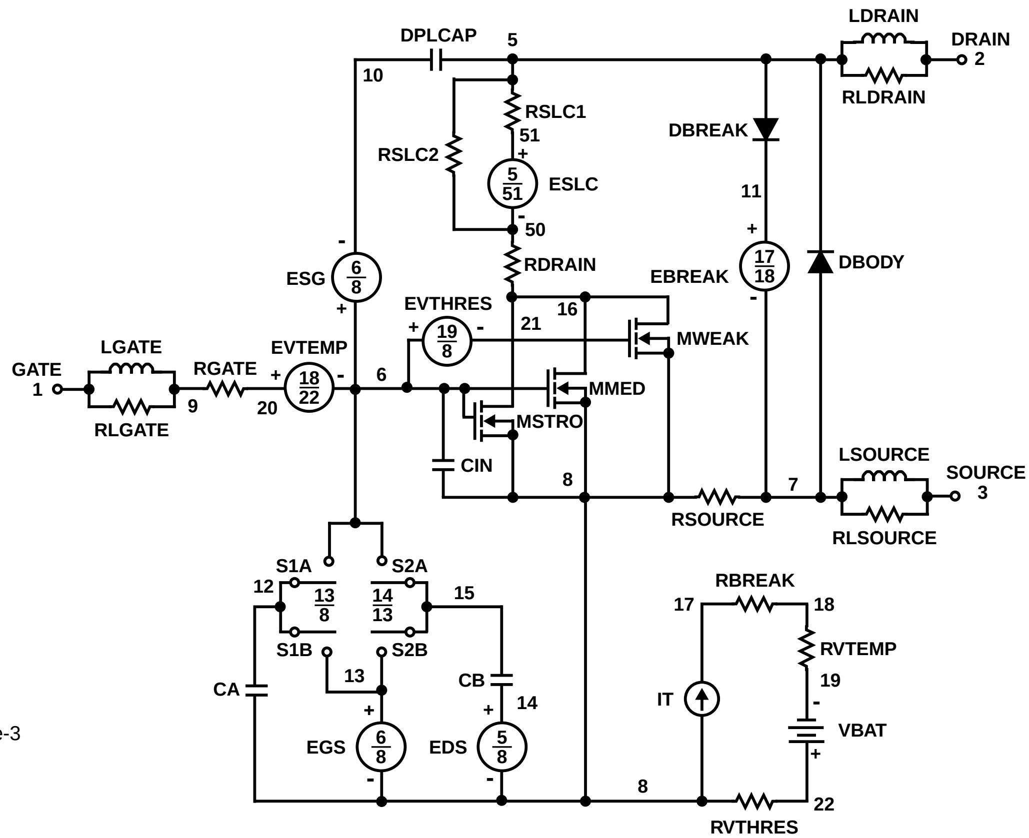


FIGURE 22. SWITCHING TIME WAVEFORM

PSPICE Electrical Model

SUBCKT HUF76143 2 1 3 ;   REV March 1998



CA 12 8 5.2e-9
CB 15 14 5e-9
CIN 6 8 3.65e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 39.38
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 2.6e-9
LSOURCE 3 7 1.1e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 1.5e-3
RGATE 9 20 0.92
RLDRAIN 2 5 10
RLGATE 1 9 26
RLSOURCE 3 7 11
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 3e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*425),4))}

.MODEL DBODYMOD D (IS = 1.2e-11 RS = 2.65e-3 TRS1 = 2.3e-3 TRS2 = -4.2e-6 CJO = 5.45e-9 TT = 3.9e-8 XTI = 4.3 N = 1.03 M = 0.43)
.MODEL DBREAKMOD D (RS = 8.5e-2 TRS1 =0 TRS2 =0)
.MODEL DPLCAPMOD D (CJO = 2.6e-9 IS = 1e-30 N = 10 M = 0.7)
.MODEL MMEDMOD NMOS (VTO = 1.9 KP = 10 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 0.92)
.MODEL MSTROMOD NMOS (VTO = 2.26KP = 215 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.62 KP = 0.1 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 9.2 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 9.8e-4 TC2 = -4e-7)
.MODEL RDRAINMOD RES (TC1 = 1e-2 TC2 = 0)
.MODEL RSLCMOD RES (TC1 = 3e-3 TC2 = -2e-5)
.MODEL RSOURCEMOD RES (TC1 = 5e-4 TC2 = 1.1e-5)
.MODEL RVTHRESMOD RES (TC = -2.2e-3 TC2 = -6e-6)
.MODEL RVTEMPMOD RES (TC1 = -1.45e-3 TC2 = -2e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5 VOFF= -2)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2 VOFF= -5)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.5 VOFF= 1)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1 VOFF= -1.5)

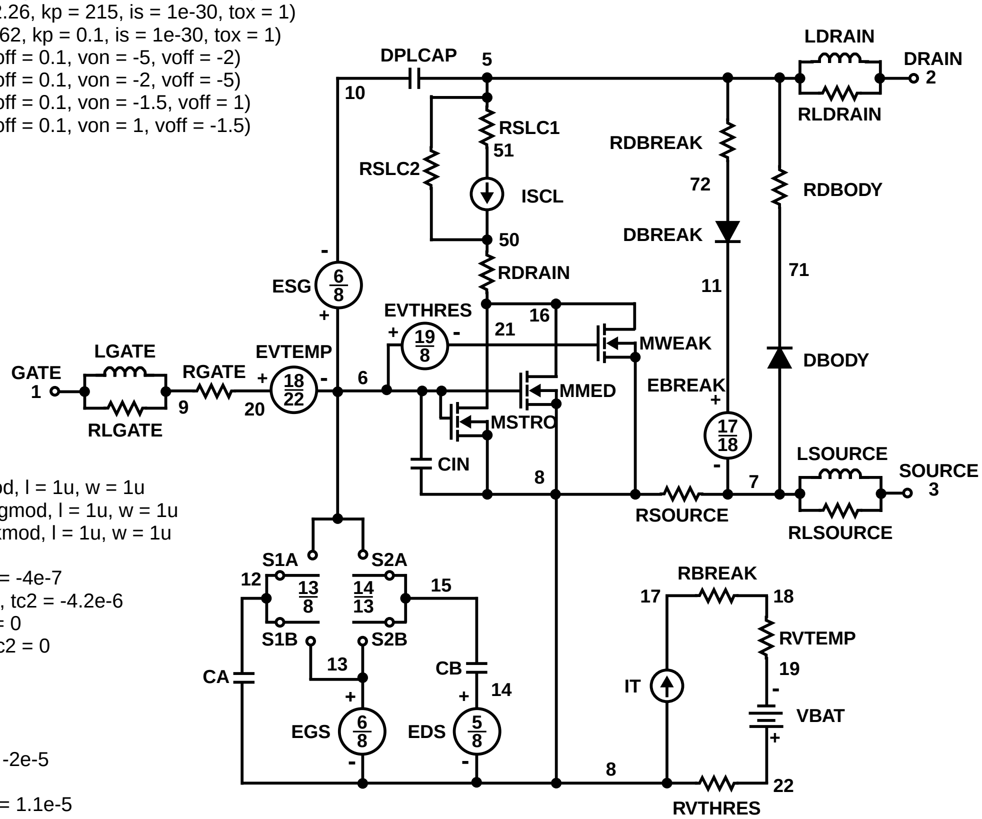
.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

REV March 1998

```
template huf76143 n2, n1, n3
electrical n2, n1, n3
{
var i iscl
d..model dbodymod =  (is = 1.2e-11, xti = 4.3, cjo = 5.45e-9, tt = 3.9e-8, n = 1.03, m = 0.43)
d..model dbreakmod = ()
d..model dplcapmod =  (cjo = 2.6e-9, is = 1e-30, n = 10, m = 0.70)
m..model mmedmod = (type=_n, vto = 1.9, kp = 10, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 2.26, kp = 215, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 1.62, kp = 0.1, is = 1e-30, tox = 1)
sw_vcsp..model s1amod =  (ron = 1e-5, roff = 0.1, von = -5, voff = -2)
sw_vcsp..model s1bmod =  (ron = 1e-5, roff = 0.1, von = -2, voff = -5)
sw_vcsp..model s2amod =  (ron = 1e-5, roff = 0.1, von = -1.5, voff = 1)
sw_vcsp..model s2bmod =  (ron = 1e-5, roff = 0.1, von = 1, voff = -1.5)

c.ca n12 n8 = 5.2e-9
c.cb n15 n14 = 5e-9
c.cin n6 n8 = 3.65e-9

d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1e-9
l.lgate n1 n9 = 2.6e-9
l.lsource n3 n7 = 1.1e-9

m.mmed n16 n6 n8 n8 = model=mmedmod, l = 1u, w = 1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l = 1u, w = 1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l = 1u, w = 1u

res.rbreak n17 n18  = 1, tc1 = 9.8e-4, tc2 = -4e-7
res.rdbody n71 n5 = 2.65e-3, tc1 = 2.3e-3, tc2 = -4.2e-6
res.rdbreak n72 n5 = 8.5e-2, tc1 = 0, tc2 = 0
res.rdrain n50 n16  = 1.5e-3, tc1 = 1e-2, tc2 = 0
res.rgate n9 n20 = 0.92
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 26
res.rlsource n3 n7 = 11
res.rslc1 n5 n51  = 1e-6, tc1 = 3e-3, tc2 = -2e-5
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 3e-3, tc1 = 5e-4, tc2 = 1.1e-5
res.rvtemp n18 n19  = 1, tc1 = -1.45e-3, tc2 = -2e-6
res.rvthres n22 n8  = 1, tc1 = -2.2e-3, tc2 = -6e-6

spe.ebreak n11 n7 n17 n18 = 39.38
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc = 1

equations {
i (n51->n50) + = iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/425))** 4))
}
}
```



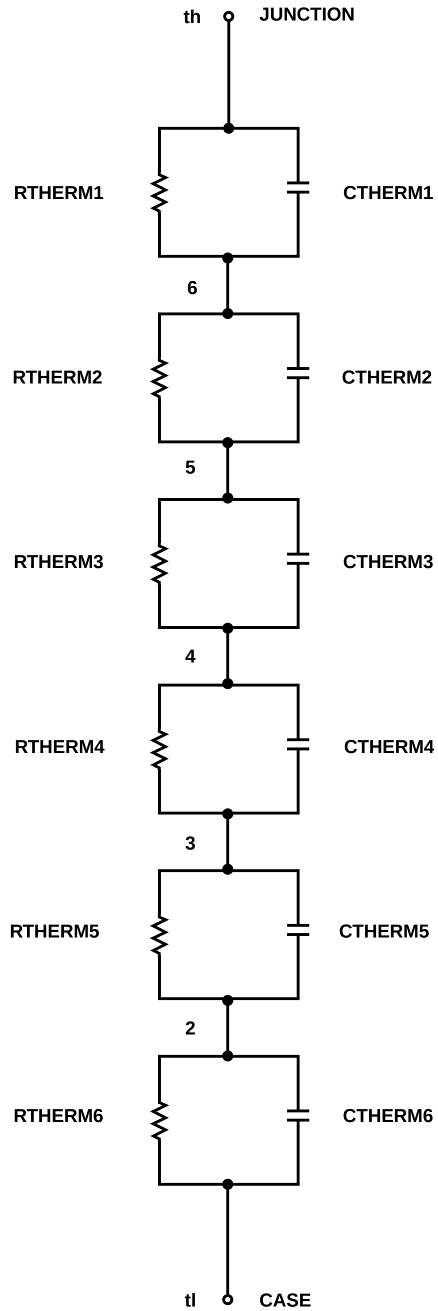
SPICE Thermal Model

REV March 1998

HUF76143

CTHERM1 th 6 5.0e-3
CTHERM2 6 5 1.2e-2
CTHERM3 5 4 2.0e-2
CTHERM4 4 3 2.8e-2
CTHERM5 3 2 2e-1
CTHERM6 2 tl 3

RTHERM1 th 6 2.0e-3
RTHERM2 6 5 2.0e-2
RTHERM3 5 4 6.9e-2
RTHERM4 4 3 1.3e-1
RTHERM5 3 2 7.5e-2
RTHERM6 2 tl 3.0e-2



SABER Thermal Model

Saber thermal model HUF76143

```
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 5.0e-3
ctherm.ctherm2 6 5 = 1.2e-2
ctherm.ctherm3 5 4 = 2.0e-2
ctherm.ctherm4 4 3 = 2.8e-2
ctherm.ctherm5 3 2 = 2.0e-1
ctherm.ctherm6 2 tl = 3

rtherm.rtherm1 th 6 = 2.0e-3
rtherm.rtherm2 6 5 = 2.0e-2
rtherm.rtherm3 5 4 = 6.9e-2
rtherm.rtherm4 4 3 = 1.3e-1
rtherm.rtherm5 3 2 = 7.5e-2
rtherm.rtherm6 2 tl = 3.0e-2
}
```