

75A, 30V, 0.0045 Ohm, N-Channel, Logic Level UltraFET Power MOSFETs



These N-Channel power MOSFETs are manufactured using the innovative UltraFET™ process.

This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA76145.

Ordering Information

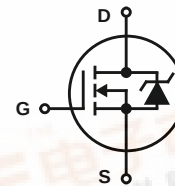
PART NUMBER	PACKAGE	BRAND
HUF76145P3	TO-220AB	76145P
HUF76145S3S	TO-263AB	76145S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF76145S3ST.

Features

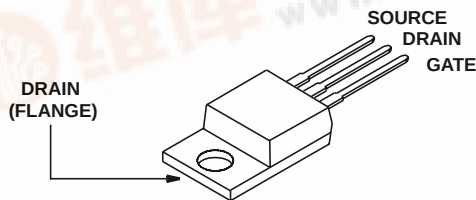
- Logic Level Gate Drive
- 75A, 30V
- Ultra Low On-Resistance, $r_{DS(ON)} = 0.0045\Omega$
- Temperature Compensating PSPICE™ Model
- Temperature Compensating SABER Model
- Thermal Impedance SPICE Model
- Thermal Impedance SABER Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
 - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

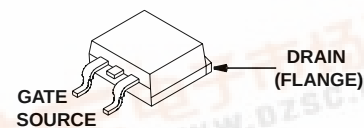


Packaging

JEDEC TO-220AB



JEDEC TO-263AB



HUF76145P3, HUF76145S3S

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

		UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	30 V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR}	30 V
Gate to Source Voltage	V_{GS}	± 16 V
Drain Current		
Continuous ($T_C = 25^{\circ}\text{C}$, $V_{GS} = 10\text{V}$) (Figure 2)	I_D	75 A
Continuous ($T_C = 100^{\circ}\text{C}$, $V_{GS} = 5\text{V}$)	I_D	75 A
Continuous ($T_C = 100^{\circ}\text{C}$, $V_{GS} = 4.5\text{V}$) (Figure 2)	I_D	75 A
Pulsed Drain Current	I_{DM}	Figure 4
Pulsed Avalanche Rating	E_{AS}	Figures 6, 17, 18
Power Dissipation	P_D	270 W
Derate Above 25°C		2.17 $\text{W}/^{\circ}\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-40 to 150 $^{\circ}\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300 $^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260 $^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}\text{C}$ to 150°C .

Electrical Specifications $T_A = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS						
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 12)	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 25V, V _{GS} = 0V	-	-	1	μA
		V _{DS} = 25V, V _{GS} = 0V, T _C = 150°C	-	-	250	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±16V	-	-	±100	nA
ON STATE SPECIFICATIONS						
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 11)	1	-	3	V
Drain to Source On Resistance	r _{DS(ON)}	I _D = 75A, V _{GS} = 10V (Figure 9, 10)	-	0.0035	0.0045	Ω
		I _D = 75A, V _{GS} = 5V (Figure 9)	-	0.0043	0.0058	Ω
		I _D = 75A, V _{GS} = 4.5V (Figure 9)	-	0.0046	0.0065	Ω
THERMAL SPECIFICATIONS						
Thermal Resistance Junction to Case	R _{θJC}	(Figure 3)	-	-	0.46	°C/W
Thermal Resistance Junction to Ambient	R _{θJA}	TO-220 and TO-263	-	-	62	°C/W
SWITCHING SPECIFICATIONS (V _{GS} = 4.5V)						
Turn-On Time	t _{ON}	V _{DD} = 15V, I _D ≅ 75A, R _L = 0.20Ω, V _{GS} = 4.5V, R _{GS} = 2.5Ω (Figures 15, 20, 21)	-	-	255	ns
Turn-On Delay Time	t _{d(ON)}		-	26	-	ns
Rise Time	t _r		-	145	-	ns
Turn-Off Delay Time	t _{d(OFF)}		-	35	-	ns
Fall Time	t _f		-	39	-	ns
Turn-Off Time	t _{OFF}		-	-	110	ns

HUF76145P3, HUF76145S3S

Electrical Specifications $T_A = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
SWITCHING SPECIFICATIONS (V _{GS} = 10V)							
Turn-On Time	t _{ON}	V _{DD} = 15V, I _D ≅ 75A, R _L = 0.20Ω, V _{GS} = 10V, R _{GS} = 2.2Ω (Figures 16, 20, 21)	-	-	110	ns	
Turn-On Delay Time	t _{d(ON)}		-	16	-	ns	
Rise Time	t _r		-	57	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	53	-	ns	
Fall Time	t _f		-	38	-	ns	
Turn-Off Time	t _{OFF}		-	-	135	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 10V	V _{DD} = 15V, I _D ≅ 75A, R _L = 0.20Ω I _{g(REF)} = 1.0mA (Figures 14, 19, 20)	-	130	156	nC
Gate Charge at 5V	Q _{g(5)}	V _{GS} = 0V to 5V		-	73	88	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 1V		-	4.65	5.6	nC
Gate to Source Gate Charge	Q _{gs}			-	12.30	-	nC
Gate to Drain “Miller” Charge	Q _{gd}			-	40.00	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz (Figure 13)	-	4900	-	pF	
Output Capacitance	C _{OSS}		-	2520	-	pF	
Reverse Transfer Capacitance	C _{RSS}		-	560	-	pF	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 75\text{A}$	-	-	1.25	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 75\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	115	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 75\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	255	nC

Typical Performance Curves

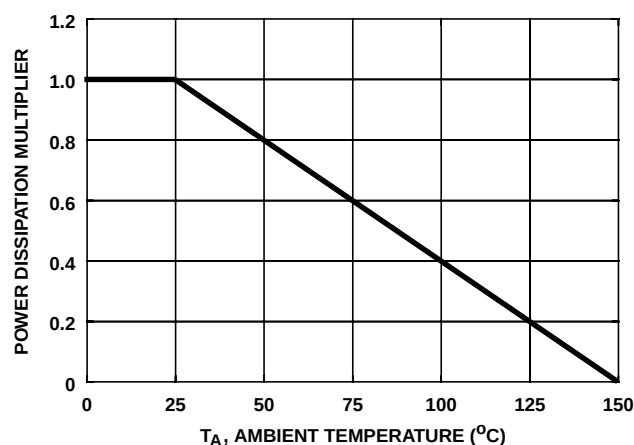


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

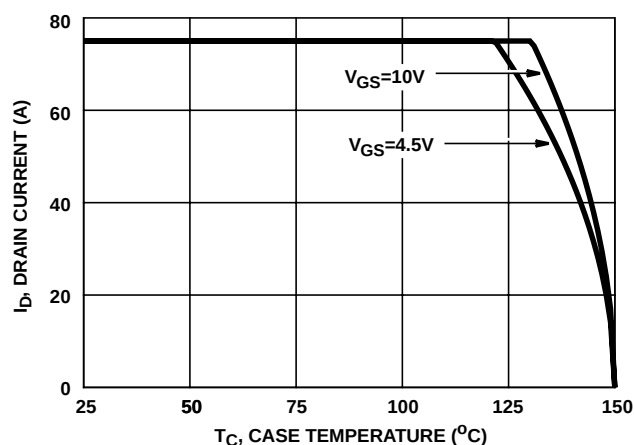


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

Typical Performance Curves (Continued)

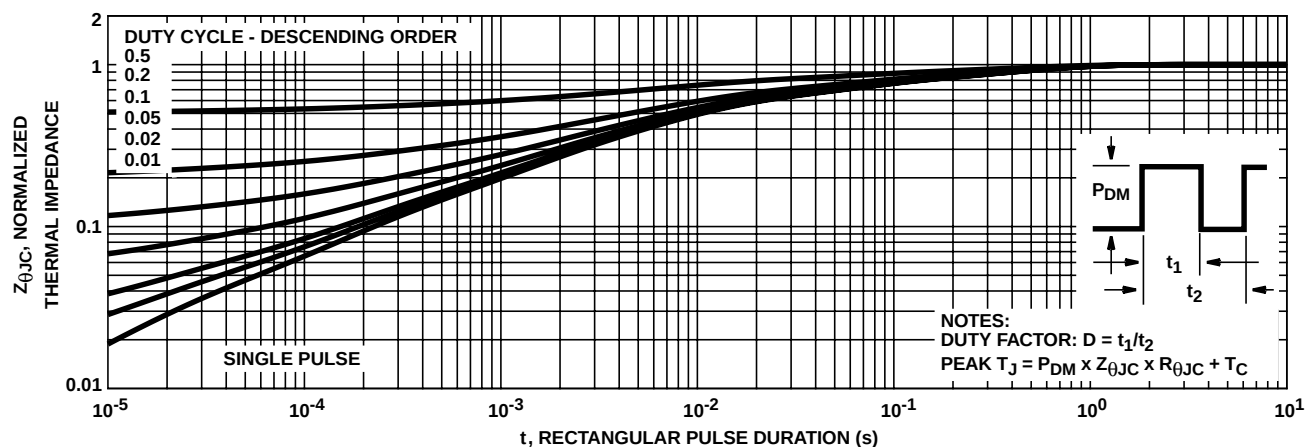


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

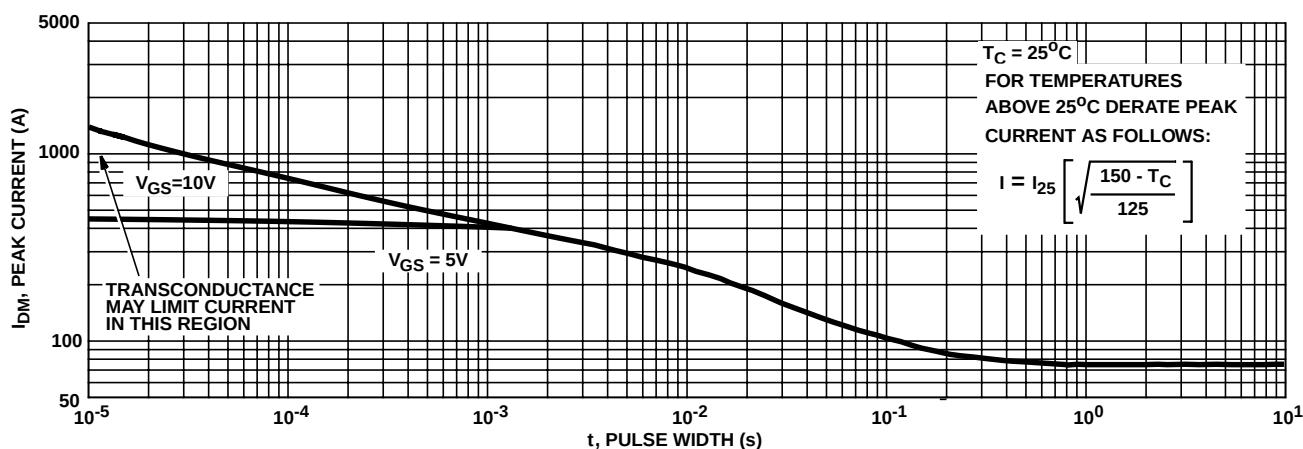


FIGURE 4. PEAK CURRENT CAPABILITY

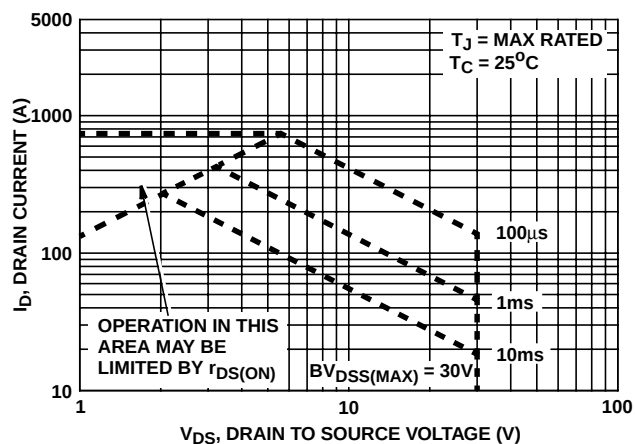
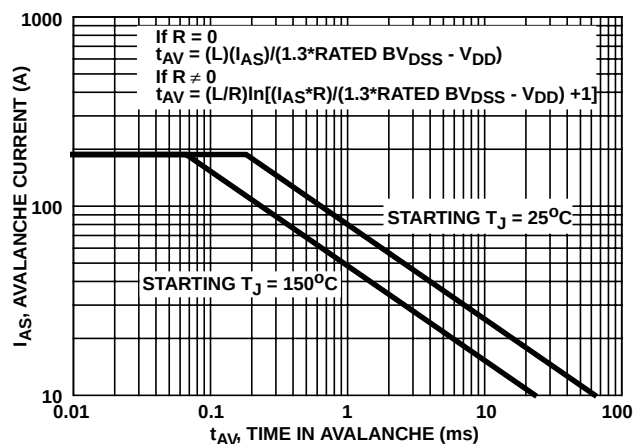


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

Typical Performance Curves (Continued)

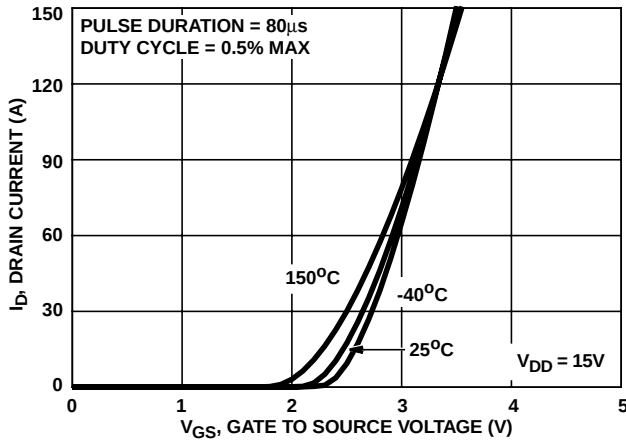


FIGURE 7. TRANSFER CHARACTERISTICS

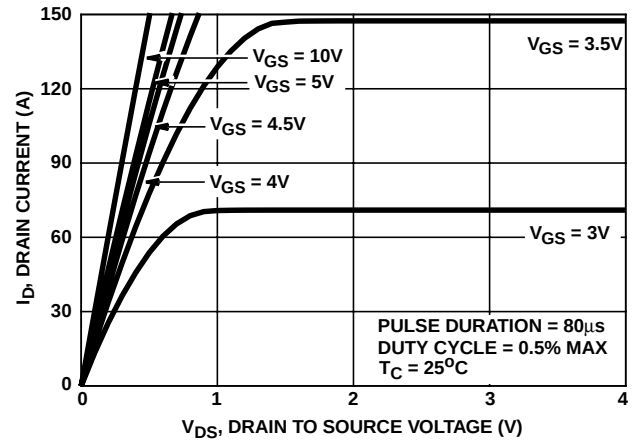


FIGURE 8. SATURATION CHARACTERISTICS

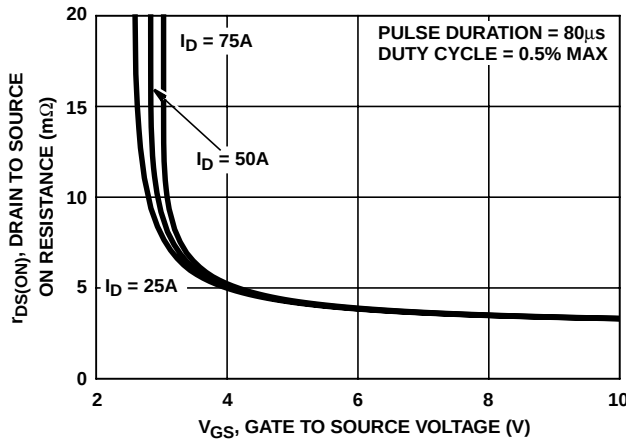


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

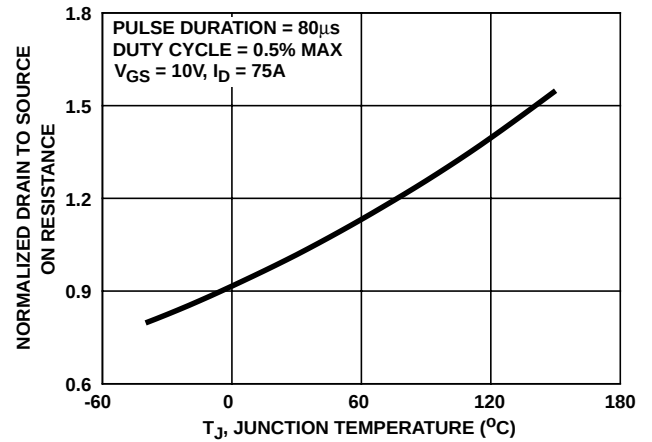


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

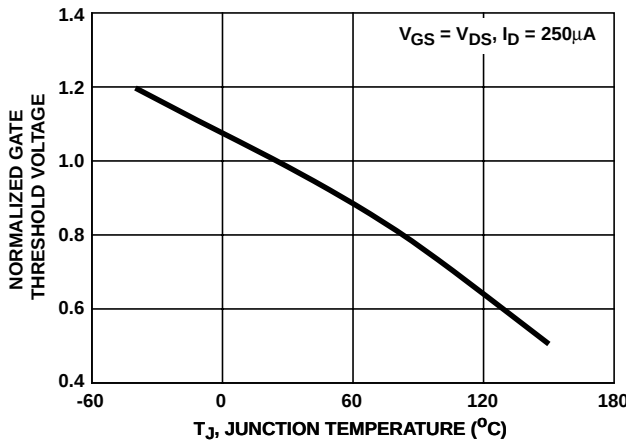


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

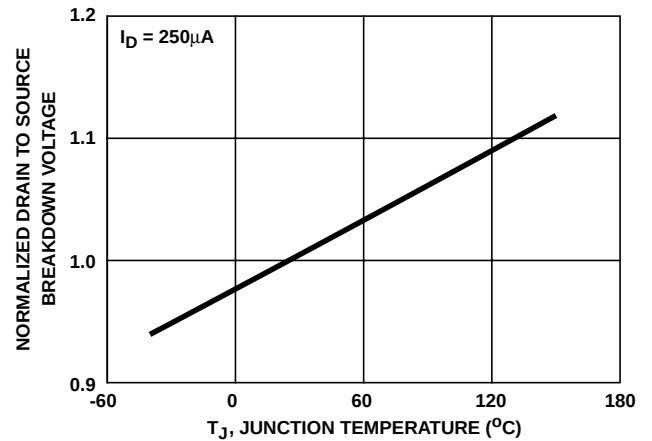


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

HUF76145P3, HUF76145S3S

Typical Performance Curves (Continued)

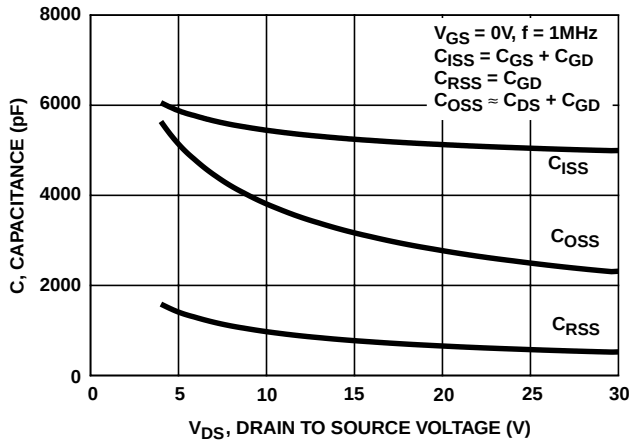
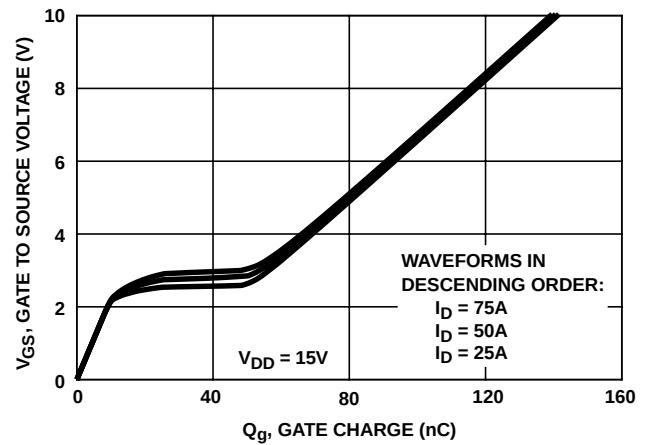


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

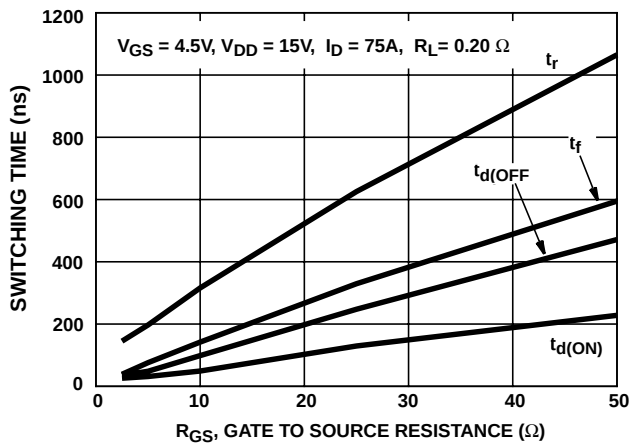


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

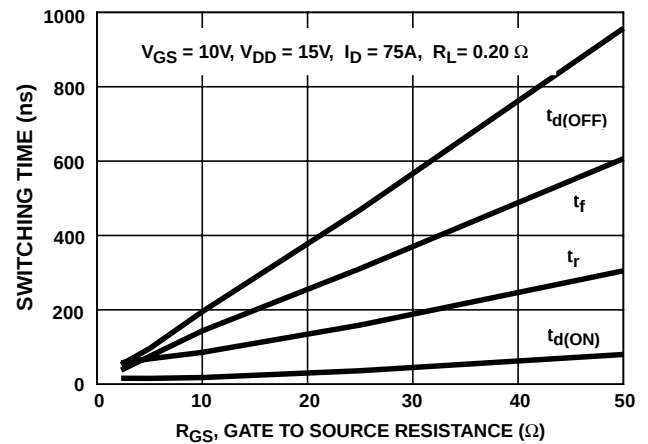


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

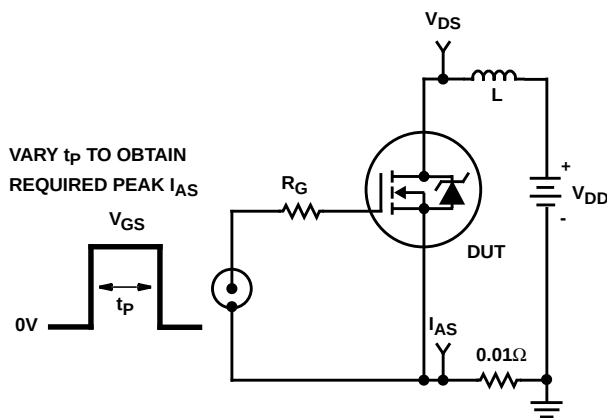


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

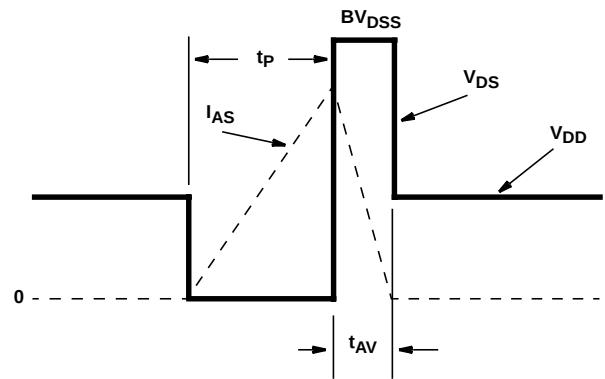


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

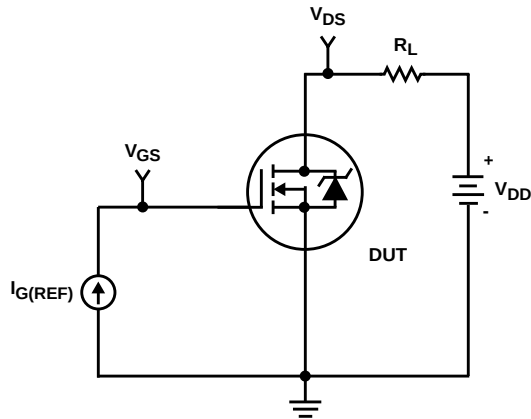


FIGURE 19. GATE CHARGE TEST CIRCUIT

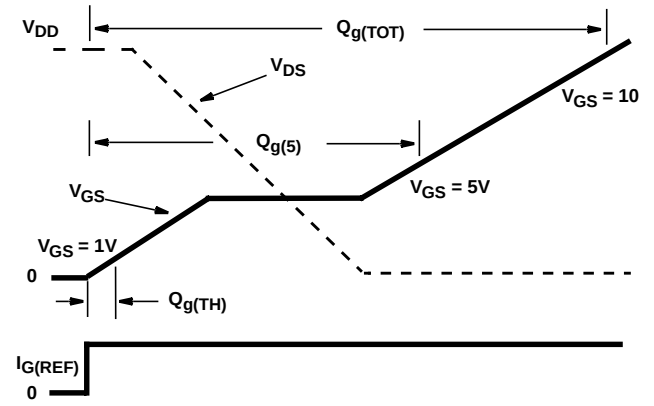


FIGURE 20. GATE CHARGE WAVEFORMS

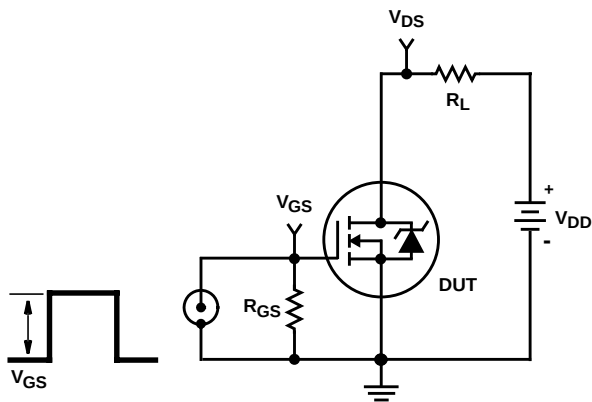


FIGURE 21. SWITCHING TIME TEST CIRCUIT

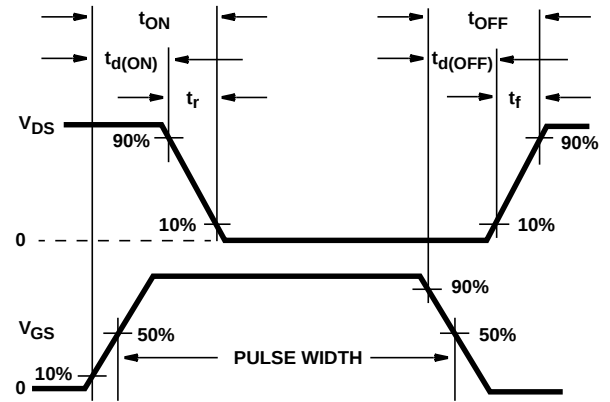


FIGURE 22. SWITCHING TIME WAVEFORM

HUF76145P3, HUF76145S3S

PSPICE Electrical Model

SUBCKT HUF76145 2 1 3 ; rev 6 Apr98

CA 12 8 7.75e-9
CB 15 14 7.45e-9
CIN 6 8 4.47e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 33.5
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1.00e-9
LGATE 1 9 2.60e-9
LSOURCE 3 7 1.10e-9
KGATE LSOURCE LGATE 0.0085

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 0.59e-3
RGATE 9 20 0.898
RLDRAIN 2 5 10
RLGATE 1 9 26
RLSOURCE 3 7 11
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 2.20e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

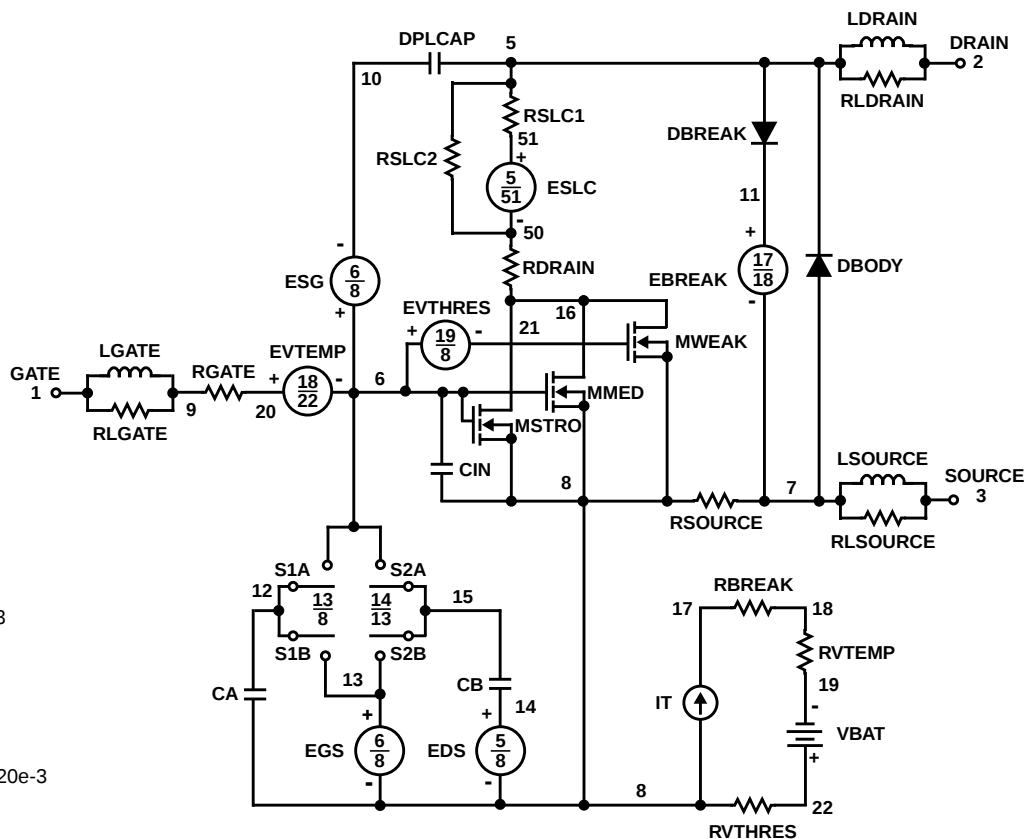
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*750),3))}

.MODEL DBODYMOD D (IS = 6.01e-12 IKF = 20 RS = 1.72e-3 TRS1 = 1.01e-3 TRS2 = 1.21e-6 CJO = 8.41e-9 TT = 4.84e-8 M = 0.45)
.MODEL DBREAKMOD D (RS = 6.80e-2 TRS1 = 1.12e-3 TRS2 = 1.25e-6)
.MODEL DPLCAPMOD D (CJO = 4.25e-9 IS = 1e-30 N = 10 M = 0.61)
.MODEL MSTROMOD NMOS (VTO = 1.74 KP = 5.00 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 0.898)
.MODEL MWEAKMOD NMOS (VTO = 1.48 KP = 0.10 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 8.98 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.01e-3 TC2 = 1.07e-7)
.MODEL RDRAINMOD RES (TC1 = 1.58e-2 TC2 = 3.76e-5)
.MODEL RSLCMOD RES (TC1 = 1.02e-4 TC2 = -1.13e-4)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = -2.73e-3 TC2 = -1.01e-5)
.MODEL RVTEMPMOD RES (TC1 = -1.50e-3 TC2 = 1.25e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.00 VOFF = -1.50)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.50 VOFF = -6.00)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.00 VOFF = 0.45)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.45 VOFF = 0.00)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



HUF76145P3, HUF76145S3S

SPICE Thermal Model

REV 14 April 1998

HUF76145

CTHERM1 th 6 5.00e-5
CTHERM2 6 5 1.00e-3
CTHERM3 5 4 2.50e-3
CTHERM4 4 3 9.00e-3
CTHERM5 3 2 3.30e-2
CTHERM6 2 tl 7.00e-2

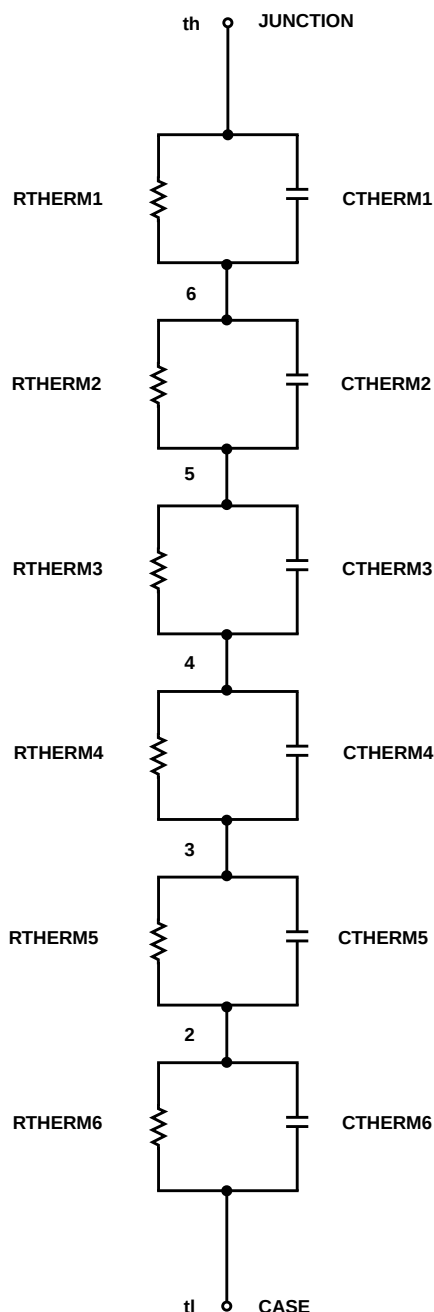
RTHERM1 th 6 2.00e-5
RTHERM2 6 5 2.06e-3
RTHERM3 5 4 6.71e-3
RTHERM4 4 3 2.07e-2
RTHERM5 3 2 4.12e-2
RTHERM6 2 tl 1.06e-1

SABER Thermal Model

Saber thermal model HUF76145

```
template thermal_model th tl
thermal_c th, tl
{
  ctherm.ctherm1 th 6 = 5.0e-5
  ctherm.ctherm2 6 5 = 1.00e-3
  ctherm.ctherm3 5 4 = 2.50e-3
  ctherm.ctherm4 4 3 = 9.00e-3
  ctherm.ctherm5 3 2 = 3.30e-2
  ctherm.ctherm6 2 tl = 7.00e-2

  rtherm.rtherm1 th 6 = 2.00e-5
  rtherm.rtherm2 6 5 = 2.06e-3
  rtherm.rtherm3 5 4 = 6.71e-3
  rtherm.rtherm4 4 3 = 2.07e-2
  rtherm.rtherm5 3 2 = 4.12e-2
  rtherm.rtherm6 2 tl = 1.06e-1
}
```



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