

International IR Rectifier

PD- 94160

IRF7704

HEXFET® Power MOSFET

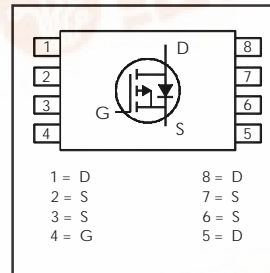
- Ultra Low On-Resistance
- P-Channel MOSFET
- Very Small SOIC Package
- Low Profile (< 1.1mm)
- Available in Tape & Reel

V _{DSS}	R _{DS(on)} max (mΩ)	I _D
-40V	46@V _{GS} = -10V	-4.6A
	74@V _{GS} = -4.5V	-3.7A

Description

HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the ruggedized device design, that International Rectifier is well known for, provides the designer with an extremely efficient and reliable device for battery and load management.

The TSSOP-8 package has 45% less footprint area than the standard SO-8. This makes the TSSOP-8 an ideal device for applications where printed circuit board space is at a premium. The low profile (<1.2mm) allows it to fit easily into extremely thin environments such as portable electronics and PCMCIA cards.



Absolute Maximum Ratings

	Parameter	Max.	Units
V _{DS}	Drain- Source Voltage	-40	V
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ -10V	-4.6	A
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ -10V	-3.7	
I _{DM}	Pulsed Drain Current ①	-19	
P _D @ T _A = 25°C	Power Dissipation ③	1.5	W
P _D @ T _A = 70°C	Power Dissipation ③	1.0	
	Linear Derating Factor	12	mW/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
T _J , T _{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

	Parameter	Max.	Units
R _{θJA}	Maximum Junction-to-Ambient③	83	°C/W

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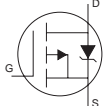
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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

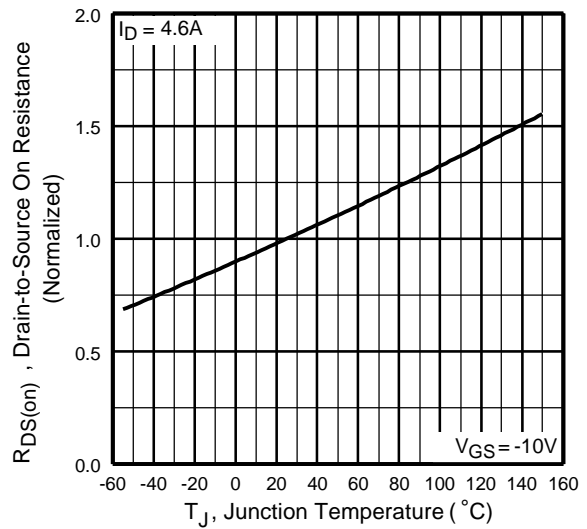
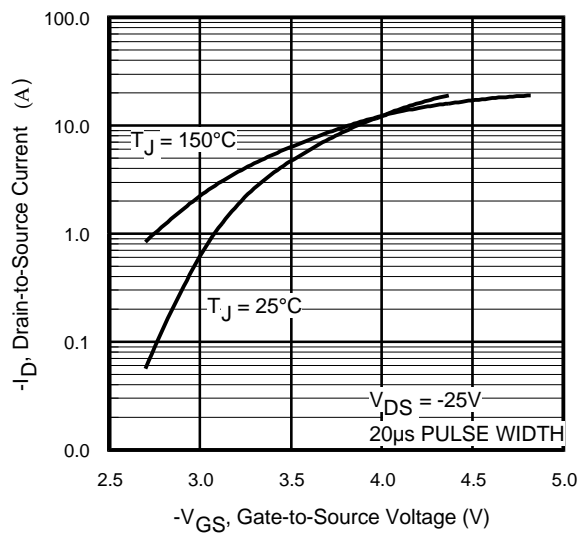
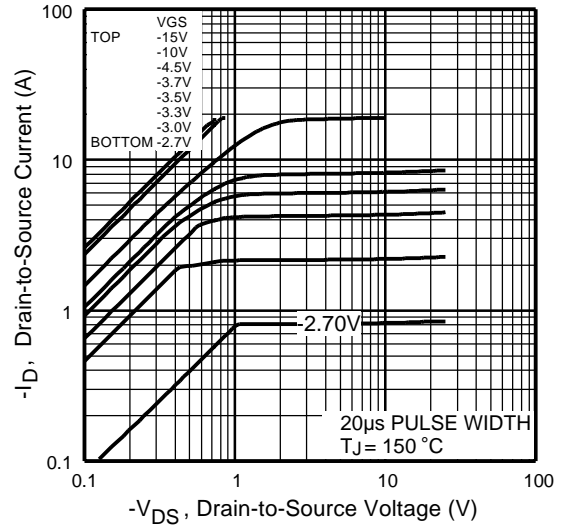
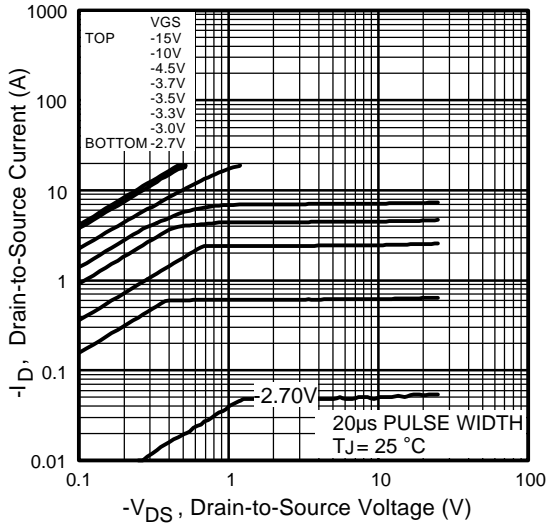
	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-40	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.03	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	46	m Ω	$V_{GS} = -10V, I_D = -4.6A$ ②
		—	—	74		$V_{GS} = -4.5V, I_D = -3.7A$ ②
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	-3.0	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	7.2	—	—	S	$V_{DS} = -10V, I_D = -4.6A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	-10	μA	$V_{DS} = -32V, V_{GS} = 0V$
		—	—	-25		$V_{DS} = -32V, V_{GS} = 0V, T_J = 70^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 20V$
Q_g	Total Gate Charge	—	25	38	nC	$I_D = -4.6A$
Q_{gs}	Gate-to-Source Charge	—	10	15		$V_{DS} = -15V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	9.5	14		$V_{GS} = -4.5V$
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	$V_{DD} = -20V$ ②
t_r	Rise Time	—	360	—		$I_D = -1.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	190	—		$R_G = 6.0\Omega$
t_f	Fall Time	—	100	—		$V_{GS} = -4.5V$
C_{iss}	Input Capacitance	—	3150	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	250	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	200	—		$f = 1.0\text{kHz}$

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-1.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-19		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}, I_S = -1.5A, V_{GS} = 0V$ ②
t_{rr}	Reverse Recovery Time	—	29	44	ns	$T_J = 25^\circ\text{C}, I_F = -1.5A$
Q_{rr}	Reverse Recovery Charge	—	41	62	nC	$di/dt = -100A/\mu s$ ②

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ③ Surface mounted on 1 in square Cu board



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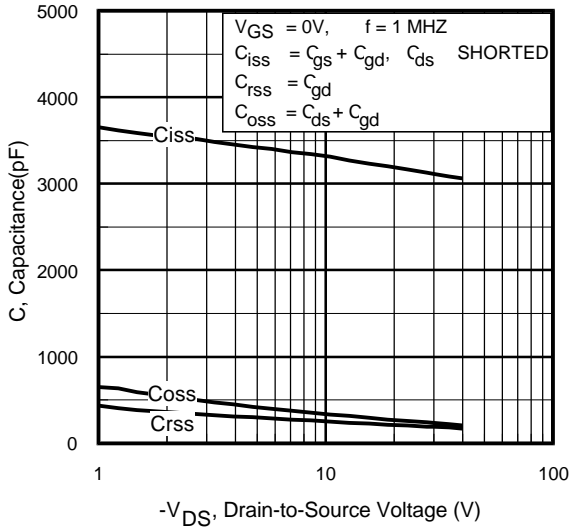


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

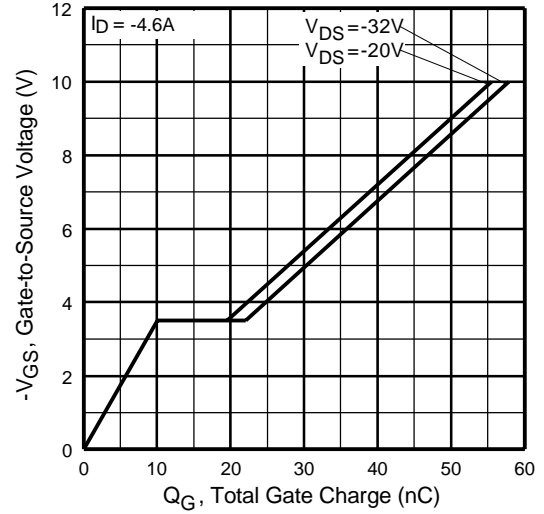


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

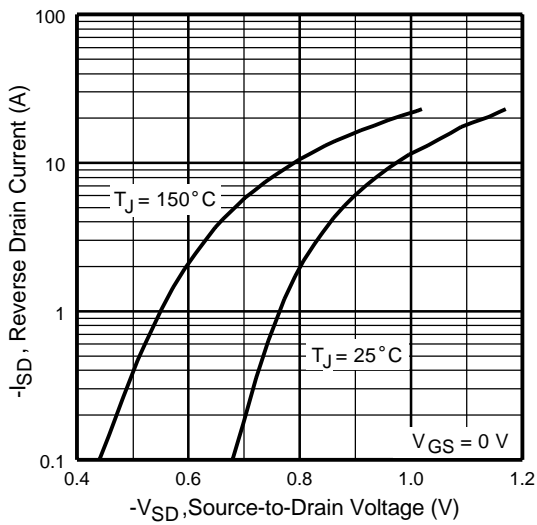


Fig 7. Typical Source-Drain Diode Forward Voltage

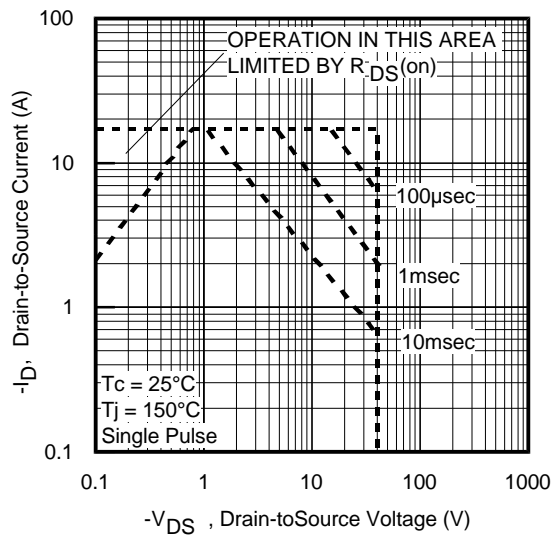


Fig 8. Maximum Safe Operating Area

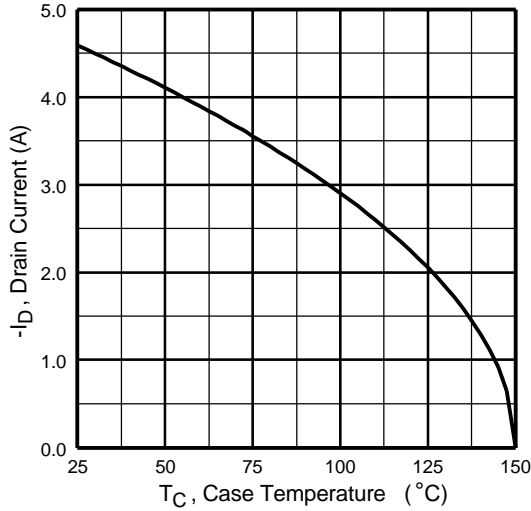


Fig 9. Maximum Drain Current Vs. Case Temperature

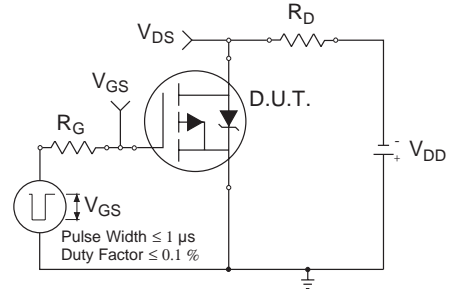


Fig 10a. Switching Time Test Circuit

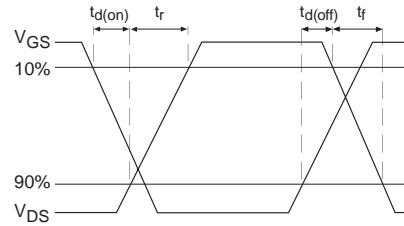


Fig 10b. Switching Time Waveforms

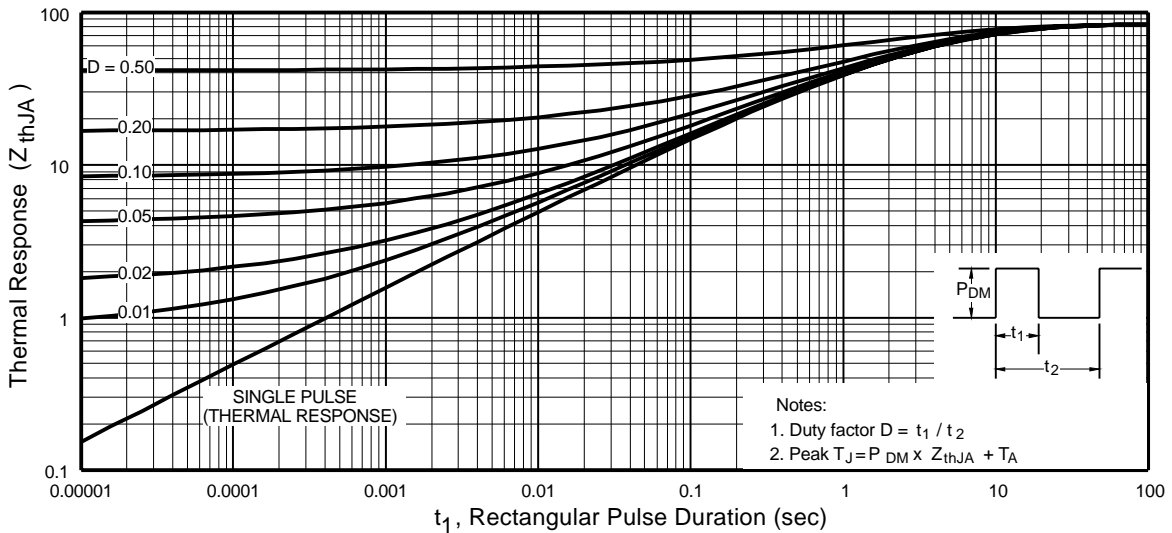


Fig 10. Typical Effective Transient Thermal Impedance, Junction-to-Ambient

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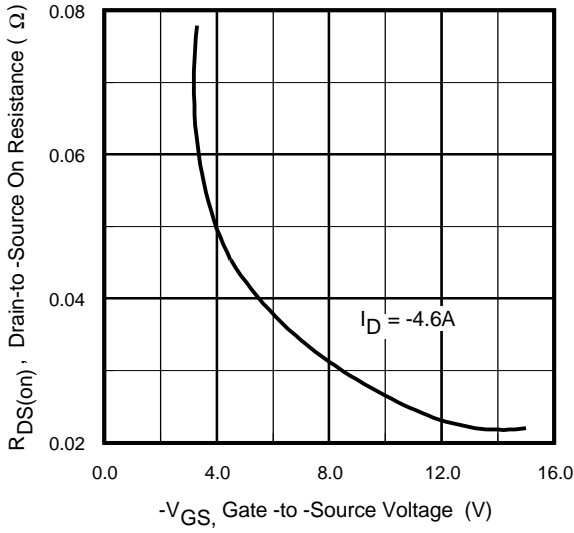


Fig 11. Typical On-Resistance Vs. Gate Voltage

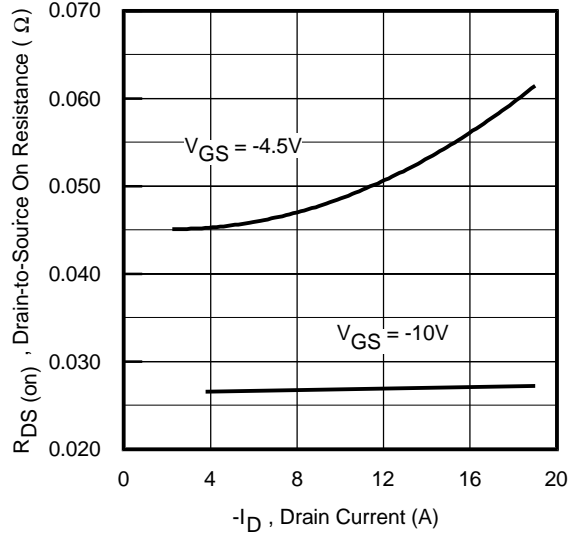


Fig 12. Typical On-Resistance Vs. Drain Current

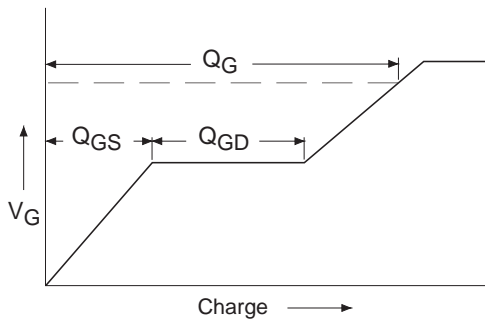


Fig 13a. Basic Gate Charge Waveform

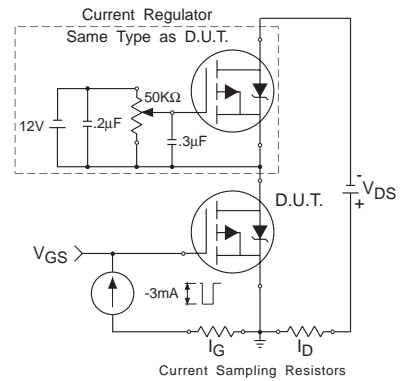


Fig 13b. Gate Charge Test Circuit

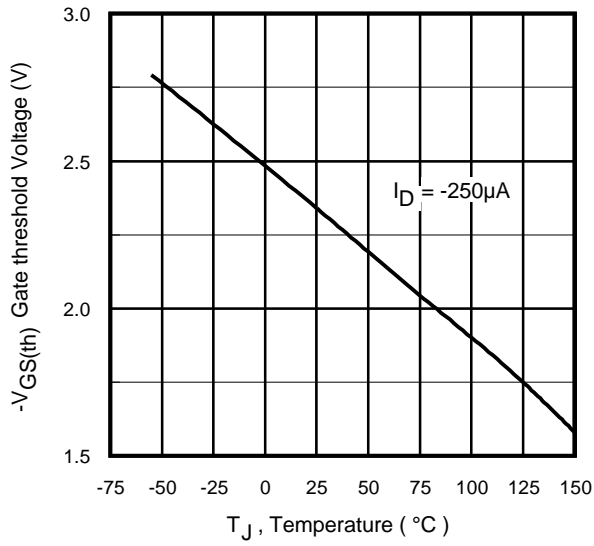


Fig 14. Threshold Voltage Vs. Temperature

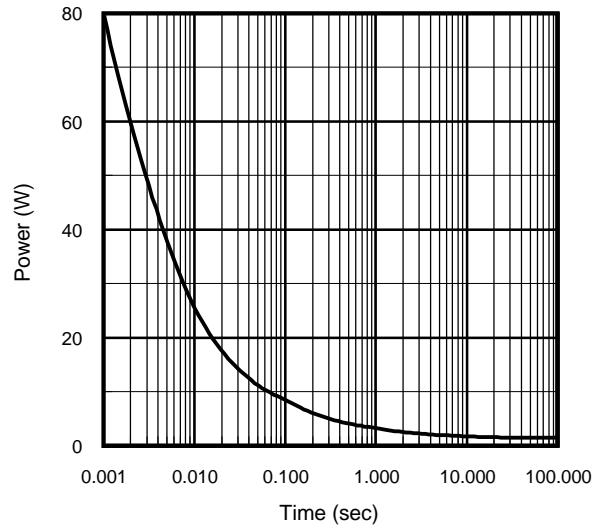
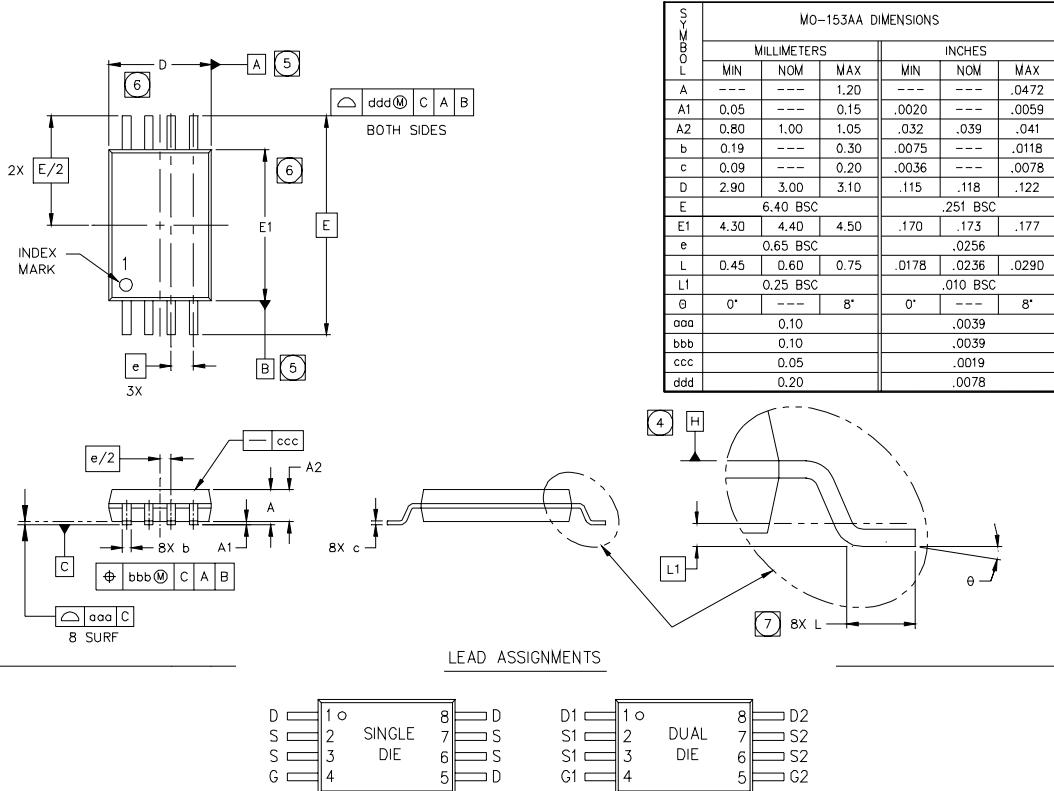


Fig 15. Typical Power Vs. Time

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TSSOP-8 Package Outline



NOTES

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS AND INCHES.
3. CONTROLLING DIMENSION: MILLIMETER.
- ④ DATUM PLANE H IS LOCATED AS SHOWN.
- ⑤ DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
- ⑥ DIMENSIONS D AND E1 ARE MEASURED AT DATUM PLANE H.
- ⑦ DIMENSION L IS THE LEAD LENGTH FOR SOLDERING TO A SUBSTRATE.
8. OUTLINE CONFORMS TO JEDEC OUTLINE MO-153AA.

Data and specifications subject to change without notice.

This product has been designed and qualified for the consumer market.

Qualification Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

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