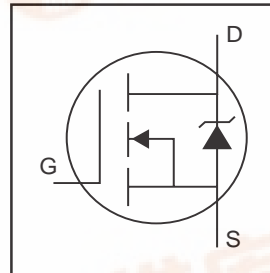


International IR Rectifier

PD-93766

IRF840LCS
IRF840LCL
HEXFET® Power MOSFET

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30V V_{GS} Rating
- Reduced C_{ISS} , C_{OSS} , C_{RSS}
- Extremely High Frequency Operation
- Repetitive Avalanche Rated

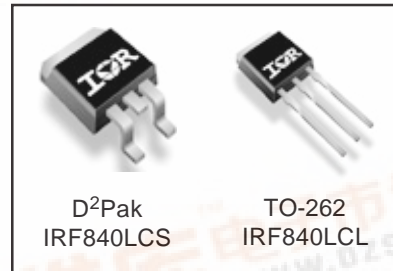


$V_{DSS} = 500V$
$R_{DS(on)} = 0.85\Omega$
$I_D = 8.0A$

Description

This new series of low charge HEXFET® power MOSFETs achieve significant lower gate charge over conventional MOSFETs. Utilizing the new LCDMOS (low charge device MOSFETs) technology, the device improvements are achieved without added product cost, allowing for reduce gate drive requirements and total system savings. In addition, reduced switching losses and improved efficiency and achievable in a variety of high frequency applications. Frequencies of a few MHz at high current are possible using the new low charge MOSFETs.

These device improvements combined with the proven ruggedness and reliability that characterize of HEXFET power MOSFETs offer the designer a new power transistor standard for switching applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑤	8.0	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑤	5.1	
I_{DM}	Pulsed Drain Current ①⑤	28	
$P_D @ T_A = 25^\circ C$	Power Dissipation	3.1	W
$P_D @ T_C = 25^\circ C$	Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy,⑤	510	mJ
I_{AR}	Avalanche Current①	8.0	A
E_{AR}	Repetitive Avalanche Energy①	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	3.5	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)**	—	40	

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.63	—	V/°C	Reference to 25°C , $I_D = 1\text{mA}$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.85	Ω	$V_{GS} = 10V, I_D = 4.8A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	4.0	—	—	S	$V_{DS} = 50V, I_D = 4.8A$ ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 500V, V_{GS} = 0V$ $V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	39	nC	$I_D = 8.0A$ $V_{DS} = 400V$ $V_{GS} = 10V$, See Fig. 6 and 13 ④⑤
Q_{gs}	Gate-to-Source Charge	—	—	10	nC	
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	19	nC	
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	$V_{DD} = 250V$ $I_D = 8.0A$ $R_G = 9.1\Omega$ $R_D = 30\Omega$, See Fig. 10 ④⑤
t_r	Rise Time	—	25	—		
$t_{d(off)}$	Turn-Off Delay Time	—	27	—		
t_f	Fall Time	—	19	—		
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	1100	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$, See Fig. 5⑤
C_{oss}	Output Capacitance	—	170	—		
C_{rss}	Reverse Transfer Capacitance	—	18	—		

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	8.0	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑤	—	—	28		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	$T_J = 25^\circ\text{C}$, $I_S = 8.0A$, $V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	490	740	ns	$T_J = 25^\circ\text{C}$, $I_F = 8.0A$
Q_{rr}	Reverse Recovery Charge	—	3.0	4.5	μC	$di/dt = 100A/\mu s$ ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 14\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 8.0A$. (See Figure 12)
- ③ $I_{SD} \leq 8.0A$, $di/dt \leq 100A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ Uses IRF840LC data and test conditions

** When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended soldering techniques refer to application note #AN-994.

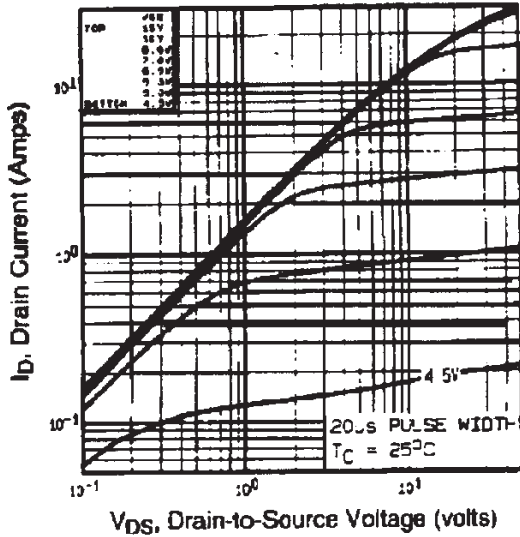


Fig 1. Typical Output Characteristics

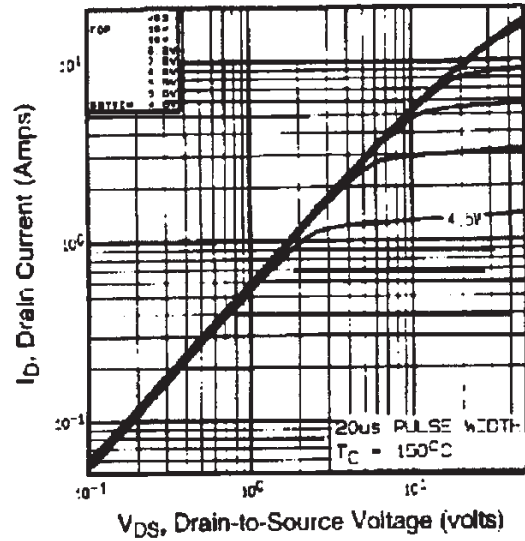


Fig 2. Typical Output Characteristics

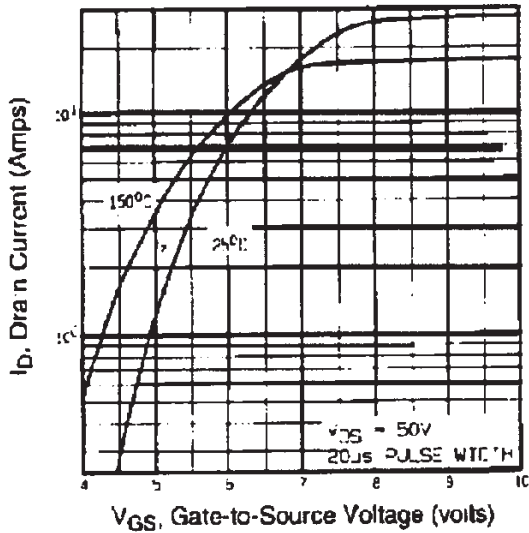


Fig 3. Typical Transfer Characteristics

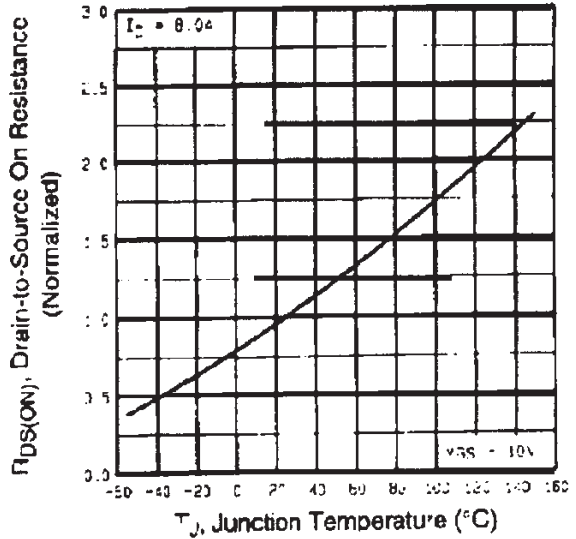


Fig 4. Normalized On-Resistance Vs. Temperature

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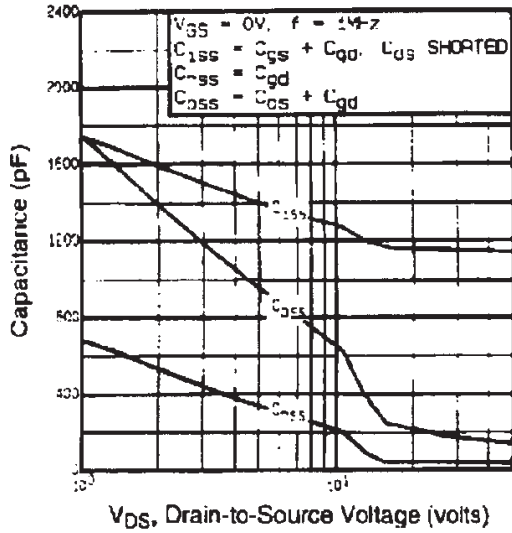


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

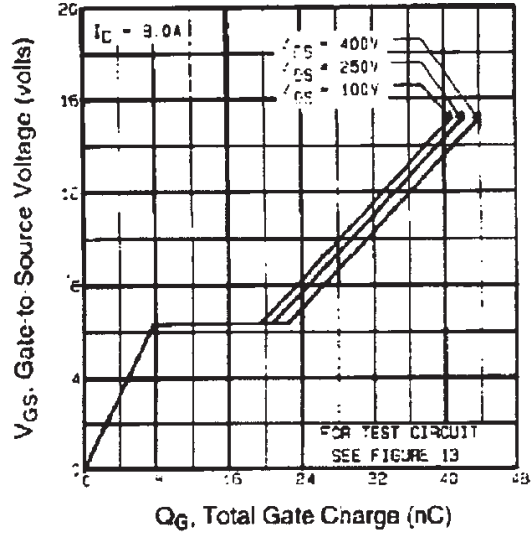


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

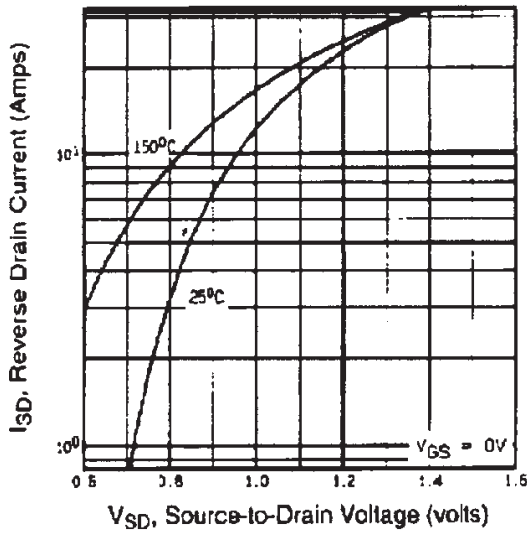


Fig 7. Typical Source-Drain Diode Forward Voltage

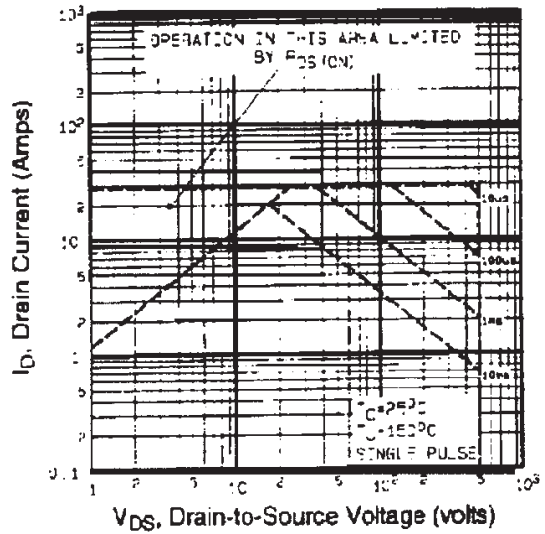


Fig 8. Maximum Safe Operating Area

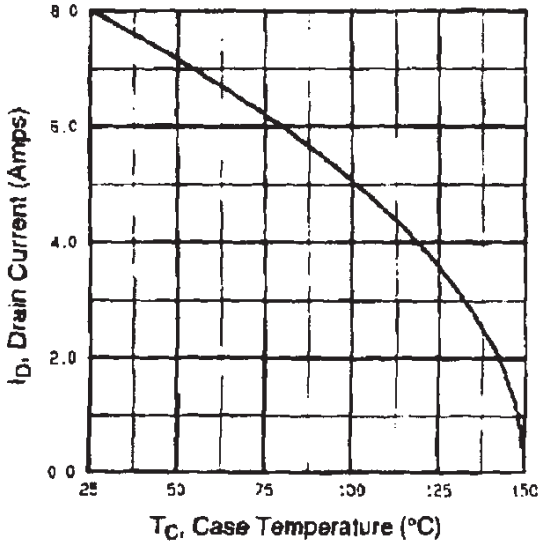


Fig 9. Maximum Drain Current Vs. Case Temperature

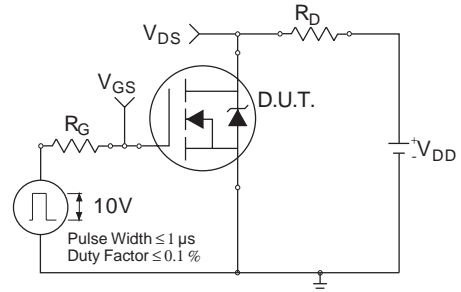


Fig 10a. Switching Time Test Circuit

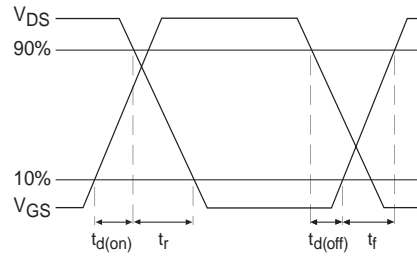


Fig 10b. Switching Time Waveforms

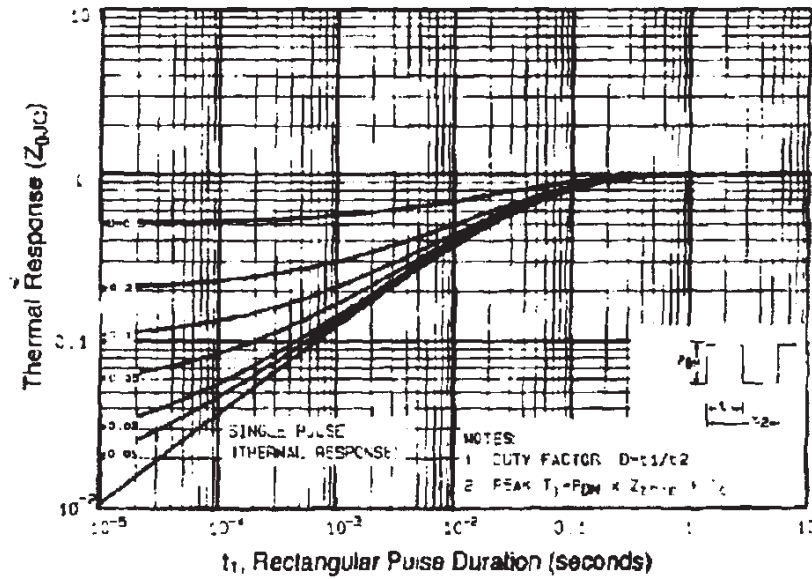


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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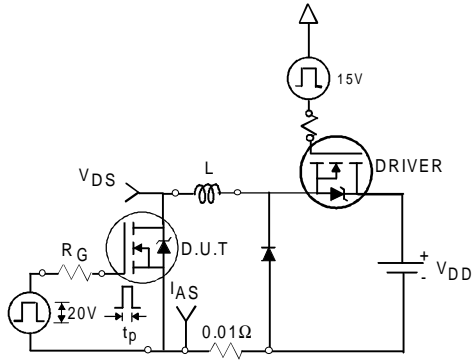


Fig 12a. Unclamped Inductive Test Circuit

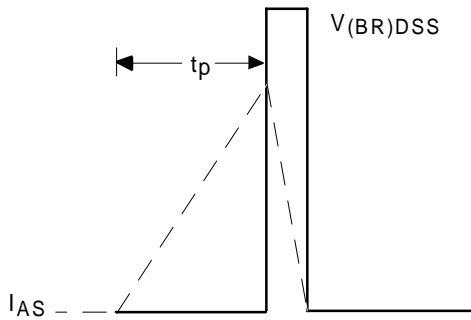


Fig 12b. Unclamped Inductive Waveforms

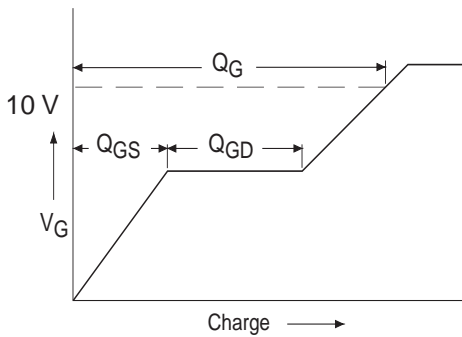


Fig 13a. Basic Gate Charge Waveform

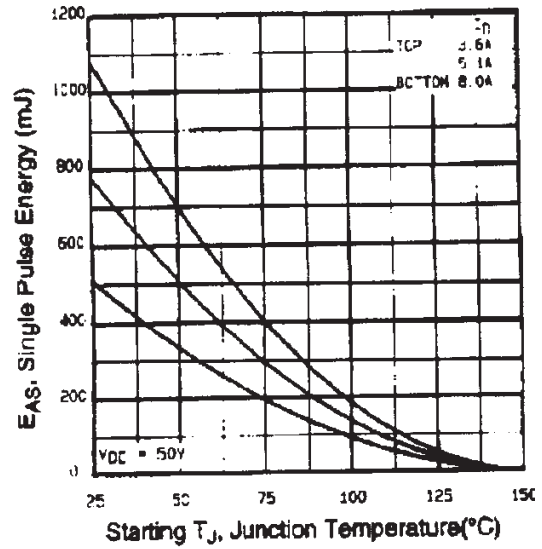


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

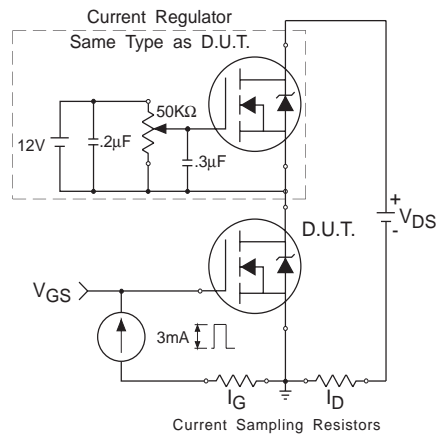
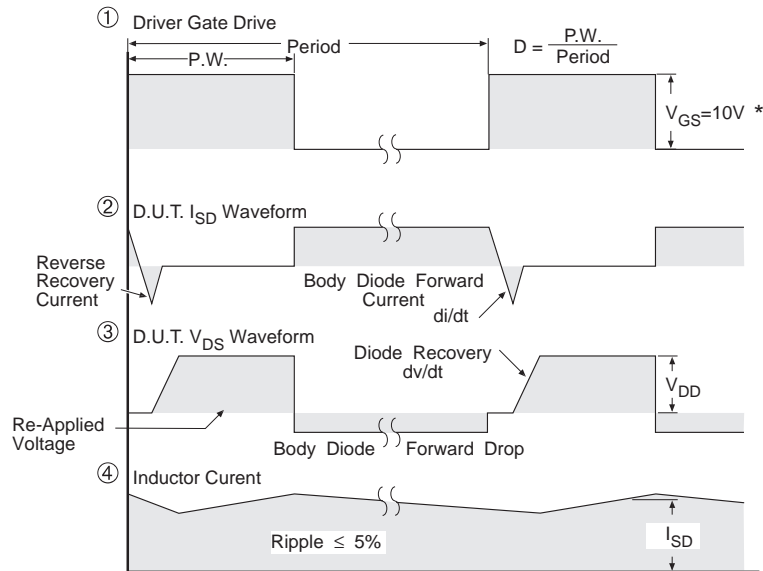
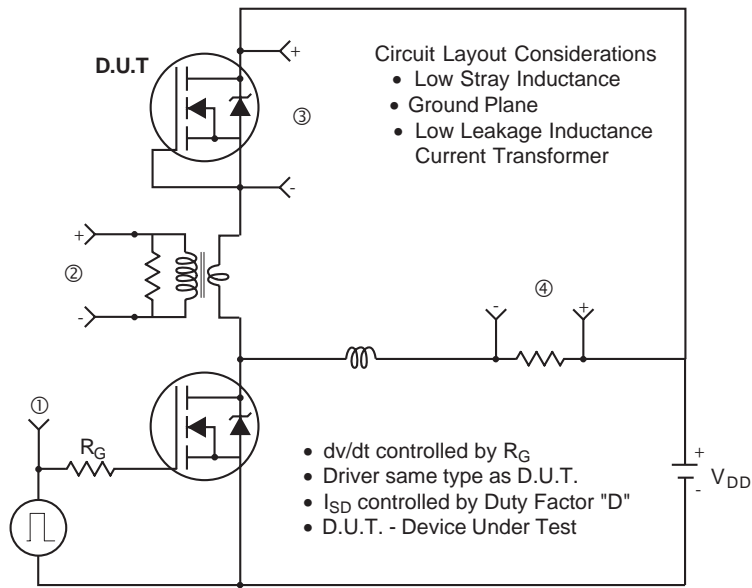


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



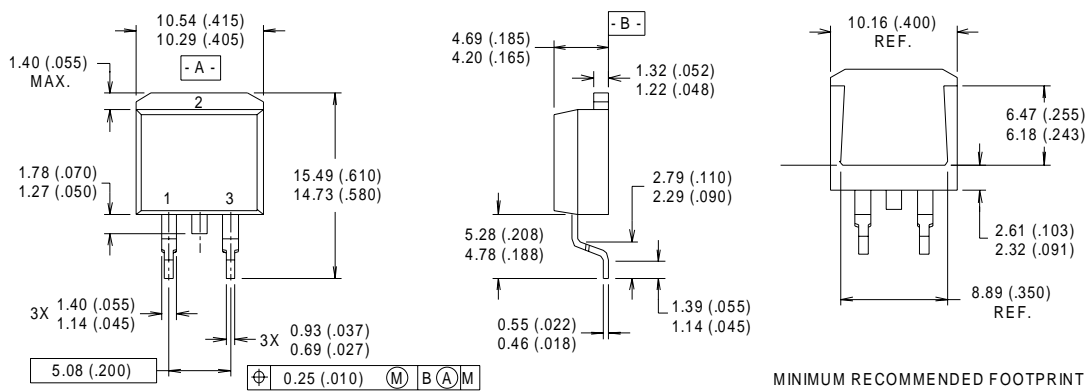
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

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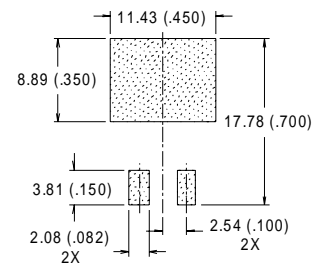
D²Pak Package Outline



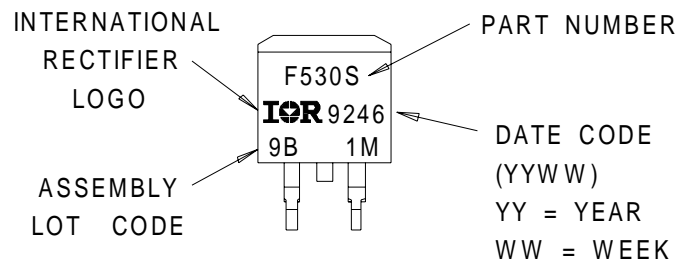
- NOTES:
- 1 DIMENSIONS AFTER SOLDER DIP.
 - 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
 - 3 CONTROLLING DIMENSION : INCH.
 - 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

- LEAD ASSIGNMENTS
- 1 - GATE
 - 2 - DRAIN
 - 3 - SOURCE

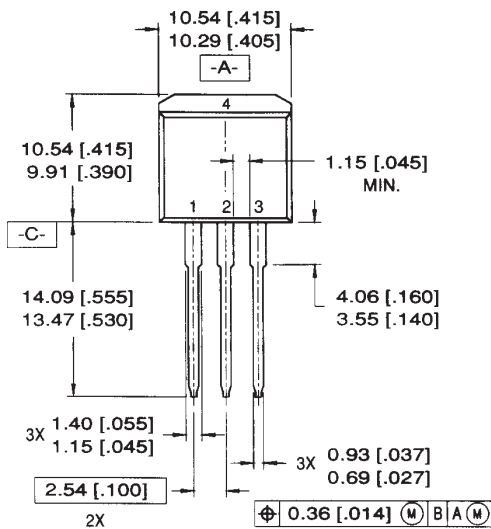
MINIMUM RECOMMENDED FOOTPRINT



D²Pak Part Marking Information



TO-262 Package Outline



LEAD ASSIGNMENTS

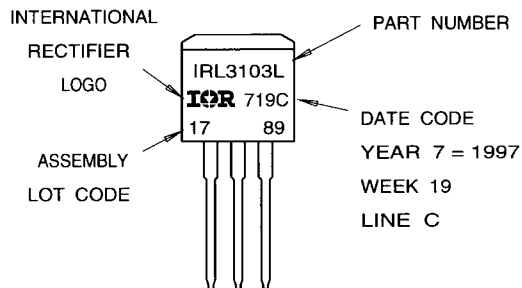
- | | |
|-----------|------------|
| 1 = GATE | 3 = SOURCE |
| 2 = DRAIN | 4 = DRAIN |

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

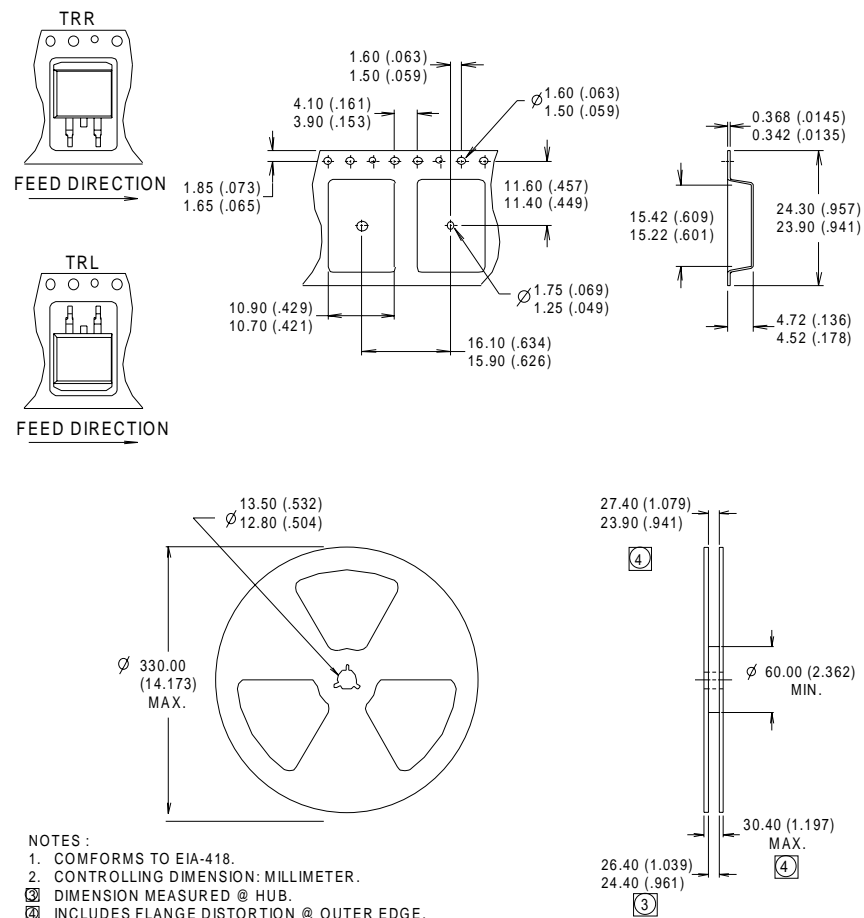
EXAMPLE: THIS IS AN IRL3103L
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"



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D²Pak Tape & Reel Information



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IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200

IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590

IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111

IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086

IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630

IR TAIWAN: 16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936

Data and specifications subject to change without notice. 1/2000

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