

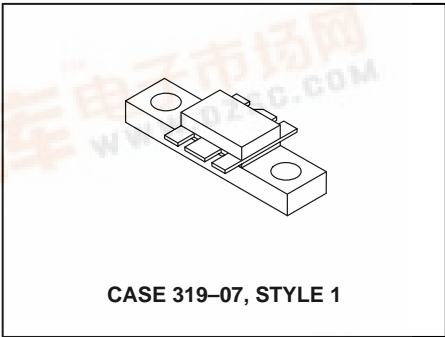
The RF Line NPN Silicon RF Power Transistor

... designed for 12.5 volt UHF large-signal, common-base amplifier applications in industrial and commercial FM equipment operating in the range of 806–960 MHz.

- Specified 12.5 Volt, 870 MHz Characteristics
 - Output Power = 10 Watts
 - Power Gain = 6.0 dB Min
 - Efficiency = 50% Min
- Series Equivalent Large-Signal Characterization
- Internally Matched Input for Broadband Operation
- Tested for Load Mismatch Stress at All Phase Angles with 20:1 VSWR @ 15.5 Volt Supply and 50% RF Overdrive
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivated



**10 W, 870 MHz
 RF POWER
 TRANSISTOR
 NPN SILICON**



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	3.8	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ (1) Derate above 25°C	P_D	40 0.32	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	–65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	3.1	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector–Emitter Breakdown Voltage ($I_C = 50 \text{ mAdc}$, $I_B = 0$)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector–Emitter Breakdown Voltage ($I_C = 50 \text{ mAdc}$, $V_{BE} = 0$)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage ($I_E = 5.0 \text{ mAdc}$, $I_C = 0$)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current ($V_{CB} = 15 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	—	2.0	mAdc

NOTES:

(continued)

- This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.
- Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

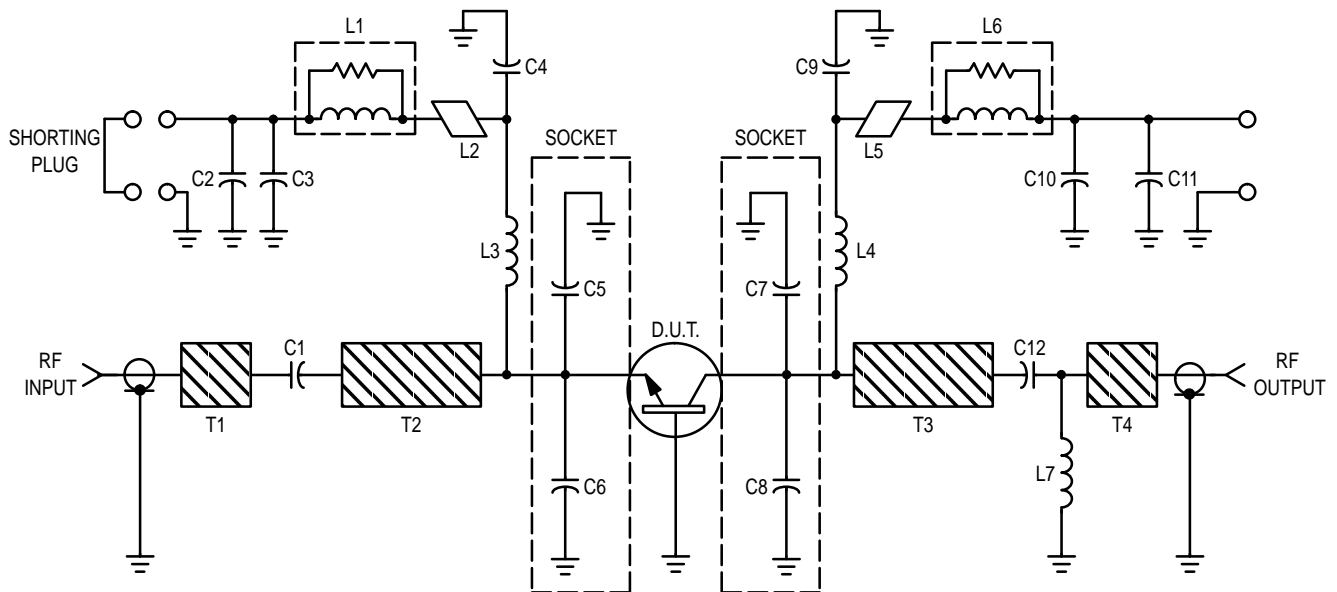


ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain ($I_C = 1.0 \text{ Adc}, V_{CE} = 5.0 \text{ Vdc}$)	h_{FE}	10	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance ($V_{CB} = 12.5 \text{ Vdc}, I_E = 0, f = 1.0 \text{ MHz}$)	C_{ob}	—	24	35	pF
FUNCTIONAL TESTS					
Common-Base Amplifier Power Gain ($P_{out} = 10 \text{ W}, V_{CC} = 12.5 \text{ Vdc}, f = 870 \text{ MHz}$)	G_{PE}	6.0	7.0	—	dB
Collector Efficiency ($P_{out} = 10 \text{ W}, V_{CC} = 12.5 \text{ Vdc}, f = 870 \text{ MHz}$)	η	50	55	—	%
Load Mismatch Stress ($V_{CC} = 15.5 \text{ Vdc}, P_{in} = 3.0 \text{ W}, (3) f = 870 \text{ MHz}, VSWR = 20:1, \text{ all phase angles}$)	—	No Degradation in Output Power			

NOTE:

3. $P_{in} = 150\%$ of the typical input power requirement for 10 W output power @ 12.5 Vdc.



C1, C12 — 50 pF, 100 Mil Chip Capacitor
 C2, C11 — 15 μF , 20 V Tantalum
 C3, C10 — 1000 pF, 350 V UNELCO
 C4, C9 — 91 pF Mini-Underwood
 C5 — 15 pF
 C6 — 15 pF
 C7 — 15 pF
 C8 — 15 pF

L1, L6 — 11 Turns 20 AWG Around 10 Ω 1/2 W Resistor
 L2, L5 — Ferrite Bead
 L3, L4 — 4 Turn 20 AWG 0.2" I.D.
 T1, T4 — $Z_0 = 50 \Omega$
 T2 — $Z_0 = 30 \Omega \ell = \lambda/4 @ 838 \text{ MHz}$
 T3 — $Z_0 = 13.5 \Omega \ell = \lambda/4 @ 838 \text{ MHz}$

L7 — 18 AWG Wire Loop

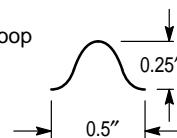


Figure 1. 870 MHz Test Circuit

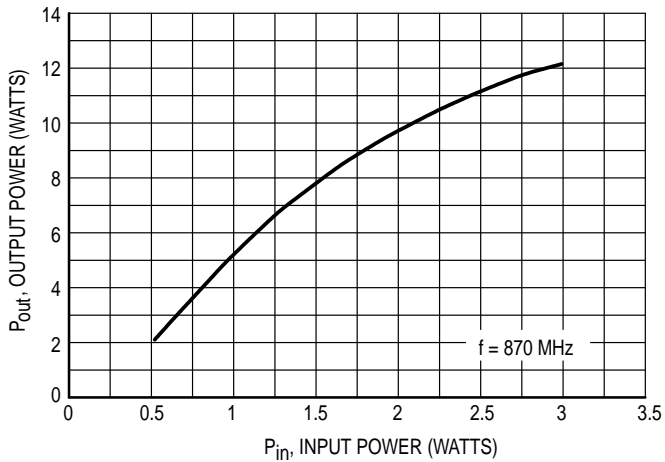


Figure 2. Output Power versus Input Power

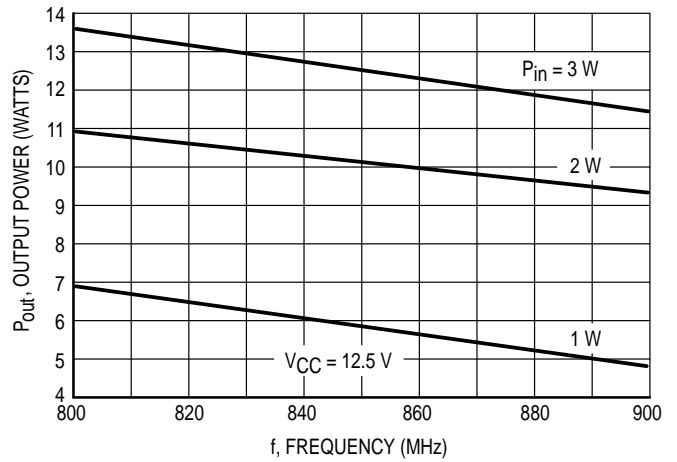


Figure 3. Output Power versus Frequency

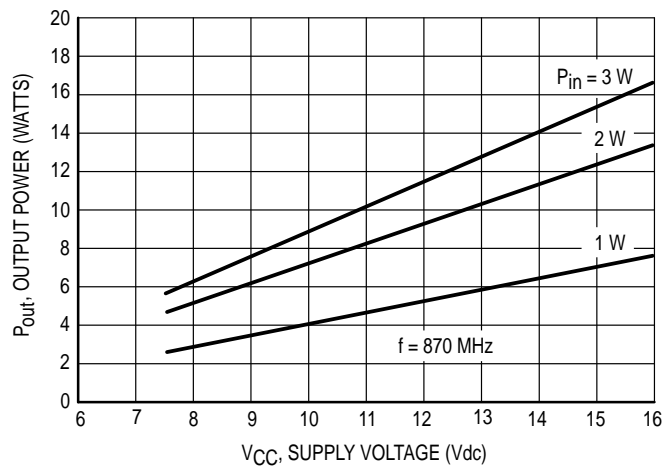
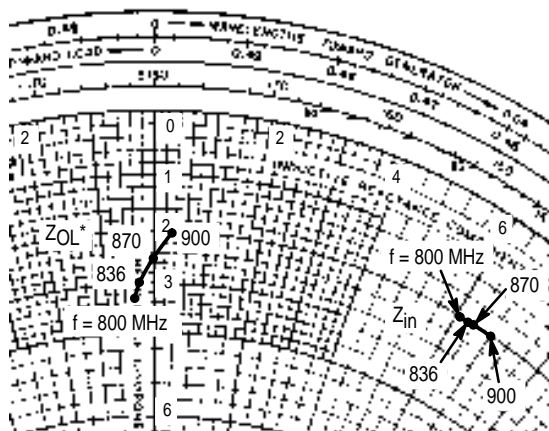


Figure 4. Output Power versus Supply Voltage



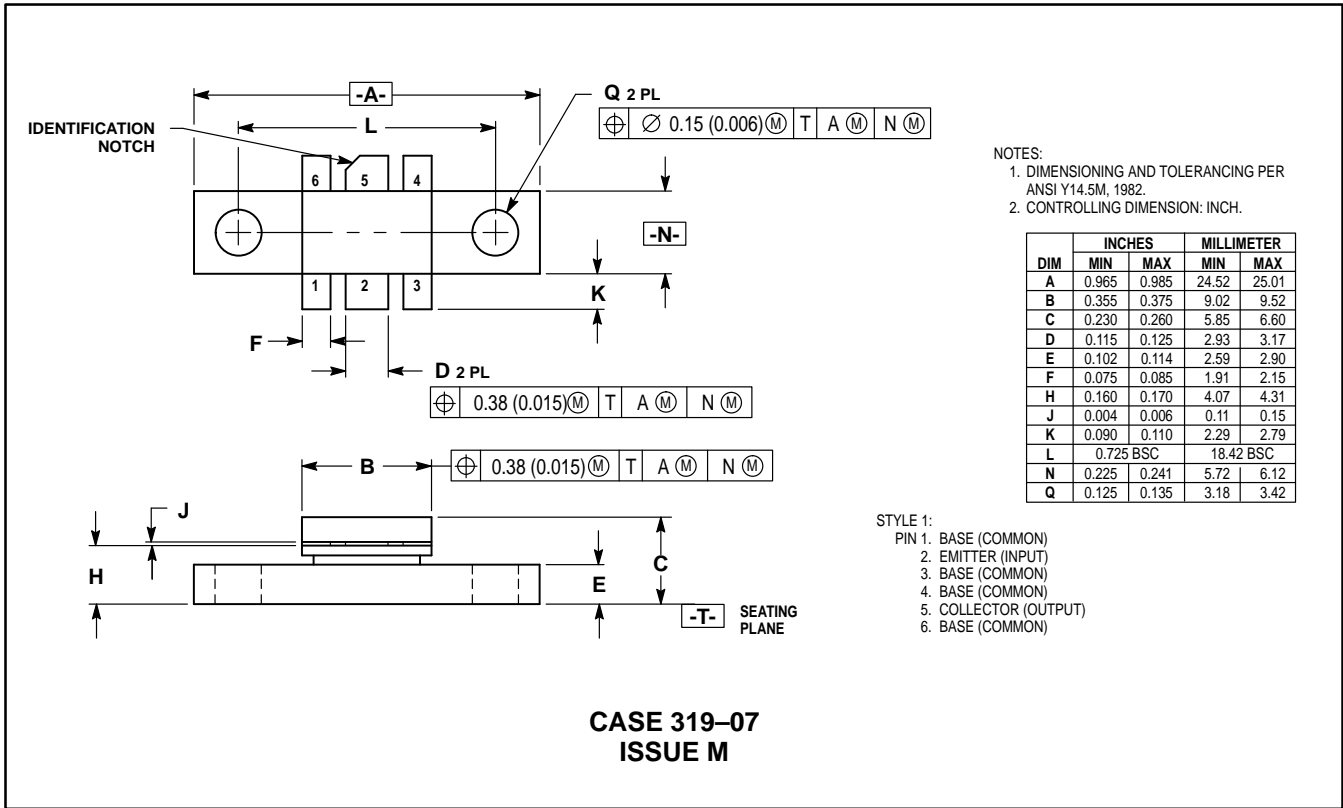
$P_{out} = 10 \text{ W}$, $V_{CC} = 12.5 \text{ Vdc}$

f MHz	Z_{in} Ohms	Z_{OL}^* Ohms
800	$2.0 + j6.1$	$3.3 - j0.4$
836	$2.0 + j6.2$	$3.0 - j0.3$
870	$2.0 + j6.4$	$2.5 + j0.0$
900	$2.0 + j6.8$	$2.0 + j0.3$

Z_{OL}^* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 5. Series Equivalent Input/Output Impedance

PACKAGE DIMENSIONS



NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

STYLE 1:
 PIN 1. BASE (COMMON)
 2. EMITTER (INPUT)
 3. BASE (COMMON)
 4. BASE (COMMON)
 5. COLLECTOR (OUTPUT)
 6. BASE (COMMON)

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