

Radiation Hardened Quad Differential Line Driver

The Intersil HS-26CT31RH is a quad differential line driver designed for digital data transmission over balanced lines and meets the requirements of EIA standard RS-422. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

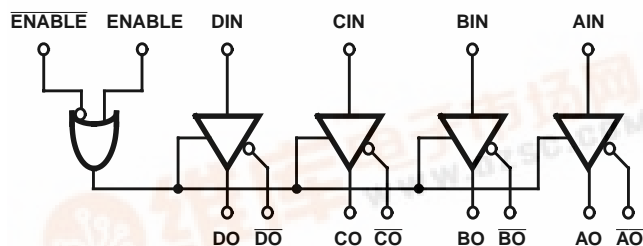
The HS-26CT31RH accepts TTL signal levels and converts them to RS-422 compatible outputs. This circuit uses special outputs that enable the drivers to power down without loading down the bus. Enable and disable pins allow several devices to be connected to the same data source and addressed independently.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95632. A "hot-link" is provided on our homepage for downloading.

<http://www.intersil.com/spacedefense/space.htm>

Logic Diagram

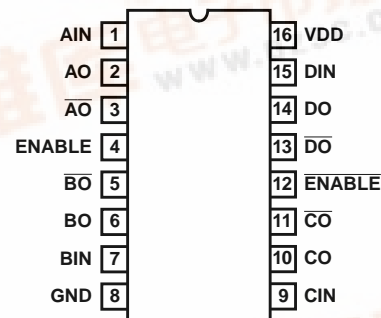


Features

- Electronically Screened to SMD #5962-95632
- QML Qualified Per MIL-PRF-38535 Requirements
- 1.2 Micron Radiation Hardened CMOS
- Total Dose Up to 300kRAD(Si)
- Latchup Free
- EIA RS-422 Compatible Outputs (Except for IOS)
- TTL Compatible Inputs
- High Impedance Outputs when Disabled or Powered Down
- Low Power Dissipation 2.75mW Standby (Max)
- Single 5V Supply
- Low Output Impedance 10Ω or Less
- Full -55°C to +125°C Military Temperature Range

Pinouts

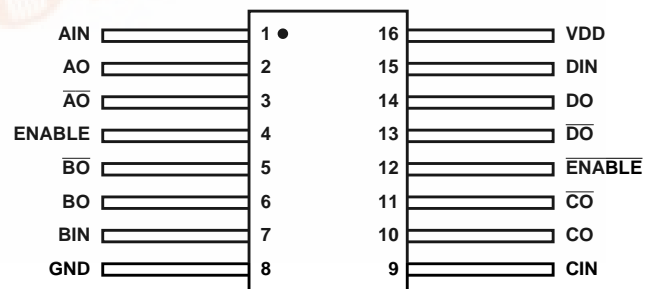
HS1-26CT31RH (SBDIP) CD1P2-T16
TOP VIEW



Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (°C)
5962F9563201QEC	HS1-26CT31RH-8	-55 to 125
5962F9563201QXC	HS9-26CT31RH-8	-55 to 125
5962F9563201V9A	HS0-26CT31RH-Q	25
5962F9563201VEC	HS1-26CT31RH-Q	-55 to 125
5962F9563201VXC	HS9-26CT31RH-Q	-55 to 125
HS1-26CT31RH/PROTO	HS1-26CT31RH/PROTO	-55 to 125
HS9-26CT31RH/PROTO	HS9-26CT31RH/PROTO	-55 to 125

HS9-26CT31RH (FLATPACK) CDFP4-F16
TOP VIEW



HS-26CT31RH

Die Characteristics

DIE DIMENSIONS:

96.5 mils x 195 mils x 21 mils
(2450 x 4950)

INTERFACE MATERIALS:

Glassivation:

Type: PSG (Phosphorus Silicon Glass)
Thickness: $10\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

Metallization:

M1: Mo/TiW
Thickness: 5800\AA
M2: Al/Si/Cu (Top)
Thickness: $10\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

Substrate:

AVLSI1RA

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential (Powered Up):

V_{DD}

ADDITIONAL INFORMATION:

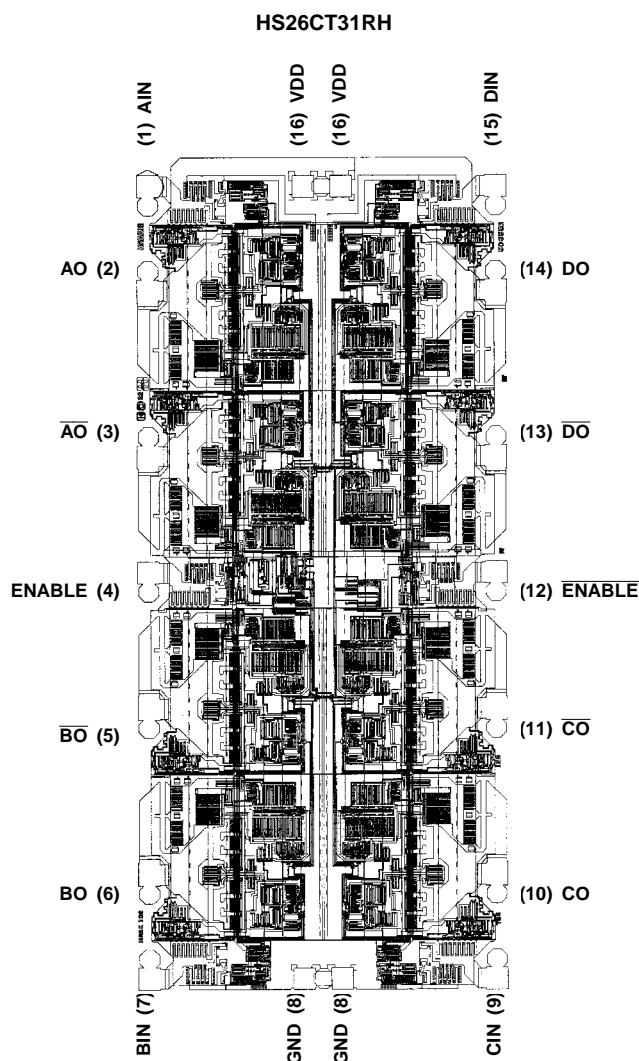
Worst Case Current Density:

$<2.0 \times 10^5 \text{A/cm}^2$

Bond Pad Size:

$110\mu\text{m} \times 100\mu\text{m}$

Metallization Mask Layout



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>