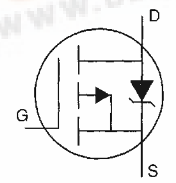
International
IOR Rectifier

IRF9620S

HEXFET® Power MOSFET

- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- P-Channel
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



V_{DSS} = -200V

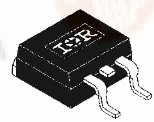
$R_{DS(on)}$ = 1.5Ω

I_D = -3.5A

Description

The HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The SMD-220 is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The SMD-220 is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



SMD-220

DATA SHEETS

Absolute Maximum Ratings

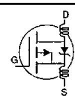
	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ -10 V	-3.5	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ -10 V	-2.0	
I_{DM}	Pulsed Drain Current ①	-14	
P_D @ T_C = 25°C	Power Dissipation	40	W
P_D @ T_A = 25°C	Power Dissipation (PCB Mount)**	3.0	
	Linear Derating Factor	0.32	W/°C
	Linear Derating Factor (PCB Mount)**	0.025	
V_{GS}	Gate-to-Source Voltage	±20	V
I_{LM}	Inductive Current, Clamp	-14	A
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

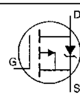
	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	3.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	—	40	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

** When mounted on 1" square PCB (FR-4 or G-10 Material).

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-200	—	—	V	V_{GS}=0V, I_D=-250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.22	—	V/°C	Reference to 25°C, I_D=-1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.5	Ω	V_{GS}=-10V, I_D=-1.5A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS}=V_{GS}, I_D=-250µA
g_{fs}	Forward Transconductance	1.0	—	—	S	V_{DS}=-50V, I_D=-1.5A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	-100	µA	V_{DS}=-200V, V_{GS}=0V
		—	—	-500		V_{DS}=-160V, V_{GS}=0V, T_J=125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V_{GS}=-20V
	Gate-to-Source Reverse Leakage	—	—	100		V_{GS}=20V
Q_g	Total Gate Charge	—	—	22	nC	I_D=-4.0A
Q_{gs}	Gate-to-Source Charge	—	—	12		V_{DS}=-160V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	10		V_{GS}=-10V See Fig. 6 and 12 ④
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	V_{DD}=-100V
t_r	Rise Time	—	25	—		I_D=-1.5A
$t_{d(off)}$	Turn-Off Delay Time	—	20	—		R_G=50Ω
t_f	Fall Time	—	15	—		R_D=67Ω See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	350	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	100	—		V_{DS}=-25V
C_{rss}	Reverse Transfer Capacitance	—	30	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-3.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-14		
V_{SD}	Diode Forward Voltage	—	—	-7.0	V	T_J=25°C, I_S=-3.5A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	300	450	ns	T_J=25°C, I_F=-3.5A
Q_{rr}	Reverse Recovery Charge	—	1.9	2.9	µC	di/dt=100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② Not Applicable

③ I_{SD}≤-3.5A, di/dt≤95A/µs, V_{DD}≤$V_{(BR)DSS}$, T_J≤150°C

④ Pulse width ≤ 300 µs; duty cycle ≤2%.

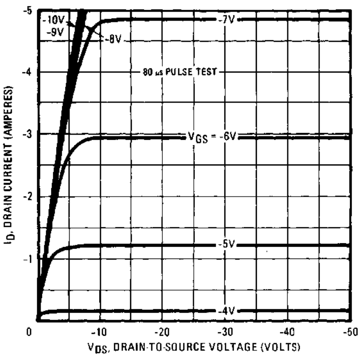


Fig. 1 — Typical Output Characteristics

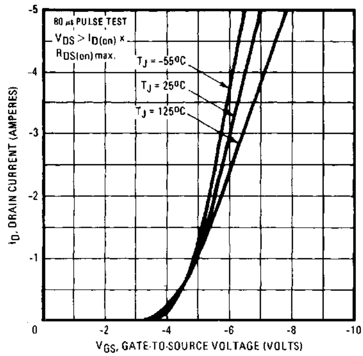


Fig. 2 — Typical Transfer Characteristics

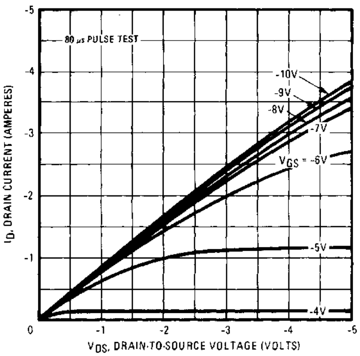


Fig. 3 — Typical Saturation Characteristics

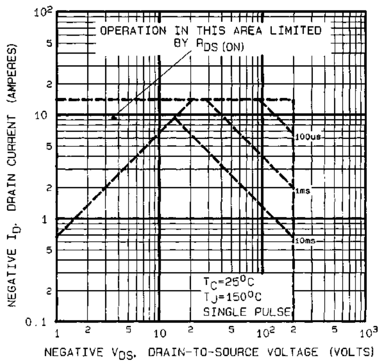


Fig. 4 — Maximum Safe Operating Area

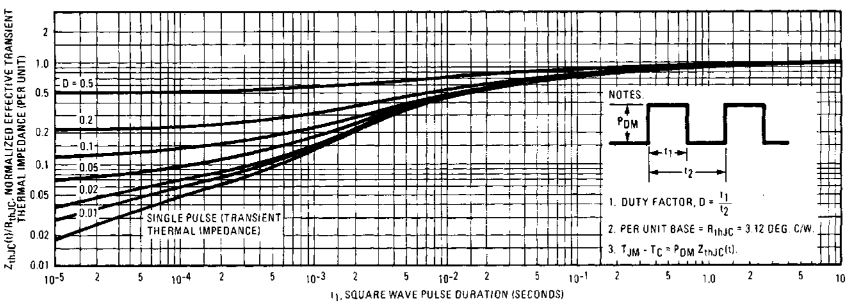


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

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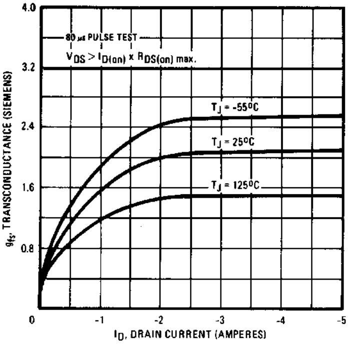

Fig. 6 — Typical Transconductance Vs. Drain Current

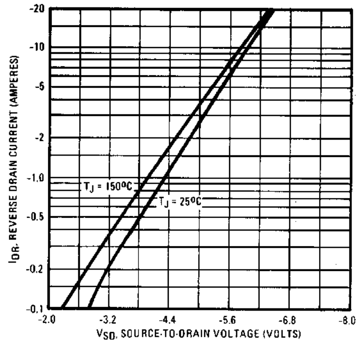

Fig. 7 — Typical Source-Drain Diode Forward Voltage

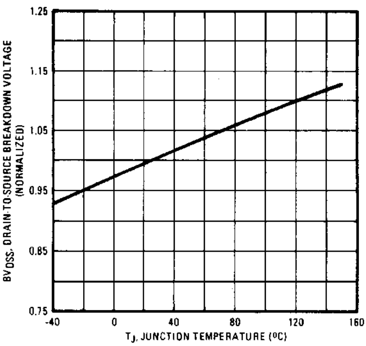

Fig. 8 — Breakdown Voltage Vs. Temperature

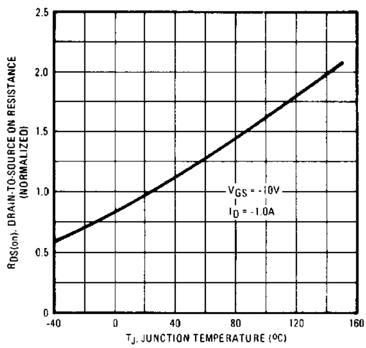

Fig. 9 — Normalized On-Resistance Vs. Temperature

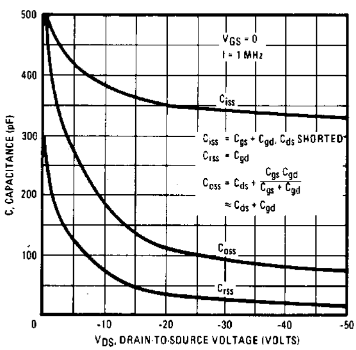

Fig. 10 — Typical Capacitance Vs.
Drain-to-Source Voltage

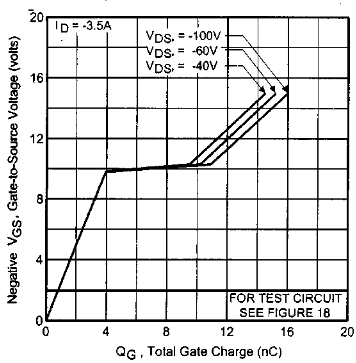

Fig. 11 — Typical Gate Charge Vs.
Gate-to-Source Voltage

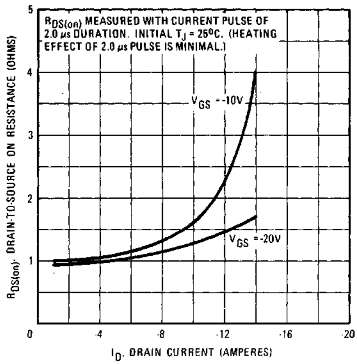

Fig. 12 — Typical On-Resistance Vs. Drain Current

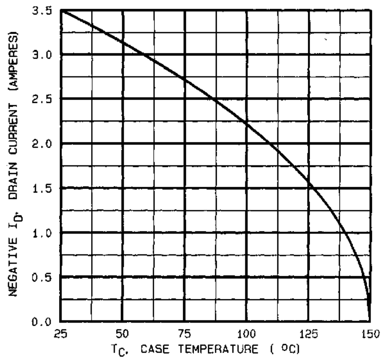

Fig. 13 — Maximum Drain Current Vs. Case Temperature

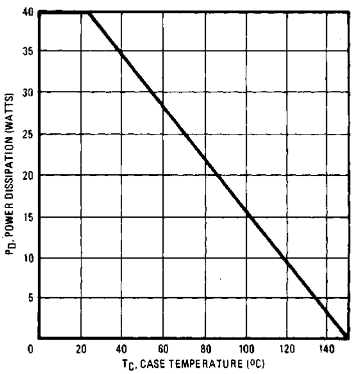

Fig. 14 — Power Vs. Temperature Derating Curve

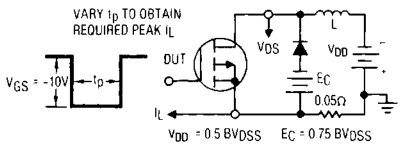

Fig. 15 — Clamped Inductive Test Circuit

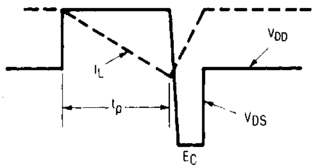

Fig. 16 — Clamped Inductive Waveforms

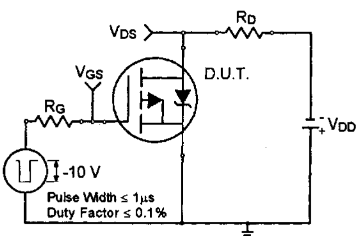

Fig. 17a — Switching Time Test Circuit

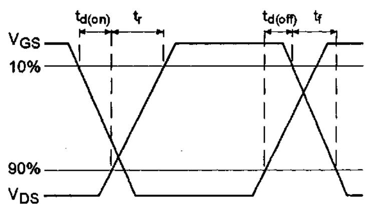

Fig. 17b — Switching Time Waveforms

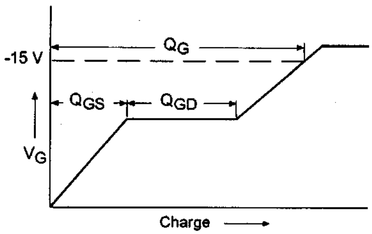

Fig. 18a — Basic Gate Charge Waveform

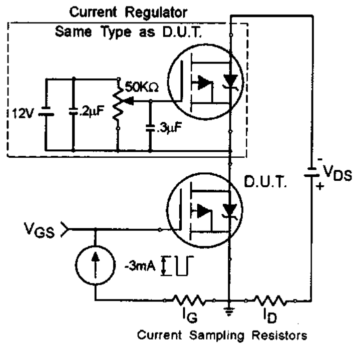

Fig. 18b — Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1506

Appendix B: Package Outline Mechanical Drawing – See page 1507

Appendix C: Part Marking Information – See page 1515

Appendix D: Tape & Reel Information – See page 1519