FA3686V

CMOS IC
For Switching Power Supply Control

■ Description

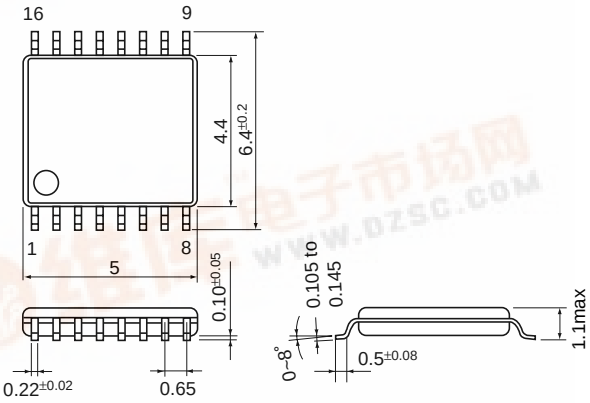
FA3686V is a PWM type DC-to-DC converter control IC with 2ch outputs that can directly drive power MOSFETs. CMOS devices with high breakdown voltage are used in this IC and low power consumption is achieved. This IC is suitable for very small DC-to-DC converters because of their small and thin package (1.1mm max.), and high frequency operation (to 1.5MHz). This IC contains built-in an error amplifier for series regulators, therefore, this IC is suitable for the 3ch power supply with a 2ch DC-to-DC converter and a 1ch series regulator.

■ Features

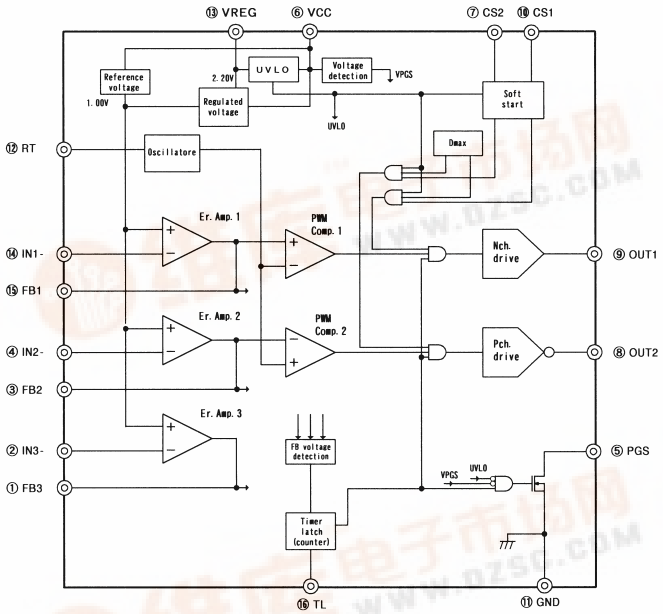
- Wide range of supply voltage: VCC=2.5 to 20V
- MOSFET direct driving
- Low operating current consumption by CMOS process: 3.0mA (typ.)
- 2ch PWM control IC
- High frequency operation: 300kHz to 1.5MHz
- Simple setting of operation frequency by timing resistor
- Built-in error amplifier for series regulator
- Soft start function on each channel (1ch, 2ch only)
- Maximum output duty cycle: 85% (typ.), at 500kHz
- Built-in under voltage lockout
- High accuracy reference voltage: VREF: 1.00V±1%, VREG: 2.20V±1%
- Timer latch for short-circuit protection with counter
- PGS pin for a power supply fault signal
- Thin and small package: TSSOP-16

■ Dimensions, mm

● TSSOP-16



■ Block diagram



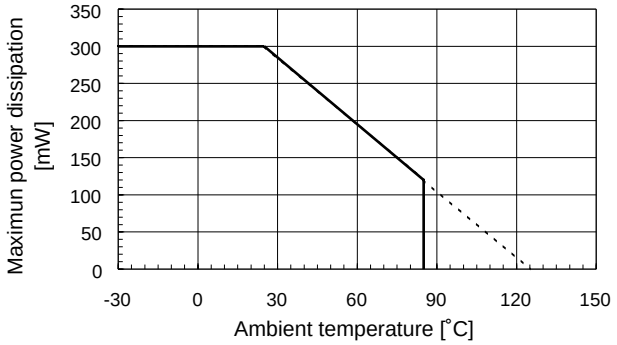
Pin No.	Pin symbol	Description
1	FB3	Ch.3 output of error amplifier
2	IN3-	Ch.3 inverting input to error amplifier
3	FB2	Ch.2 output of error amplifier
4	IN2-	Ch.2 inverting input to error amplifier
5	PGS	PGS signal output
6	VCC	Power supply
7	CS2	Soft start for Ch.2
8	OUT2	Ch.2 output
9	OUT1	Ch.1 output
10	CS1	Soft start for Ch.1
11	GND	Ground
12	RT	Oscillator timing resistor
13	VREG	Regulated voltage output
14	IN1-	Ch.1 inverting input to error amplifier
15	FB1	Ch.1 output of error amplifier
16	TL	Timer latched short circuit protection

■ Absolute maximum ratings

Item		Symbol	Rating	Unit
Power supply voltage		V_{CC}	20	V
PGS pin voltage		V_{PGS}	20	V
FB1, IN1–, FB2, IN2–, FB3, IN3– pin voltage		V_{EA_IN}	–0.3 to 5.0	V
CS1, CS2, RT, TL, VREG pin voltage		V_{CTR_IN}	–0.3 to 5.0	V
OUT1/2	OUT pin source current	I_{OUT-}	–400 (peak)	mA
	OUT pin sink current	I_{OUT+}	150 (peak)	mA
OUT1/2	OUT pin source current	I_{OUT-}	–50 (continuous)	mA
	OUT pin sink current	I_{OUT+}	50 (continuous)	mA
Power dissipation *		P_d	300 (Ta≦25˚C)	mW
Operating junction temperature		T_J	+125	˚C
Operating ambient temperature		T_{OPR}	–30 to +85	˚C
Storage temperature		T_{STG}	–40 to +125	˚C

* Derating factor Ta≧25˚C: 3mW/˚C

Maximum power dissipation curve



■ Recommended operating conditions

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}		2.5		18	V
CS1, CS2, TL pin voltage	V_{CTR_IN}		0.0		2.5	V
IN1–, IN2–, IN3– pin voltage	V_{EA_IN}		0.0		2.5	V
Oscillation frequency	f_{OSC}		300	500	1500	kHz
VREG pin capacitance	C_{REG}	Vcc<10V	0.1	1.0	4.7	µF
		10V≦Vcc<18V	0.47	1.0	4.7	µF
VREG pin current	I_{REG}				1.0	mA
VCC pin capacitance	C_{VCC}		1.0			µF
CS1 pin capacitance	C_{CS1}	Between CS1 and GND	0.01			µF
CS2 pin capacitance	C_{CS2}	Between CS2 and VREG	0.01			µF

■ Electrical characteristics (V_{CC}=3.3V, C_{REG}=1.0µF, R_T=12kΩ, Ta=+25˚C)

Regulated voltage for internal control blocks (VREG pin)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Regulated voltage	V_{REG}		2.178	2.200	2.222	V
Line regulation	V_{REG_LINE}	V_{CC}=2.5 to 18V		±5	±15	mV
Load regulation	V_{REG_LOAD}	I_{REG}=0 to 1mA	–5	–1		mV
Variation with temperature	V_{REG_TC}	Ta=–30 to +85˚C		±0.5		%

Oscillator section (RT pin)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC}		435	500	565	kHz
Line regulation	f_{OSC_LINE}	V_{CC}=2.5 to 18V		±1	±5	%
Variation with temperature	f_{OSC_TC1}	Ta=–30 to +85˚C		±3		%

Error amplifier section (IN1–, FB1, IN2–, FB2, IN3–, FB3 pin)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Reference voltage (CH.1)	V_{REF1}	*1	0.99	1.00	1.01	V
Reference voltage (CH.2)	V_{REF2}	*2	0.98	1.00	1.02	V
Reference voltage (CH.3)	V_{REF3}	*3	0.98	1.00	1.02	V
V_{REF} Line regulation	V_{REF_LINE}	V_{CC}=2.5 to 18V		±2	±5	mV
V_{REF} Variation with temperature	V_{REF_TC1}	Ta=–30 to +85˚C		±0.5		%
Input bias current	I_{IN-}	V_{INx-}=0.0 to 2.5V *4		0.0		mA
Open loop gain	A_{VO}			70		dB
Unity gain bandwidth	f_T			1.5		MHz
Output current (sink)	I_{SIFB}	V_{FBx}=0.5V, V_{INx-}=V_{REG} *4	2.3	3.5	4.7	mA
Output current (source)	I_{SOFB}	V_{FBx}=V_{REG}–0.5V, V_{INx-}=0V *4	–360	–270	–180	µA

*1 The FB1 voltage is measured under the condition that IN1- pin and FB1 pin are shorted. The input offset voltage of the error amplifier is included.
*2 The FB2 voltage is measured under the condition that IN2- pin and FB2 pin are shorted. The input offset voltage of the error amplifier is included.
*3 The FB3 voltage is measured under the condition that IN3- pin and FB3 pin are shorted. The input offset voltage of the error amplifier is included.
*4 The “x” of INx- and FBx refers to 1 to 3.

Soft start section (CS1, CS2 pin)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Threshold voltage (CS1)	V_{CS1D0}	Duty cycle=0%, V_{FB1}=1.4V		0.82		V
	V_{CS1D20}	Duty cycle=20%, V_{FB1}=1.4V	0.89	0.925	0.96	V
	V_{CS1D80}	Duty cycle=80%, V_{FB1}=1.4V	1.25	1.285	1.32	V
Threshold voltage (CS2)	V_{CS2D0}	Duty cycle=0%, V_{FB2}=0.7V		1.33		V
	V_{CS2D20}	Duty cycle=20%, V_{FB2}=0.7V	1.20	1.235	1.27	V
	V_{CS2D80}	Duty cycle=80%, V_{FB2}=0.7V	0.84	0.875	0.91	V
Charge current of CS2 (source)	I_{CS1}	V_{CS1}=0.5V	–2.	–2.0	–1.5	µA
Charge current of CS2 (sink)	I_{CS2}	V_{CS2}=V_{REG}–0.5V	1.5	2.0	2.4	µA

Pulse width modulation (PWM) section (FB1, FB2 pin)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Max. duty cycle of OUT1	D_{MAX1}	f_{OSC}=300kHz		87		%
		R_T=12kΩ (f_{OSC}≒500kHz)	80	85	90	%
		f_{OSC}=1.5MHz		78		%
Max. duty cycle of OUT2	D_{MAX2}	f_{OSC}=300kHz		88		%
		R_T=12k (f_{OSC}≒500kHz)	80	85	90	%
		f_{OSC}=1.5MHz		73		%
Threshold voltage of FB1	V_{FB1D0}	Duty cycle=0%		0.82		V
	V_{FB1D20}	Duty cycle=20%		0.925		V
	V_{FB1D80}	Duty cycle=80%		1.285		V
Threshold voltage of FB2	V_{FB2D0}	Duty cycle=0%		1.33		V
	V_{FB2D20}	Duty cycle=20%		1.235		V
	V_{FB2D80}	Duty cycle=80%		0.875		V

Timer latch protection section (TL pin)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Threshold voltage of FB1	$V_{THFB1TL}$	*1	1.5		2.0	V
Threshold voltage of FB2	$V_{THFB2TL}$	*2	0.2		0.6	V
Threshold voltage of FB3	$V_{THFB3TL}$	*1	1.5		2.0	V
Threshold voltage of CS1	$V_{VTHCS1TL}$	*3	0.2		0.6	V
Threshold voltage of CS2	$V_{VTHCS2TL}$	*4	1.5		2.0	V
TL pin voltage for counting 16th stage	V_{TL16}		0		0.2	V
TL pin voltage counting 17th stage	V_{TL17}		V_{REG}–0.2		V_{REG}	V

*1 The latched mode operates when the voltage of FB1 or FB3 exceeds the threshold voltage as shown in the table.
*2 The latched mode operates when the FB2 voltage falls below the threshold voltage as shown in the table.
*3 The timer latch of FB1 is disabled when the CS1 voltage is below the threshold voltage as shown in the table.
*4 The timer latch of FB2 is disabled when the CS2 voltage is above the threshold voltage as shown in the table.

Under voltage lockout circuit section (VCC pin)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
ON threshold voltage of VCC	V_{UVLO}		2.0	2.2	2.35	V
Hysteresis voltage	$\triangle V_{UVLO}$			0.1		V

PGS section (VCC, PGS pin)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Threshold voltage of VCC	V_{PGS}	V_{CC} decreasing	2.15	2.25	2.35	V
Hysteresis voltage	$\triangle V_{PGS}$	V_{CC} increasing		0.10		V
VPGS variation with temperature	V_{PGS_TC1}	Ta=–30 to +85˚C		±1		%
On resistance	R_{PGS}	V_{CC}=2.2V, I_{PGS}=10mA		50	100	Ω

Output section (OUT1, OUT2 pin)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
High side on resistance of OUT1/2	R_{ONHI}	I_{OUTx}=-50mA *		10	20	Ω
		I_{OUTx}=-50mA, V_{CC}=5V *		9		Ω
		I_{OUTx}=-50mA, V_{CC}=15V *		8		Ω
Low side on resistance of OUT1/2	R_{ONLO}	I_{OUTx}=50mA *		5	10	Ω
		I_{OUTx}=50mA, V_{CC}=5V *		5		Ω
		I_{OUTx}=50mA, V_{CC}=15V *		5		Ω
Rise time of OUT1/2	t_{RISE}	C_L=1000pF		25		ns
Fall time of OUT1/2	t_{FALL}	C_L=1000pF		40		ns

* The “x” of OUTx refers to 1, 2.

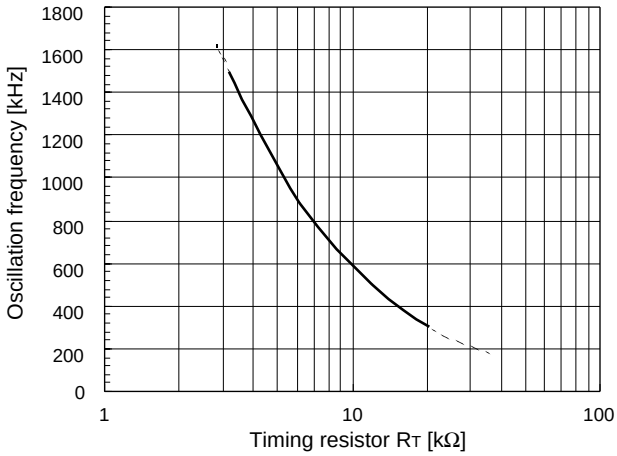
Overall section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Supply current	I_{CCA}	Ch.1, Ch.2 operating mode		3.0	4.0	mA
	I_{CCA1}	Ch.1, Ch.2 off mode		2.5		mA
	I_{CCA2}	Ch.1, Ch.2 operating mode, V_{CC}=18V		3.5		mA
	I_{CCA3}	Latch mode		2.5		mA

■ Characteristic curves

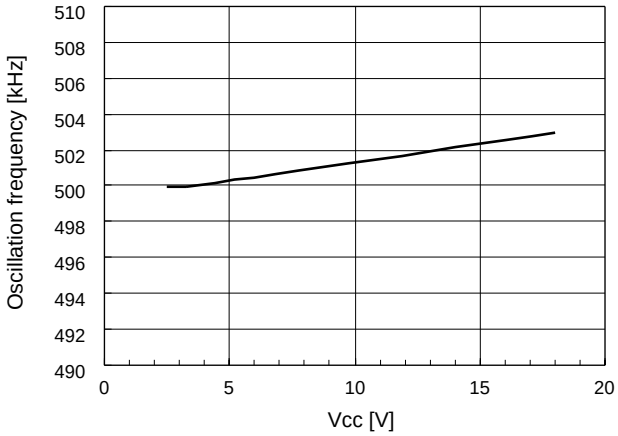
Oscillation frequency vs. timing resistor

V_{CC}=3.3V, Ta=25˚C



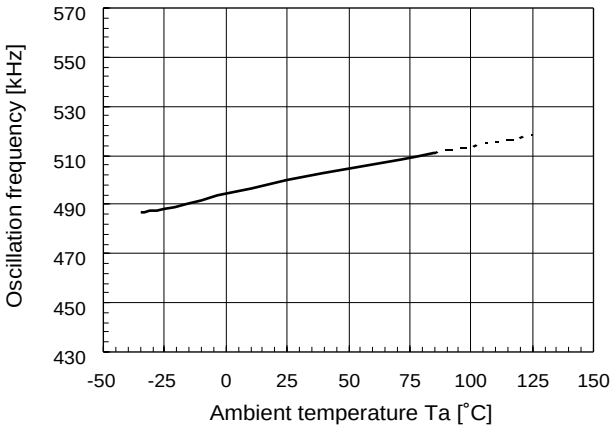
Oscillation frequency vs. supply voltage Vcc

Ta=25˚C, R_T=12kΩ (f_{OSC}=500kHz)



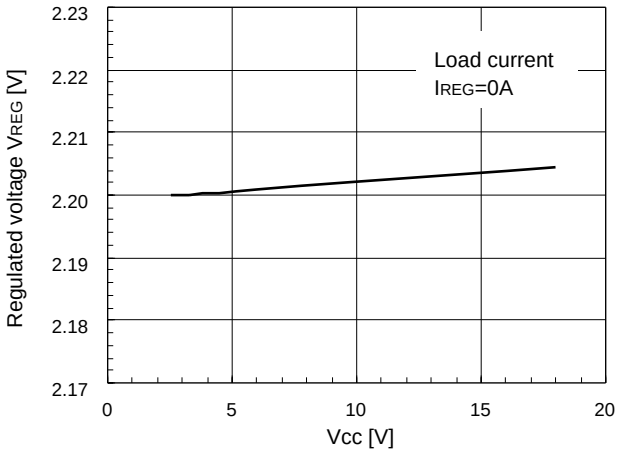
Oscillation frequency vs. ambient temperature

V_{CC}=3.3V, R_T=12kΩ (f_{OSC}=500kHz)



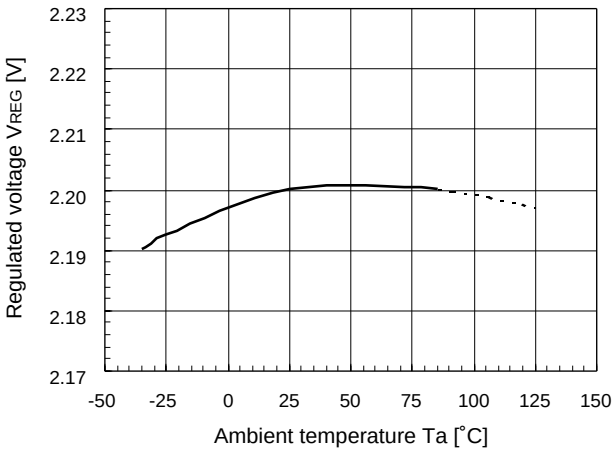
Regulated voltage vs. supply voltage Vcc

Ta=25˚C, R_T=12kΩ (f_{OSC}=500kHz)



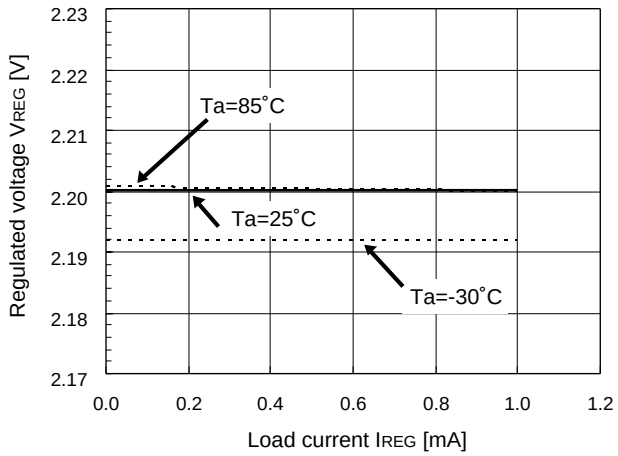
Regulated voltage vs. ambient temperature

V_{CC}=3.3V, R_T=12kΩ (f_{OSC}=500kHz)



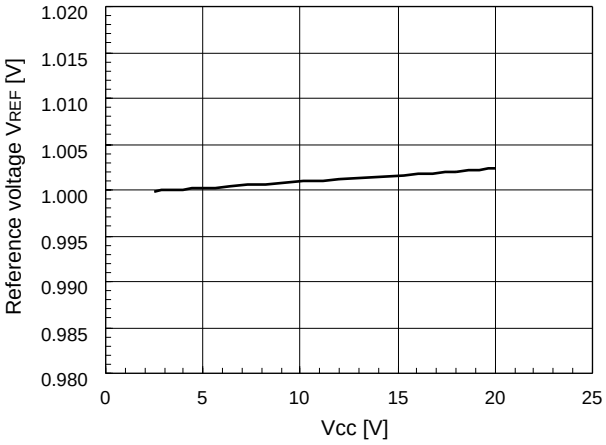
Regulated voltage vs. load current

V_{CC}=3.3V, R_T=12kΩ (f_{OSC}=500kHz)



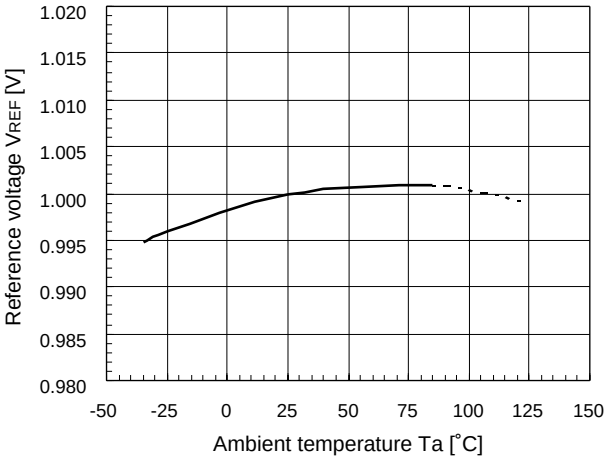
Reference voltage vs. supply voltage Vcc

Ta=25˚C, RT=12kΩ (fosc=500kHz)



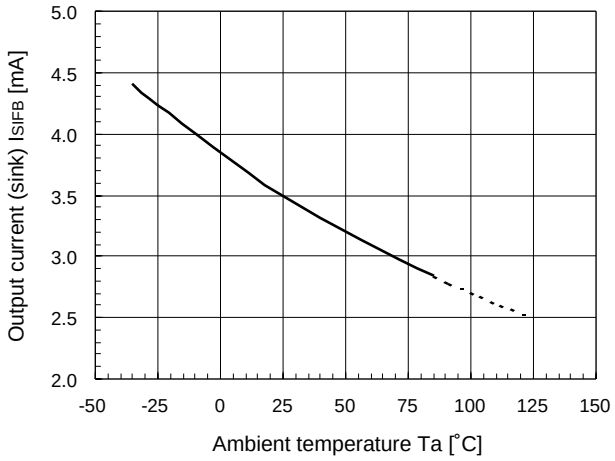
Reference voltage vs. ambient temperature

Vcc=3.3V, RT=12kΩ (fosc=500kHz)



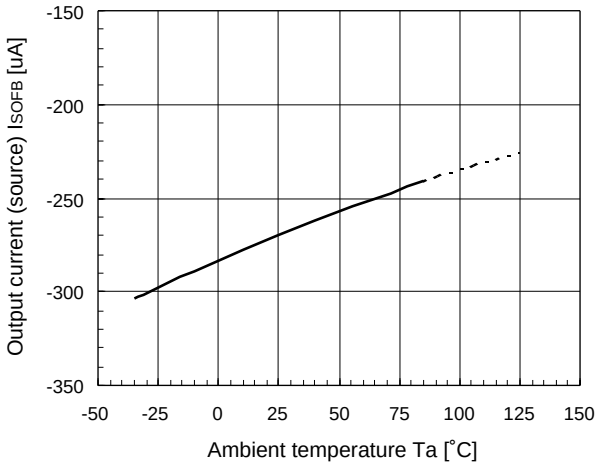
Error amp. output current (sink) vs. ambient temperature

Vcc=3.3V, RT=12kΩ (fosc=500kHz)



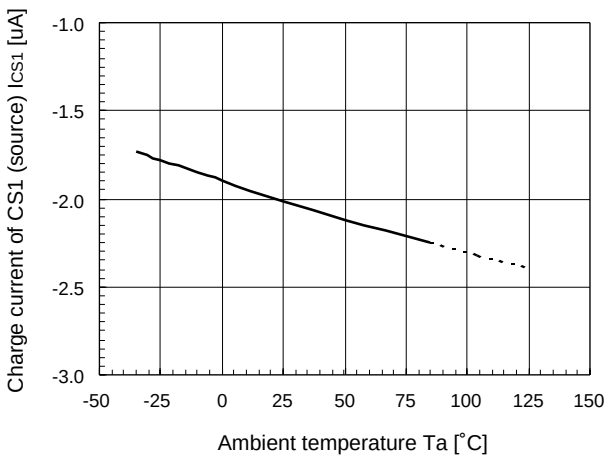
Error amp. output current (source) vs. ambient temperarure

Vcc=3.3V, RT=12kΩ (fosc=500kHz)



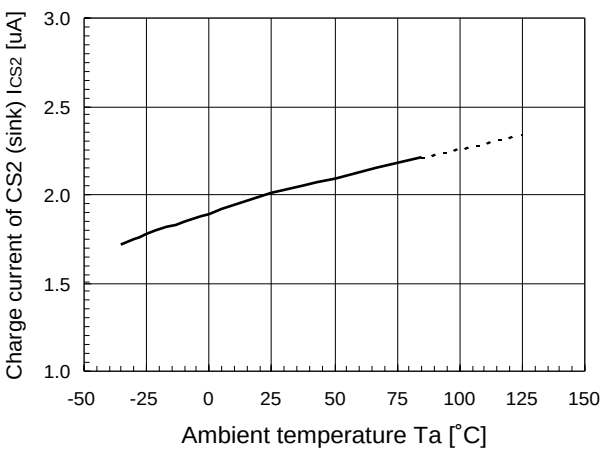
Charge current of CS1 (source) vs. ambient temperature

Vcc=3.3V, RT=12kΩ (fosc=500kHz)

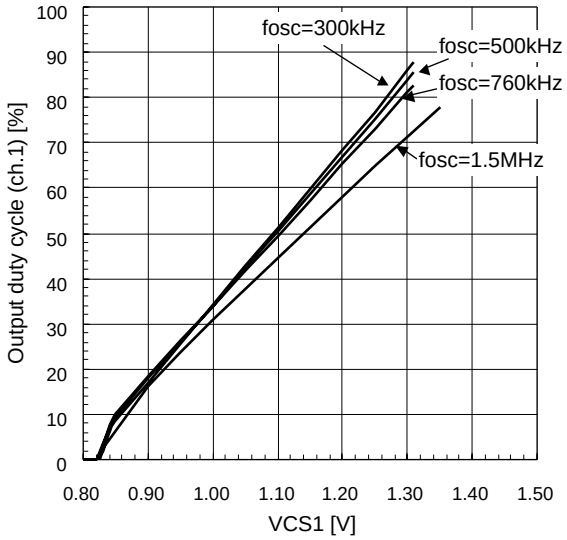


Charge current of CS2 (sink) vs. ambient temperature

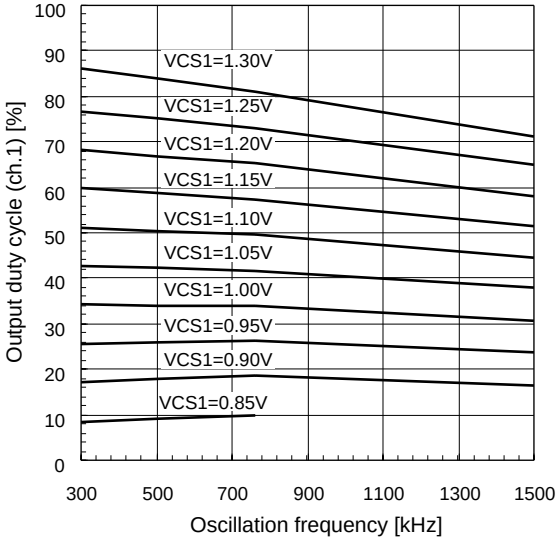
Vcc=3.3V, RT=12kΩ (fosc=500kHz)



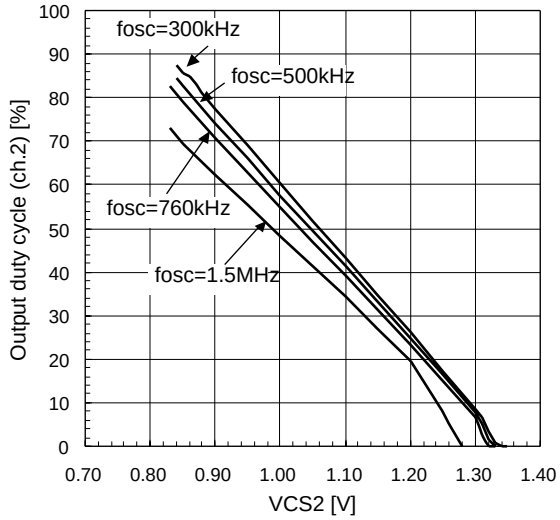
Output duty cycle vs. CS voltage (ch. 1)
VCC=3.3V, Ta=25˚C



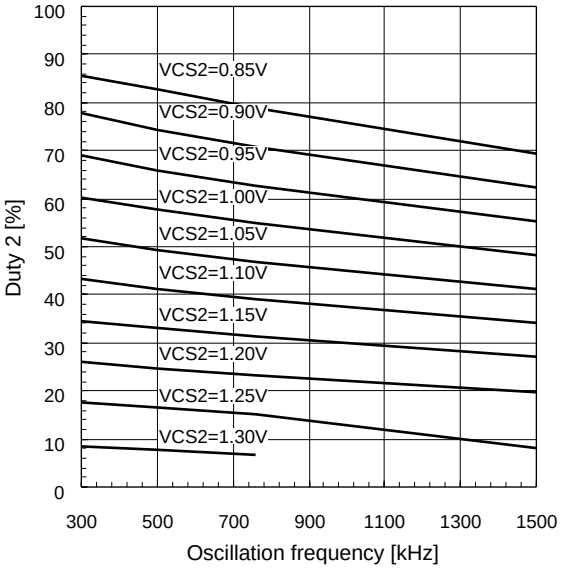
Output duty cycle vs. oscillation frequency (ch. 1)
VCC=3.3V, Ta=25˚C



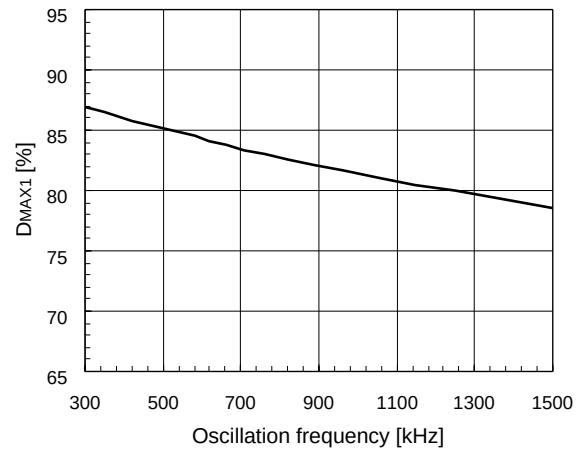
Output duty cycle vs. CS voltage (ch. 2)
VCC=3.3V, Ta=25˚C



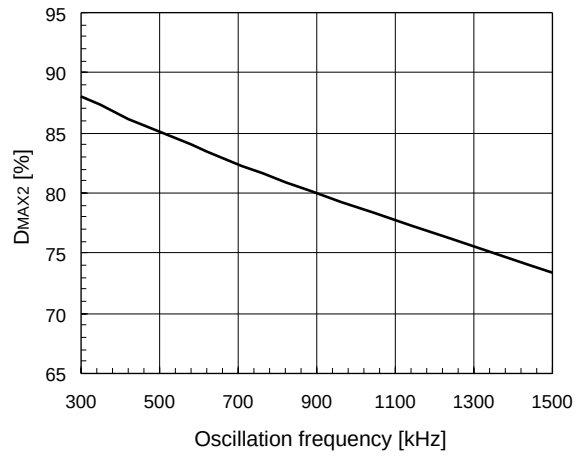
Output duty cycle vs. oscillation frequency (ch. 2)
VCC=3.3V, Ta=25˚C



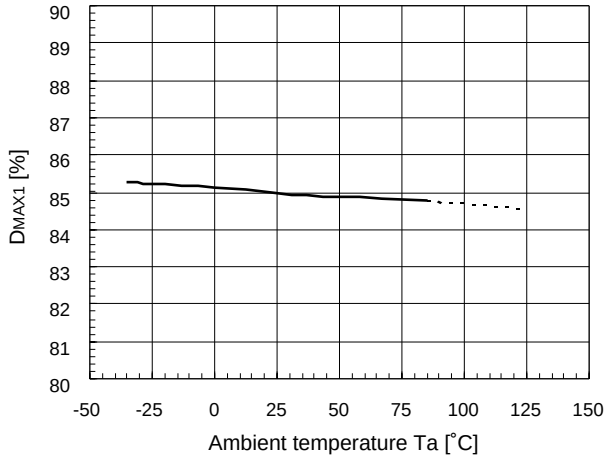
Maximum duty cycle vs. oscillation frequency (ch. 1)
VCC=3.3V, Ta=25˚C



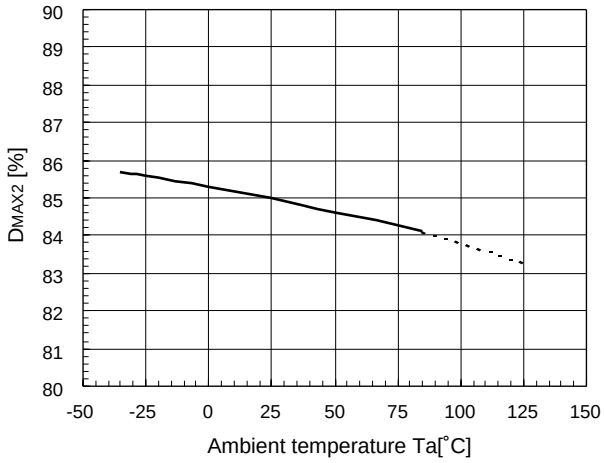
Maximum duty cycle vs. oscillation frequency (ch. 2)
VCC=3.3V, Ta=25˚C



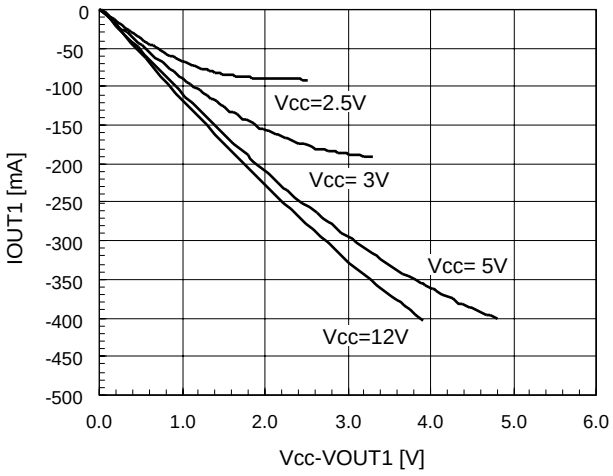
Maximum duty cycle vs. ambient temperature (ch. 1)
V_{CC}=3.3V, R_T=12kΩ (f_{OSC}=500kHz)



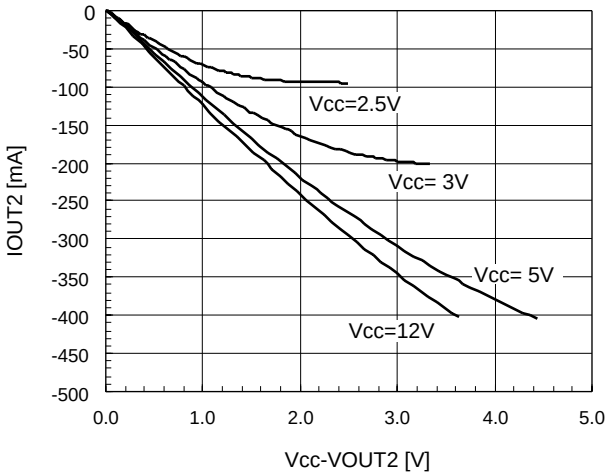
Maximum duty cycle vs. ambient temperature (ch. 2)
V_{CC}=3.3V, R_T=12kΩ (f_{OSC}=500kHz)



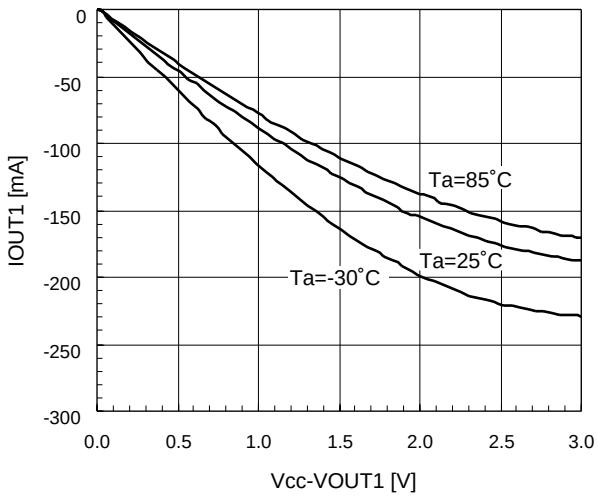
OUT1 terminal source current vs. H level output voltage
Ta=25˚C



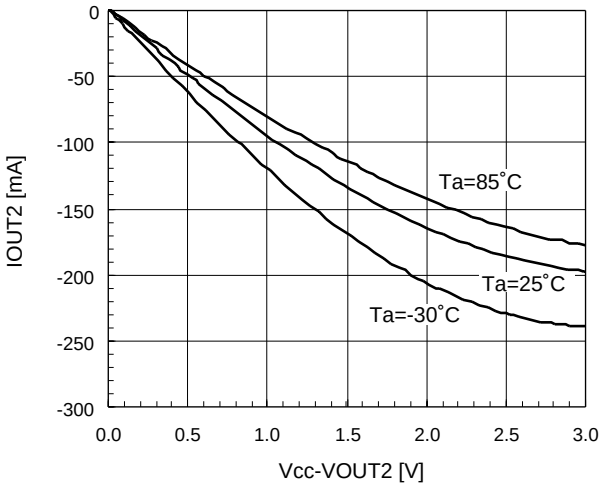
OUT2 terminal source current vs. H level output voltage
Ta=25˚C



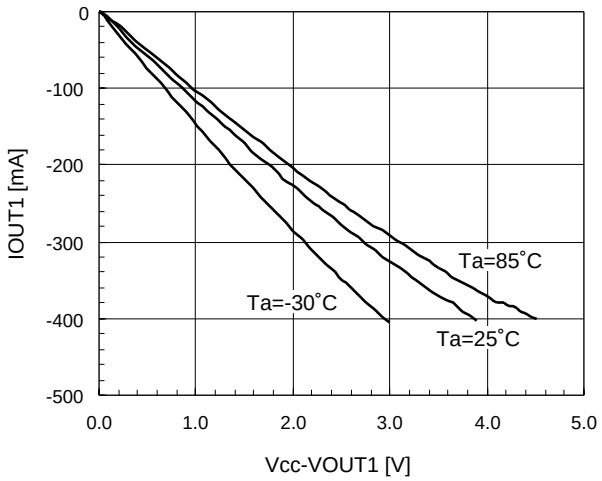
OUT1 terminal source current vs. H level output voltage
V_{CC}=3.3V



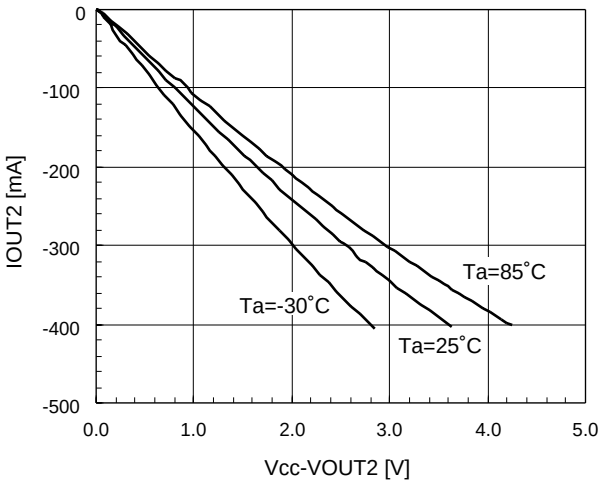
OUT2 terminal source current vs. H level output voltage
V_{CC}=3.3V



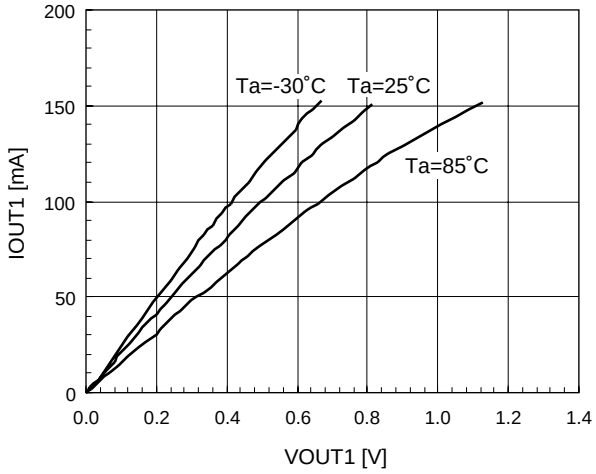
OUT1 terminal source current vs. H level output voltage
V_{CC}=12V



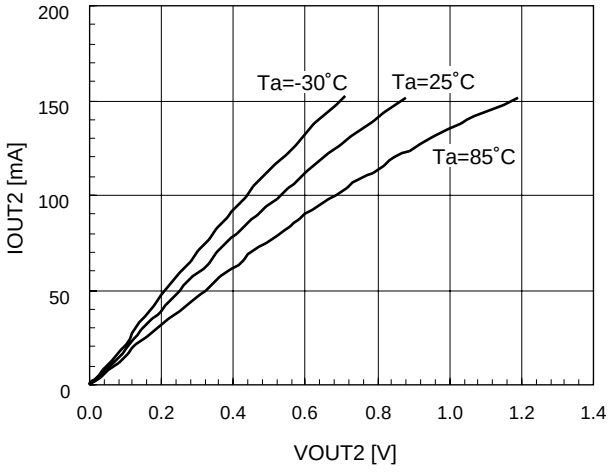
OUT2 terminal source current vs. H level output voltage
V_{CC}=12V



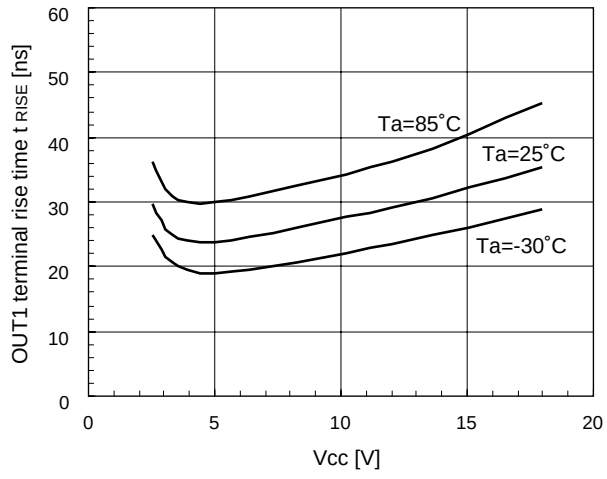
OUT1 terminal sink current vs. L level voltage



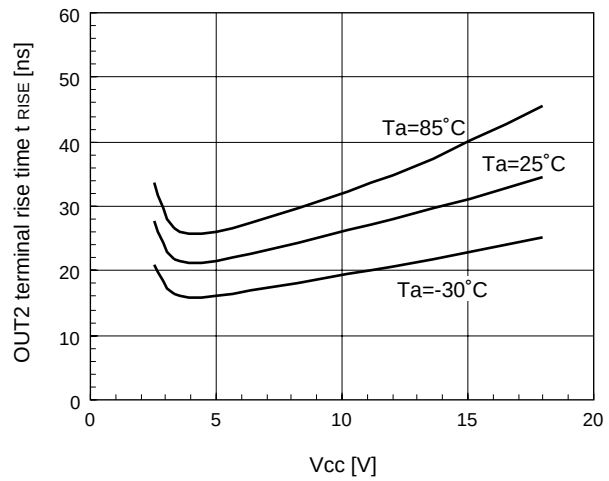
OUT2 terminal sink current vs. L level voltage



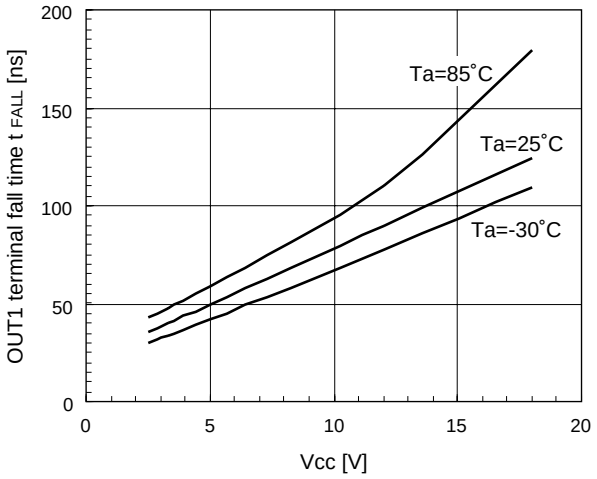
OUT1 terminal rise time vs. supply voltage Vcc
C_L=1000pF



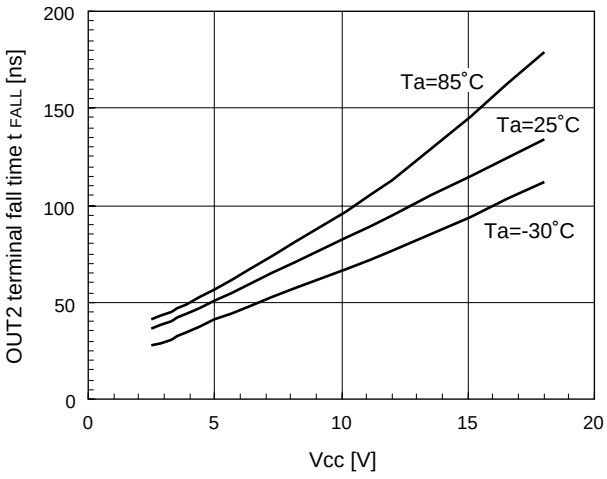
OUT2 terminal rise time vs. supply voltage Vcc
C_L=1000pF



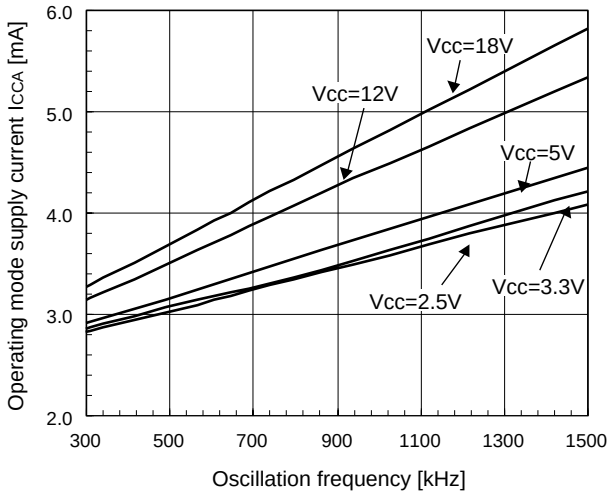
OUT1 terminal fall time vs. supply voltage Vcc
CL=1000pF



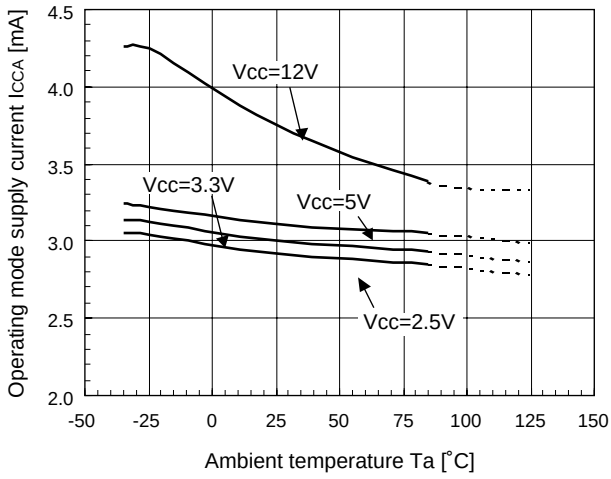
OUT2 terminal fall time vs. supply voltage Vcc
CL=1000pF



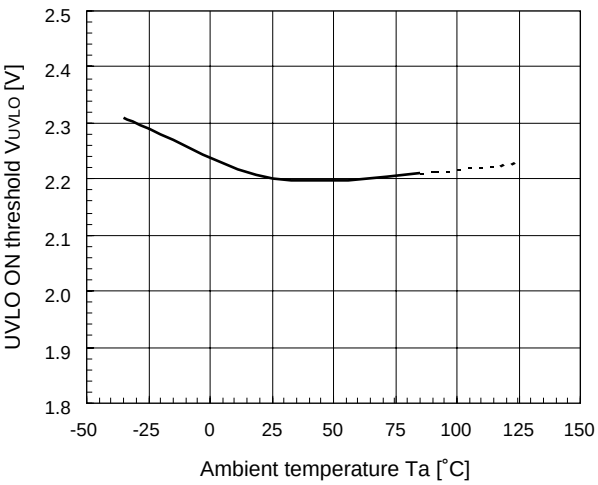
Operating mode supply current vs. oscillation frequency
Ta=25˚C



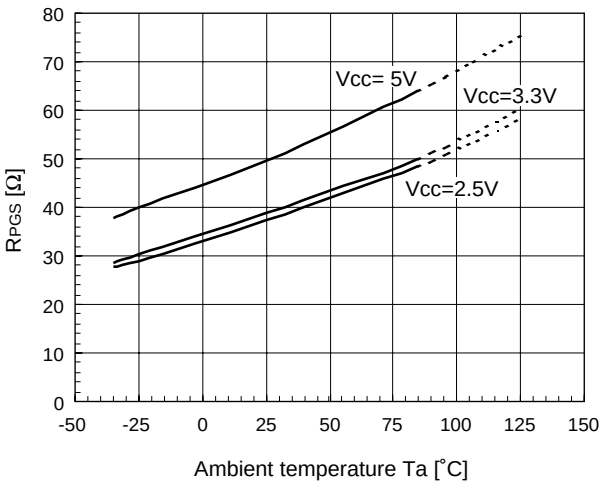
Operating mode supply current vs. ambient temperature



UVLO ON threshold vs. ambient temperature

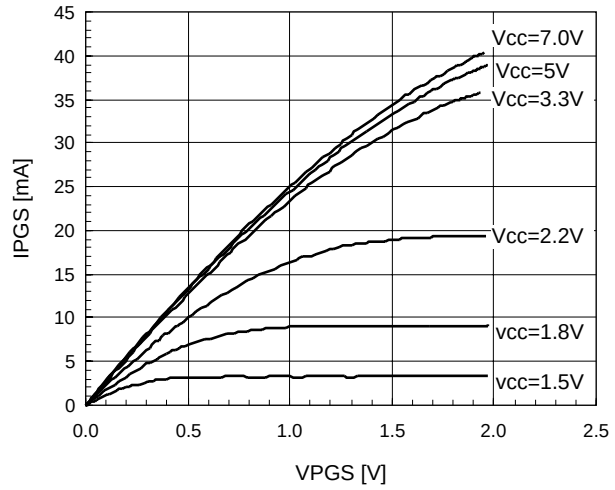


PGS terminal on resistance vs. ambient temperature

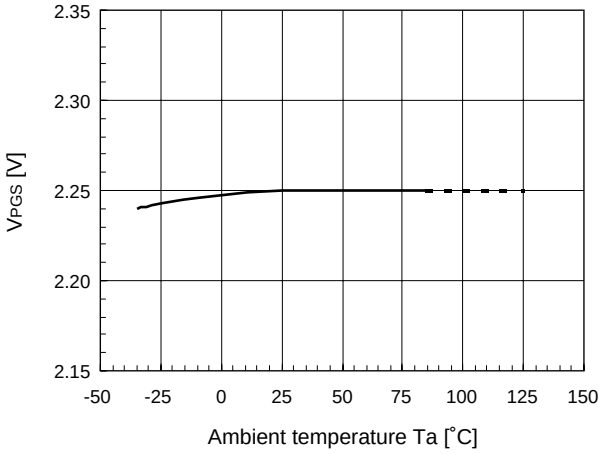


PGS terminal current vs. voltage

Ta=25˚C

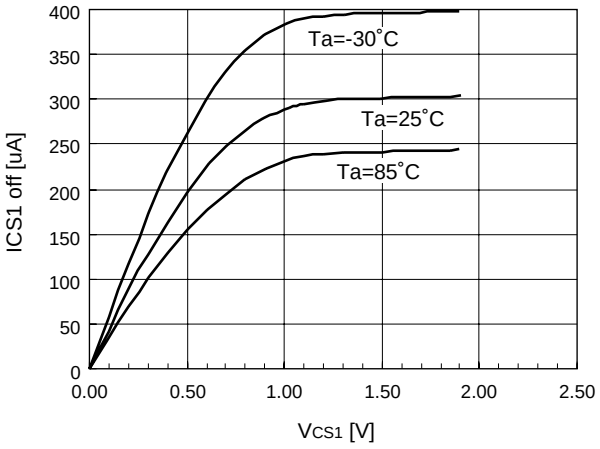


PGS terminal threshold voltage of VCC vs. ambient temperature



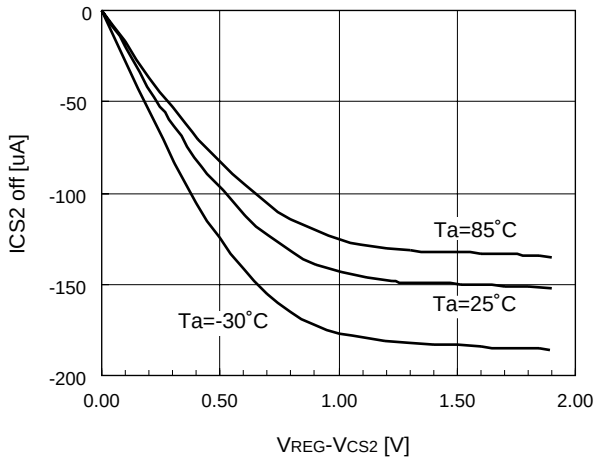
CS1 internal discharge switch current vs. voltage

VCC=3.3V, RT=12kΩ (fOSC=500kHz)

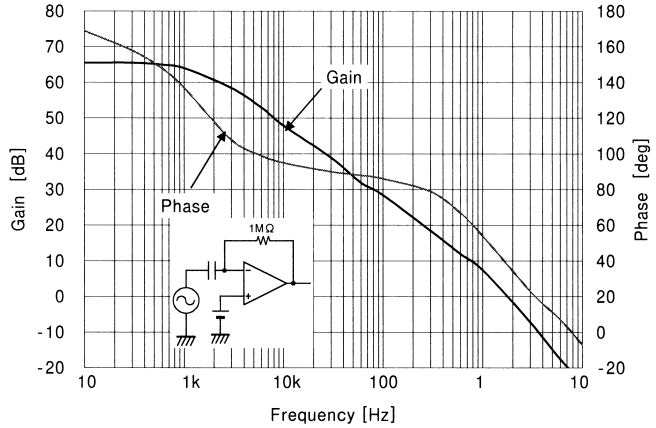


CS2 internal discharge switch current vs. voltage

VCC=3.3V, RT=12kΩ (fOSC=500kHz)



Error amplifier gain and phase vs. frequency



■ Description of each circuit

1. Reference voltage circuit (V_{REF})
This circuit generates the reference voltage of 1.00V (ch1: ±1%; ch2, 3: ±2%) compensated in temperature from V_{CC} voltage, and is connected to the non-inverting input of the error amplifier. This voltage cannot be observed directly because an external pin for this purpose is not provided.

2. Regulated voltage circuit (V_{REG})
This circuit generates 2.20V±1% based on the reference voltage V_{REF}, and is used as the power supply of the internal IC circuits. This voltage is generated when the supply voltage, V_{CC}, is input. The V_{REG} voltage also is used as a regulated power supply for soft start and others. The output current for external circuit should be within 1mA. A capacitor connected between VREG pin and GND pin is necessary to stable the V_{REF} voltage (To determine capacitance, refer to recommended operating conditions). The V_{REG} voltage is regulated in V_{CC} voltage of 2.4V or above.

3. Oscillator
The oscillator generates a triangular waveform by charging and discharging the built-in capacitor. A desired oscillation frequency can be set by the value of the resistor connected to the RT pin (Fig. 1). The built-in capacitor voltage oscillates between approximately 0.82V and 1.38V at fosc=500kHz (that of ch1 and ch2 are slightly different) with almost the same charging and discharging gradients (Fig. 2). You can set the desired oscillation frequency by changing the gradients using the resistor connected to the RT pin. (Large R_T: low frequency, small R_T: high frequency) The oscillator waveform cannot be observed from the outside because a pin for this purpose is not provided. The RT pin voltage is approximately 1V DC in normal operation. The oscillator output is connected to the PWM comparator.

4. Error amplifier circuit
The error amplifiers 1, 2, 3 have inverting input pins of IN1– pin (Pin 14), IN2– pin (Pin 4) and IN3– pin (Pin 2). The non-inverting input is internally connected to the reference voltage V_{REF} of the error amplifier 1 (1.00V±1%; 25˚C) and the error amplifiers 2, 3 (1.00V±2%; 25˚C). The FB pins (Pin1, Pin15) are the output of the error amplifiers. An external RC network is connected between FB pin and IN– pin for gain and phase compensation setting. The error amplifier 3 can be used for a series regulator.

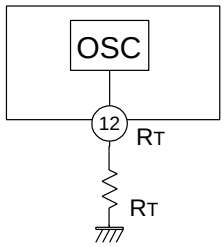


Fig. 1

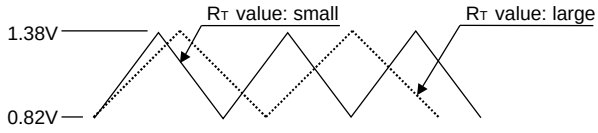


Fig. 2

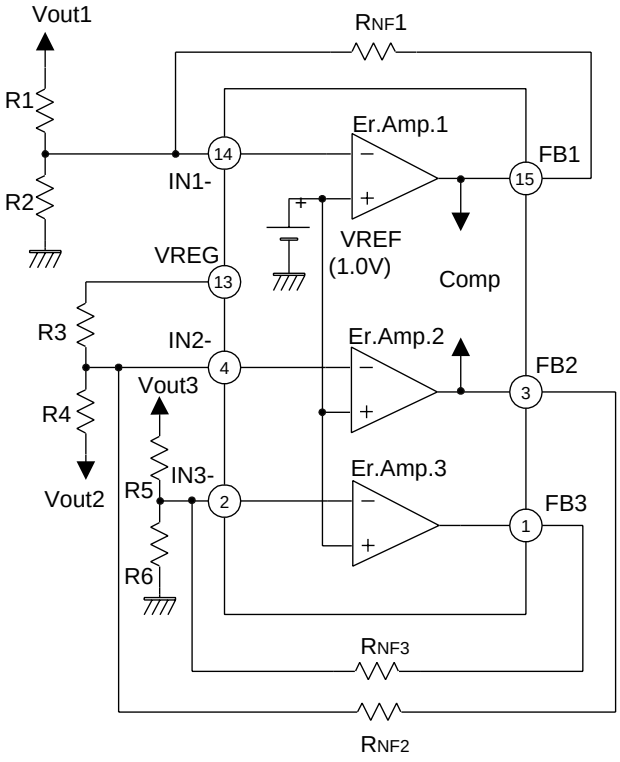


Fig. 3

5. PWM comparator

The PWM output generates from the oscillator output, the error amplifier output (FB1, FB2) and CS voltage (CS1, CS2) (Fig. 4). The oscillator output is compared with the preferred lower voltage between FB1 and CS1 for ch1. While the preferred voltage is lower than oscillator output, the PWM output is low. While the preferred voltage is higher than oscillator output, the PWM output is high. Since the phase of Ch2 is the opposite phase of Ch1, higher voltage between FB2 and CS2 is preferred and while the preferred voltage is lower than the oscillator output, the PWM output 2 is high. (Cannot be observed externally) The output polarity of OUT1, OUT2 changes according to the condition of SEL pin. (See Fig. 6) The maximum duty cycle (DMAX1, DMAX2) is internally set approximately 85%. Note that the maximum duty cycle depends on operation frequencies. (See the characteristics curve: Output duty cycle vs. oscillation frequency)

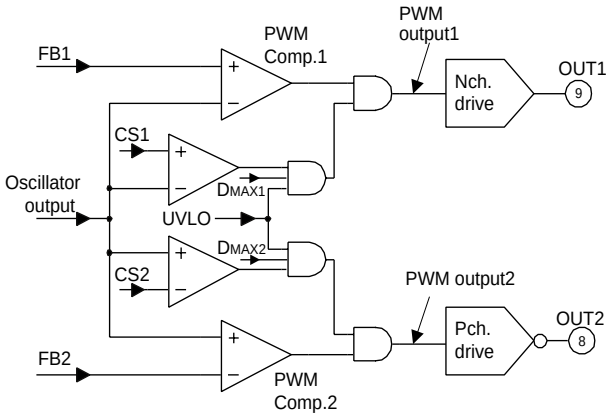


Fig. 4

6. Soft start function

This IC has a soft start function to protect DC-to-DC converter circuits from damage when starting operation. CS1 pin (Pin10) and CS2 pin (Pin7) are used for soft start function of ch1 and ch2 respectively. (Fig. 5) When the supply voltage is applied to the VCC pin and UVLO is cancelled, the capacitor C_{CS1} and C_{CS2} is charged by the internal constant current sources (2µA, typ.). Then, the CS1 voltage gradually increases, and the CS2 voltage gradually decreases. Since the CS1, and CS2 are connected to the PWM comparator, the pulses gradually widen and then the soft start function operates. (Fig. 6)

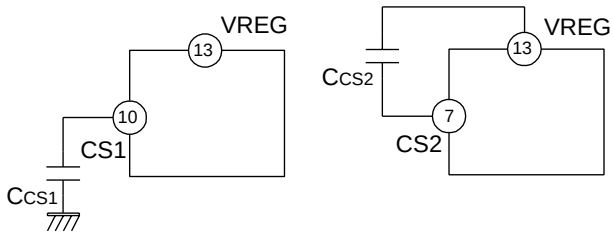


Fig. 5

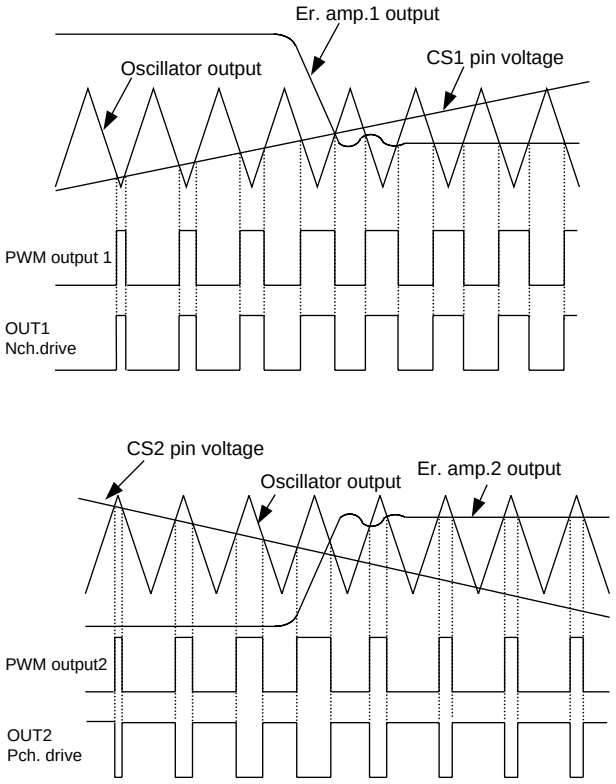


Fig. 6

7. Timer latch short-circuit protection circuit

This IC has the timer latch short-circuit protection circuit. The circuit cuts off the output of all channels when the output voltage of DC-to-DC converter drops due to short circuit or overload. Delay time of the timer latch mode is set by a counter system in the internal circuit, therefore, no external parts are necessary. When one of the output voltage of the DC-to-DC converter drops due to a short circuit or overload, the FB1 and FB3 pin voltage increases up to around the V_{REG} voltage for ch1 and ch3, or the FB2 pin voltage drops down to around 0V for ch2.

The counter system operates when the FB1 or FB3 pin voltage exceeds the timer latch threshold voltage of 2.0V(max.) or FB2 pin voltage falls below timer latch threshold voltage of 0.2V(min.). The counter system counts oscillator waveform. If this system counts the oscillation cycles of 2^{16} times (TL pin: GND, 16th stage counter) or 2^{17} times (TL pin: VREG, 17th stage counter), this circuit detects short circuit. Then the IC is set to off latch mode and the output of all channels is shut off and the current consumption becomes 2.5mA (typ.). (Fig. 7)

If the DC-to-DC converters return to normal before counter system counts 2^{16} or 2^{17}, counter is reset.

The period (tp) between the occurrences of short-circuit in the converter output and setting to off latch mode can be calculated by the following equations:

$$tp\ [s] = 2^{16} \times \frac{1}{fosc} \qquad \text{TL pin: GND}$$

$$tp\ [s] = 2^{17} \times \frac{1}{fosc} \qquad \text{TL pin: VREG}$$

Example. When fosc=500kHz and TL pin to GND, the period tp is:
$tp=2^{16} \times 1/500kHz=0.131sec.$

You can reset off latched mode of the short-circuit protection by either of the following ways to 1) CS pins, or 2) VCC pin:

1) Set the CS pin of the cause of off latch mode as follows.
   CS1 pin voltage = 0V, CS2 pin voltage = VREG
2) V_{CC} voltage is below UVLO off threshold voltage (2.1V typ.).
   Connect the TL pin to either VREG or GND. If TL pin is opened, the counter operation is unstable.

8. Output circuit

The IC contains a push-pull output stage and can directly drive MOSFETs. The maximum peak current of the output stage is sink current of +150mA, and source current of –400mA. The IC can also drive NPN and PNP transistors. The maximum current in such cases is ±50mA. You must design the output current considering the rating of power dissipation. (See "Design advice".)

9. Undervoltage lockout circuit

The IC contains an undervoltage lockout circuit to protect the circuit from the damage caused by malfunctions when the supply voltage drops. When the supply voltage rises from 0V, the IC starts to operate at V_{CC} of 2.2V (typ.) and outputs generate pulses. If a drop of the supply voltage occurs, it stops output at V_{CC} of 2.1V (typ.). When it occurs, the CS1 pin is turned to low level and the CS2 pin to high level, and then these pins are reset.

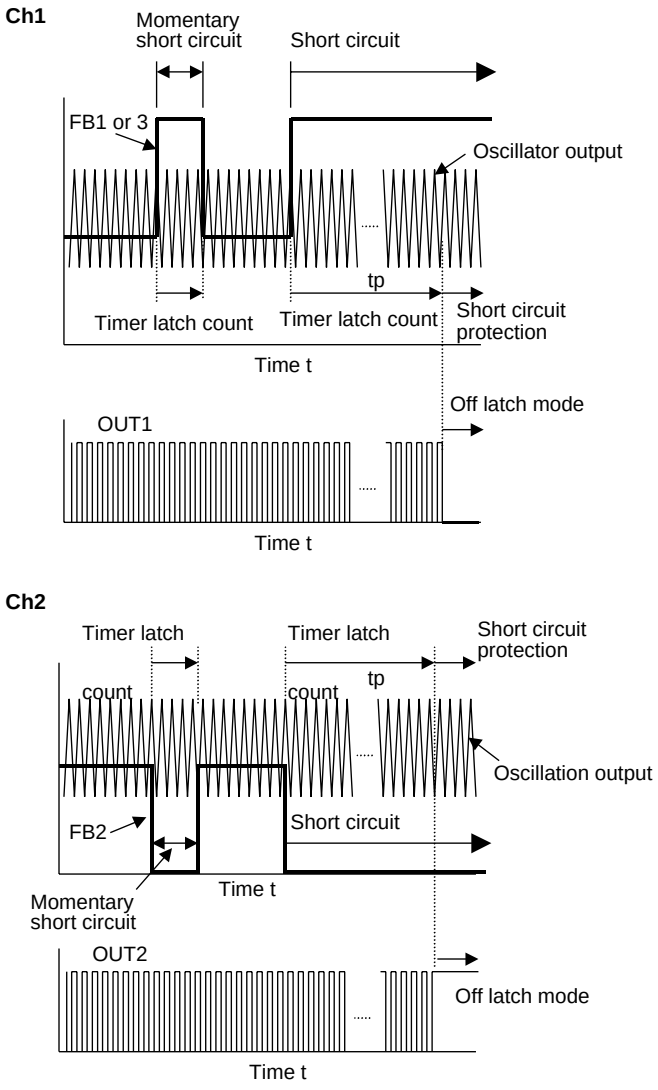


Fig. 7

10. PGS circuit

The PGS pin is an open drain output of Nch MOSFET for transmitting fault signals of the power supply. The PGS circuit is enabled when Vcc voltage is over the operating threshold voltage (approximately 1V). The Nch MOSFET turns ON and the PGS pin is connected to GND if any of the following three conditions occurs:

1) the V_{CC} voltage is below the threshold voltage (V_{CC} increasing: 2.35V typ.; V_{CC} decreasing: 2.25V typ.), 2) UVLO turns on (V_{CC}=2.1V or below), 3) IC is off latch mode.

The operation sequence is shown in Fig. 8.

As shown in Fig. 8, in the case of increasing the Vcc voltage with the voltage V applied to the PGS pin, when the Vcc voltage reaches 1V, PGS circuit is enabled and detects that the Vcc voltage is not enough high. Then PGS circuit turns the Nch MOSFET on and output fault signal. The fault signal is cancelled when the V_{CC} voltage exceeds 2.35V (typ.).

In the case that the V_{CC} voltage exceeds 2.53V (typ.) and the IC is off latch mode, the PSG circuit detects it as abnormal and the Nch MOSFET is turned on.

In the case of decreasing the V_{CC} voltage, the circuit sends out fault signals when the V_{CC} voltage is below 2.25V (typ.) and continues to output until the V_{CC} voltage reaches below the PGS circuit operation threshold voltage of approximately 1V. (Under the V_{CC} voltage of 1V, the circuit does not operate normally.)

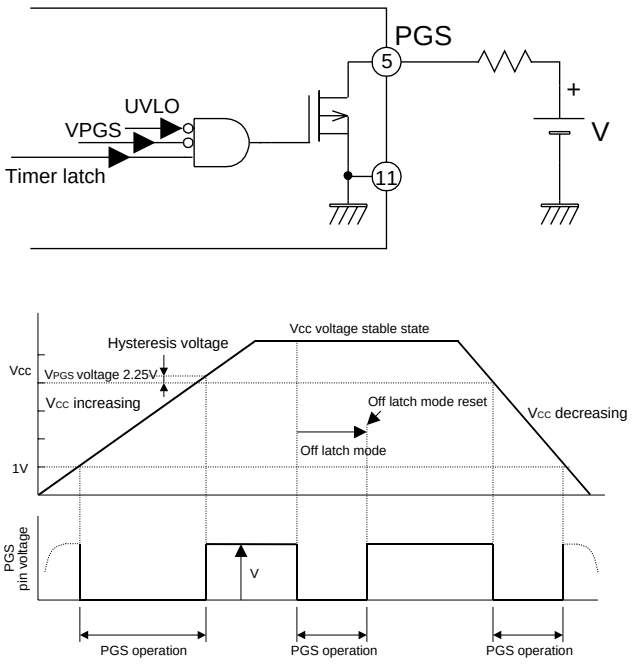


Fig. 8

■ Design advice

1. Setting the oscillation frequency

As described in item 1, "Description of each circuit," a desired oscillation frequency can be determined by the value of the resistor connected to the RT pin. When designing an oscillation frequency, you can set any frequency between 300kHz and 1.5MHz. You can obtain the oscillation frequency from the characteristic curve "Oscillation frequency (fosc) vs. timing resistor resistance (R_T)" or the value can be approximately calculated by the following expression.

$$f_{OSC} = 4050 \times R_T^{-0.86}$$

$$R_T = \left(\frac{4050}{f_{OSC}}\right)^{1.16}$$

f_{OSC}: Oscillation frequency [kHz]
RT: Timing resistor [kΩ]

This expression, however, can be used for rough calculation, the obtain value is not guaranteed. The operation frequency varies due to the conditions such as tolerance of the characteristics of the ICs, influence of noises, or external discrete components. When determining the values, examine the effectiveness of the values in an actual circuit. The timing resistor R_T should be wired to the GND pin as shortly as possible because the RT pin is a high impedance pin and is easy affected by noises.

2. Determining soft start period

The period from the start of charging the capacitor C_{CS} to widening n% of output duty cycle can be roughly calculated by the following expression: (see Fig. 5 for symbols)

$$t\,[s] = \frac{V_{CS2n} \times C_{CS1}}{I_{CS1}}$$ For CS1 pin

$$t\,[s] = \frac{(V_{REG} - V_{CS2n}) \times C_{CS1}}{I_{CS2}}$$ For CS2 pin

C_{CS1}, C_{CS2}: Capacitance connected to the CS1 or CS2 pin [µF]
I_{CS1}, I_{CS2}: CS charge current [µA] (2µA typ.)

V_{CS1n} and V_{CS2n} are the voltage of the CS1 and CS2 pins in n% of output duty cycle, and vary in accordance with operating frequency. The value can be obtained from the characteristic curve "Output duty cycle vs. C_S voltage"
The charging of the C_{CS1} and C_{CS2} starts after the UVLO is unlocked. Therefore, the period from power-on of V_{CC} to widening n% of output duty cycle is the sum of t0 and t.
To reset the soft start function, the supply voltage V_{CC} is lowered below the UVLO voltage (2.1V typ.) and then the internal switch discharges the CS capacitor. The characteristics of the internal switch for discharge are shown in following the characteristics curves of "Characteristics of CS1 internal discharge switch current vs. voltage" and "Characteristics of CS2 internal discharge switch current vs. voltage". Therefore, when determining the period of soft start at restarting the power supply, consider the characteristics carefully.

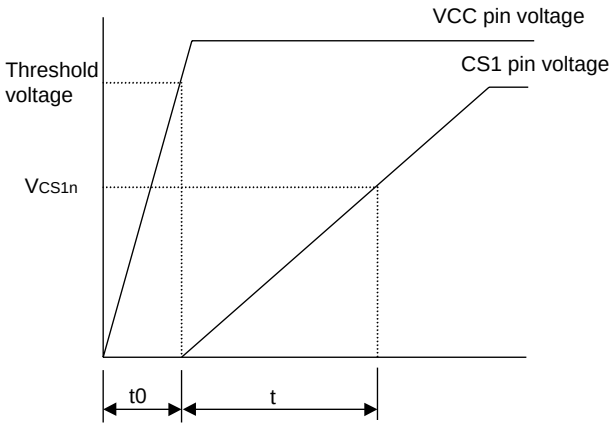


Fig. 9

3. Determining the output voltage of DC-DC converters

The ways to determine the output voltage of the DC-DC converter of each channel is shown in Fig. 10 and the following equations.

For ch1:
The output voltage of a boost circuit is determined by:

$$Vout1 = \frac{R1 + R2}{R2} \times V_{REF}$$

For ch2:
The output voltage of an inverting circuit is determined by:

$$Vout2 = \frac{R3 + R4}{R3} \times V_{REF} - \frac{R4}{R3} \times V_{REG}$$

The ratio of resistances is determined by:

$$\frac{R3}{R3} = \frac{V_{REG} - V_{REF}}{Vout2 + V_{REF}}$$

(Use the absolute value of the Vout2 voltage.)

For ch3:
The output voltage of a series regulator is determined by:

$$Vout3 = \frac{R5 + R6}{R6} \times V_{REF}$$

4. Restriction of external discrete components and recommended operating conditions

To achieve a stable operation of the IC, the value of external discrete components connected to VCC, VREG, CS pins should be within the recommended operating conditions. And the voltage and current applied to each pin should be also within the recommended operating conditions. If the pin voltage of OUT1, OUT2, or VREG becomes higher than the VCC pin voltage, the current flows from the pins to the VCC pin because parasitic three diode exist between the VCC pin and these pins. Be careful not to allow this current to flow.

5. Loss calculation of IC

Since it is difficult to measure IC loss directly, the calculation to obtain the approximate loss of the IC connected directly to a MOSFET is described below.
When the supply voltage is V_{CC}, the current consumption of the IC is I_{CCA}, the total input gate charge of the driven MOSFET is Qg and the switching frequency is fsw, the total loss Pd of the IC can be calculated by:

$Pd \fallingdotseq V_{CC} \times (I_{CCA} + Qg \times fsw)$.
The value in this expression is influenced by the effects of the dependency of supply voltage, the characteristics of temperature, or the tolerance of parameter. Therefore, evaluate the appropriateness of IC loss sufficiently considering the range of values of above parameters under all conditions.

Example:
I_{CCA}=3.0mA for V_{CC}=3.3V in the case of a typical IC from the characteristics curve. Qg=6nC, fsw=500kHz, the IC loss "Pd" is as follows.
$Pd \fallingdotseq 3.3 \times (3.0mA + 6nC \times 500kHz) \fallingdotseq 19.8mW$

If two MOSFETs are driven under the same condition for 2 channels, Pd is as follows:

$Pd \fallingdotseq 3.3 \times \{3.0mA + 2 \times (6nC \times 500kHz)\} = 29.7mW$

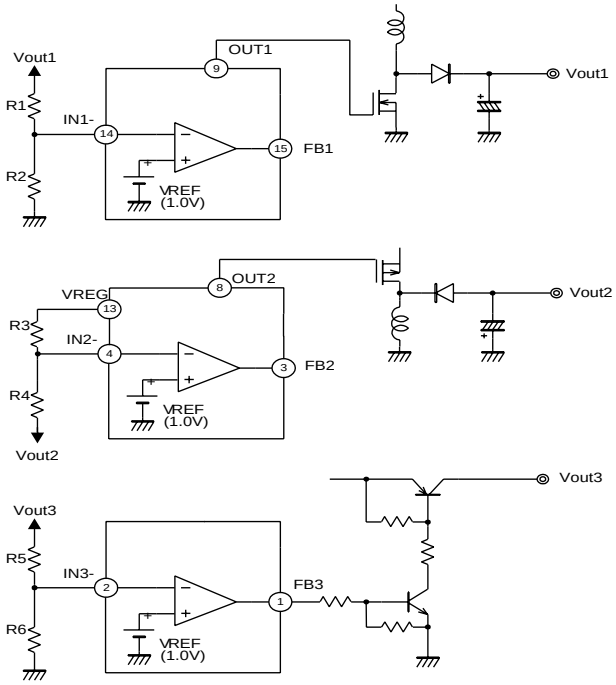
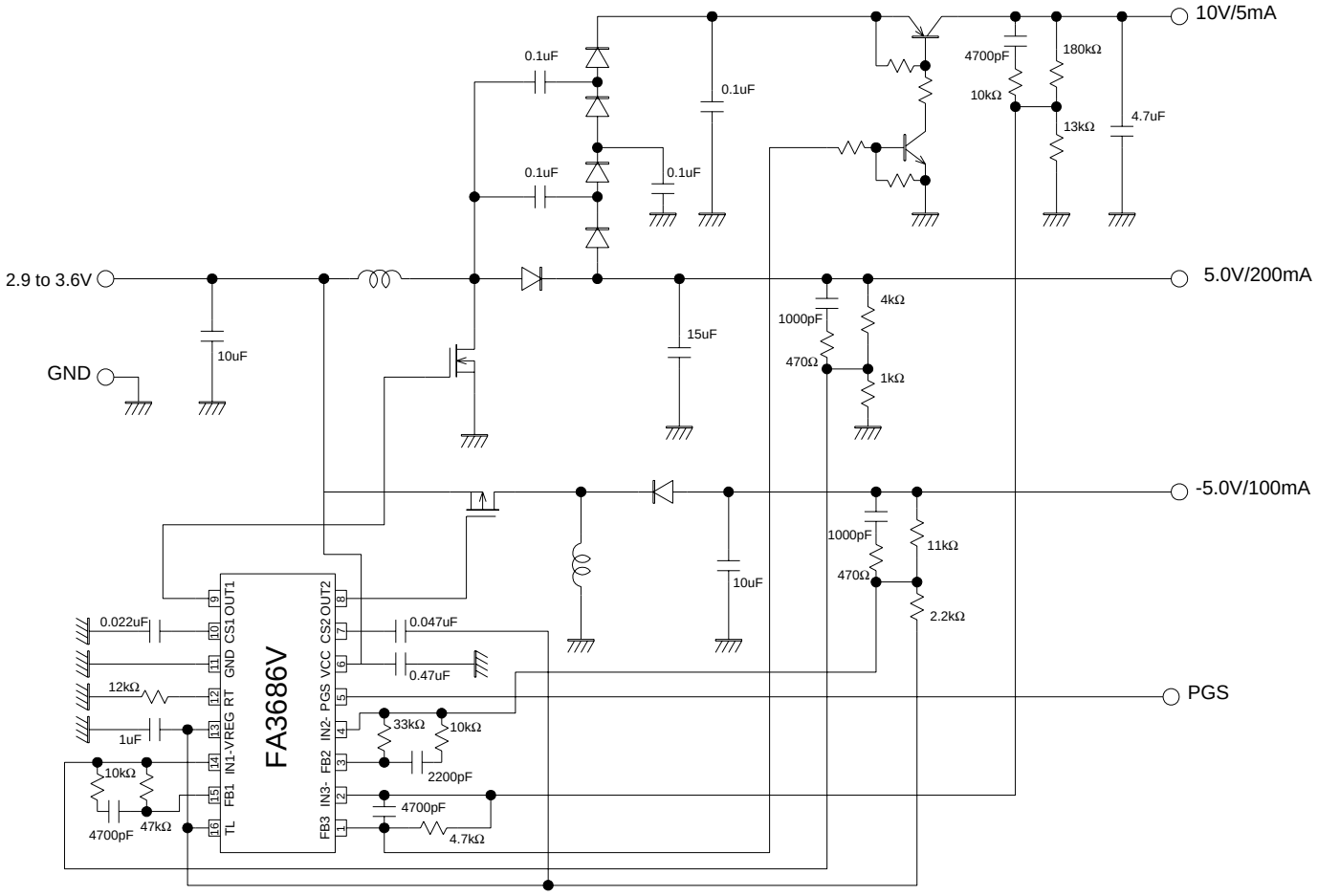


Fig. 10

■ Application circuit



Parts tolerances characteristics are not defined in the circuit design sample shown above. When designing an actual circuit for a product, you must determine parts tolerances and characteristics for safe and economical operation.