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FAN4800
Low Start-Up Current PFC/PWM Controller Combos

Features

- Low start-up current(100µA typ.)
- Low operating current(2.5mA typ.)
- Low total harmonic distortion, high power factor
- Pin-compatible upgrade for the ML4800
- Average current, continuous, or discontinuous boost leading edge PFC
- Slew rate enhanced transconductance error amplifier for ultra-fast PFC response
- Internally synchronized leading edge PFC and trailing edge PWM
- Reduction of ripple current in the storage capacitor between the PFC and PWM sections
- PWM configurable for current mode or voltage mode operation
- Additional folded-back current limit for PWM section
- 20V BiCMOS process
- VIN OK guaranteed turn on PWM at 2.25V
- Vcc OVP Comparator, Low Power Detect Comparator
- Current-Fed gain modulator for improved noise immunity
- Brown out control, over-voltage protection, UVLO, soft start, and Reference OK
- Available in a 16-DIP Package

Applications

- Desktop PC Power Supply
- Internet Server Power Supply
- Un-interruptible Power Supply UPS
- Battery Charger
- DC Motor Power Supply
- Monitor Power Supply
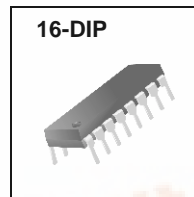- Telecom System Power Supply
- Distributed Power

General Description

The FAN4800 is a controller for power factor corrected, switched mode power supplies. Power Factor Correction (PFC) allows the use of smaller, lower cost bulk capacitors, reduces power line loading and stress on the switching FETs, and results in a power supply that fully complies with the IEC-1000-3-2 specifications. Intended as a Bi-CMOS version of the industry-standard ML4800, the FAN4800 includes circuits for the implementation of leading edge, average current, boost type power factor correction and a trailing edge, pulse width PWM (Pulse Width Modulator). A gate driver with 1A capabilities minimizes the need for external driver circuits. Low power requirements improve efficiency and reduce component costs.
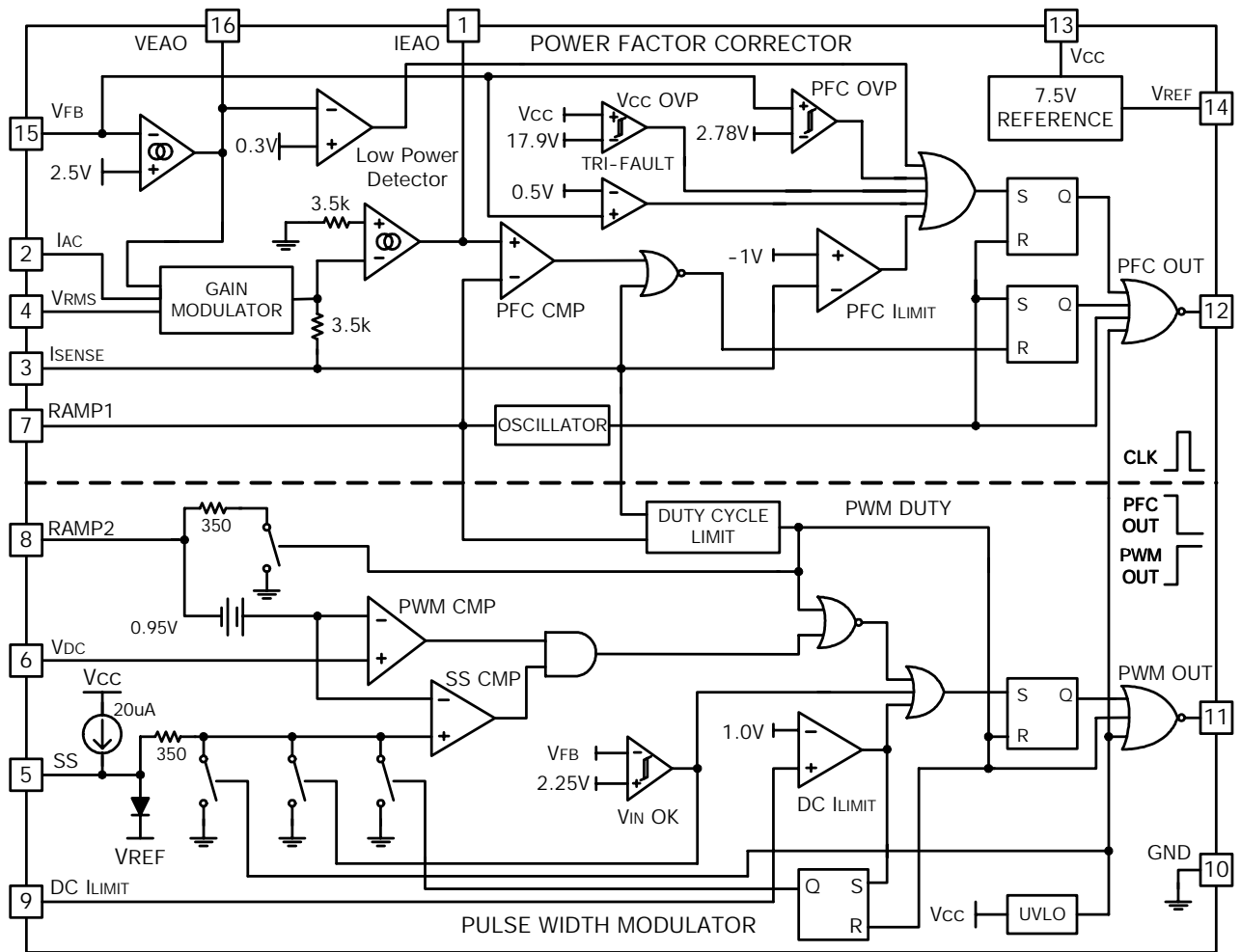
An over voltage comparator shuts down the PFC section in the event of a sudden decrease in load. The PFC section also includes peak current limiting and input voltage brownout protection. The PWM section can be operated in current or voltage mode, at up to 250kHz, and includes an accurate 50% duty cycle limit to prevent transformer saturation.

The FAN4800 includes a folded-back current limit for the PWM section to provide a short circuit protection function.
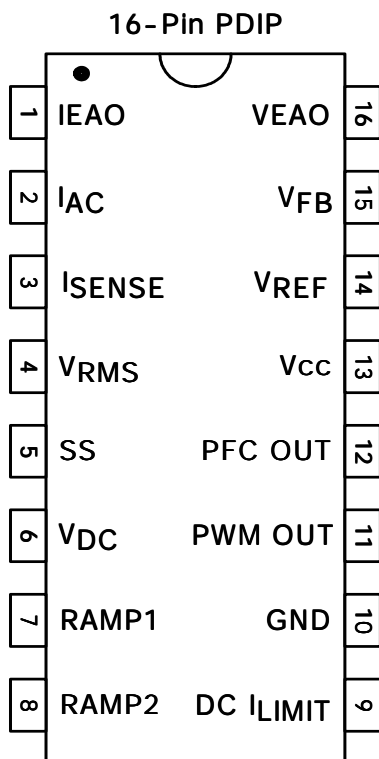
16-DIP

Rev. 1.0.0

Internal Block Diagram

Pin Configuration

16-Pin PDIP

Pin	Left			Right	Pin
1	IEAO			VEAO	16
2	IAC			VFB	15
3	ISENSE			VREF	14
4	VRMS			VCC	13
5	SS			PFC OUT	12
6	VDC			PWM OUT	11
7	RAMP1			GND	10
8	RAMP2			DC ILIMIT	9

Pin Descriptions

Pin No.	Symbol	Description
1	IEAO	PFC transconductance current error amplifier output
2	IAC	PFC gain control reference input
3	ISENSE	Current sense input to the PFC current limit comparator
4	VRMS	Input for PFC RMS line voltage compensation
5	SS	Connection point for the PWM soft start capacitor
6	VDC	PWM voltage feedback input
7	RAMP1 (RtCt)	Oscillator timing node; timing set by RT, CT
8	RAMP2 (PWM RAMP)	In current mode, this pin functions as the current sense input; in voltage mode, it is the PWM input from the PFC output (feed forward ramp)
9	DC ILIMIT	PWM current limit comparator input
10	GND	Ground
11	PWM OUT	PWM driver output
12	PFC OUT	PFC driver output
13	VCC	Positive supply
14	VREF	Buffered output for the internal 7.5V reference
15	VFB	PFC transconductance voltage error amplifier input
16	VEAO	PFC transconductance voltage error amplifier output

Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Parameter	Min.	Max.	Unit
V_{CC}	-	20	V
IEAO	0	5.5	V
I_{SENSE} Voltage	-5	0.7	V
Voltage on Any Other Pin	GND-0.3	VCC+0.3	V
I_{REF}	-	10	mA
I_{AC} Input Current	-	1	mA
Peak PFC OUT Current, Source or Sink	-	1	A
Peak PWM OUT Current, Source or Sink	-	1	A
PFC OUT, PWM OUT Energy per Cycle	-	1.5	μJ
Junction Temperature	-	150	°C
Storage Temperature Range	-65	150	°C
Operating Temperature Range	-40	125	°C
Lead Temperature (Soldering,10 sec.)	-	260	°C
Thermal Resistance(θ_{JA}) Plastic DIP	-	80	°C/W

Electrical Characteristics

Unless otherwise stated, these specifications apply: VCC=15V, RT=52.3KΩ, CT=470pF, TA= -40°C to 125°C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VOLTAGE ERROR AMPLIFIER						
Input Voltage Range	Vfb	Note3	0	-	6	V
Transconductance	gm1	-	50	70	90	μmho
Feedback Reference Voltage	Vref(PFC)	T_A =25°C	2.45	2.5	2.55	V
Input Bias Current	Ib(Veao)	Note1	-1.0	-0.05	-	μA
Output High Voltage	Veao(H)	-	5.8	6.0	-	V
Output Low Voltage	Veao(L)	-	-	0.1	0.4	V
Sink Current	Isink(V)	T_A =25°C, V_{FB} = 3V VEAO = 6.0V	-	-35	-20	μA
Source Current	Isource(V)	T_A =25°C, V_{FB} = 1.5V VEAO = 1.5V	30	40	-	μA
Open Loop Gain	Gv	Note2, Note3	50	60	-	dB
Power Supply Rejection Ratio	PSRR1	11V < V_{CC} < 16.5V(Note3)	50	60	-	dB

Electrical Characteristics (Continued)

Unless otherwise stated, these specifications apply: VCC=+15V, RT=52.3KΩ, CT=470pF, TA= -40°C to 125°C.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
CURRENT ERROR AMPLIFIER						
Input Voltage Range	Vieao	Note3	-1.5	-	0.7	V
Transconductance	gm2	-	50	85	100	µmho
Input Offset Voltage	Voffset	TA =25°C	-	-	25	mV
Input Bias Current	Ibeao	Note3	-1	-	-	µA
Output High Voltage	Ieao(H)	-	4.0	4.25	-	V
Output Low Voltage	Ieao(L)	-	-	1.0	1.2	V
Sink Current	Isink(I)	ISENSE = +0.5, IEAO = 4.0V	-	-65	-35	µA
Source Current	Isource(I)	ISENSE = -0.5, IEAO = 1.5V	35	75	-	µA
Open Loop Gain	Gi	Note3	60	70	-	dB
Power Supply Rejection Ratio	PSRR2	11V < Vcc <16.5V(Note3)	60	75	-	dB
PFC OVP COMPARATOR						
Threshold Voltage	Vovp	TA =25°C	2.70	2.78	2.9	V
Hysteresis	HY(ovp)	TA =25°C	230	-	350	mV
LOW POWER DETECT COMPARATOR						
Threshold Voltage	Vth(lp)	TA =25°C	0.15	0.3	0.4	V
VCC OVP COMPARATOR						
Threshold Voltage	Vcc_ovp	TA =25°C	17.5	17.9	18.5	V
Hysteresis	HY(Vcc_ovp)	TA =25°C	1.40	1.5	1.65	V
TRI-FAULT DETECT						
Time to Fault Detect High	Td(F)	VFB=VFault Detect LOW to VFB=Open. 470pF from VFB to GND(Note3)	-	2	4	ms
Fault Detect Low	F(L)	-	0.4	0.5	0.6	V
PFC ILIMIT COMPARATOR						
Threshold Voltage	Vth(cs)	-	-1.10	-1.00	-0.90	V
(PFC ILIMIT VTH - Gain Modulator Output)	Vth(cs)-Vgm	-	5	100	-	mV
Delay to Output(Note 3)	Td(pfc_off)	-	-	250	-	ns
DC ILIMIT COMPARATOR						
Threshold Voltage	Vth(DC)	-	0.95	1.0	1.05	V
Delay to Output(Note 3)	Td(pwm_off)	-	-	250	-	ns
VIN OK COMPARATOR						
Threshold Voltage	Vth(OK)	-	2.10	-	2.45	V
Hysteresis	HY(OK)	-	0.8	1.0	1.2	V

Electrical Characteristics (Continued)

Unless otherwise stated, these specifications apply: VCC=15V, RT=52.3KΩ, CT=470pF, TA= -40°C to 125°C.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GAIN MODULATOR						
Gain (Note 2)	G1	I_{AC} =100μA, V_{RMS} =0, V_{FB}=1V T_A =25°C	0.70	0.84	0.95	
	G2	I_{AC} =100μA, V_{RMS} =1.1V, V_{FB}=1V T_A =25°C	1.80	2.00	2.20	
	G3	I_{AC} =150μA, V_{RMS} =1.8V, V_{FB}=1V T_A =25°C	0.90	1.00	1.10	
	G4	I_{AC} =300μA, V_{RMS} =3.3V, V_{FB}=1V T_A =25°C	0.25	0.32	0.40	
Band Width	BW	I_{AC} =100μA(Note3)	-	10	-	MHz
Output Voltage = 3.5kΩ * (I_{SENSE} - I_{OFFSET})	Vo(gm)	I_{AC} =250μA, V_{RMS} =1.1V, V_{FB}=2V T_A =25°C	0.80	1.00	1.20	V
OSCILLATOR						
Initial Accuracy	Fosc1	T_A =25°C	68	-	81	kHz
Voltage Stability	ΔFosc1	11V < V_{CC} < 16.5V	-	1	-	%
Temperature Stability	ΔFosc2	-	-	2	-	%
Total Variation	Fosc2	Line, Temp	66		84	kHz
Ramp Valley to Peak Voltage	Vramp	Note3	-	2.75	-	V
PFC Dead Time	Tdead	-	-	685	-	ns
CT Discharge Current	Idis	V_{RAMP2} = 0V, V_{RAMP1} = 2.5V	6.5	-	15	mA
REFERENCE						
Output Voltage	Vref1	T_A =25°C, I(V_{REF}) = 1mA	7.4	7.5	7.6	V
Line Regulation	ΔVref1	11V < V_{CC} < 16.5V	-	10	25	mV
Load Regulation	ΔVref2	0mA < I(V_{REF}) < 7mA	-	10	20	mV
Temperature Stability	ΔVref4	-	-	0.4	-	%
Total Variation	Vref2	Line, Load, Temp(Note3)	7.35	-	7.65	V
Long Term Stability	ΔVref5	T_J = 125°C, 1000hours(Note3)	5	-	25	mV
PFC						
Minimum Duty Cycle	Dmin	V_{IEAO} > 4.0V	-	-	0	%
Maximum Duty Cycle	Dmax	V_{IEAO} < 1.2V	92	95	-	%
Output Low Rdson	Ron(low)1	I_{OUT} = -20mA at T_A =25°C	-	-	15	Ω
	Ron(low)2	I_{OUT} = -100mA at T_A =25°C	-	-	15	Ω
Output Low Voltage	Vol1	I_{OUT} = -10mA, VCC = 9V at T_A =25°C (Note3)	-	0.4	0.8	V
Output High Rdson	Ron(high)1	I_{OUT} = 20mA at T_A =25°C	-	15	20	Ω
	Ron(high)2	I_{OUT} = 100mA at T_A =25°C	-	15	20	Ω
Rise/Fall Time	Tr(pfc)	C_L = 1000pF(Note3)	-	50	-	ns

Electrical Characteristics (Continued)

Unless otherwise stated, these specifications apply: VCC=+15V, RT=52.3KΩ, CT=470pF, TA= -40°C to 125°C.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PWM						
Duty Cycle Range	D	-	0-42	0-47	0-49	%
Output Low Rdson	Ron(low)3	I_{OUT} = -20mA at T_A =25°C	-	-	15	Ω
	Ron(low)4	I_{OUT} = -100mA at T_A =25°C	-	-	15	Ω
Output Low Voltage	Vol2	I_{OUT} = -10mA, VCC = 9V T_A =25°C	-	0.4	0.8	V
Output High Rdson	Ron(high)3	I_{OUT} = 20mA at T_A =25°C	-	15	20	Ω
	Ron(high)4	I_{OUT} = 100mA at T_A =25°C	-	15	20	Ω
Rise/Fall Time	Tr(pwm)	C_L = 1000pF(Note3)	-	50	-	ns
PWM Comparator Level Shift	PWM(ls)	-	0.8	0.95	1.2	V
SUPPLY						
Start-up Current	Ist	V_{CC} = 12V, C_L = 0pF	-	100	200	μA
Operating Current	Iop	14V, C_L = 0pF	-	2.5	7.0	mA
Under Voltage Lockout Threshold	Vth(start)	-	12.74	13	13.26	V
Under Voltage Lockout Hysteresis	Vth(hys)	-	2.80	3.0	3.20	V

Note1: Includes all bias currents to other circuits connected to the V_{FB} pin.

Note2: Gain = K $\times$ 5.375V; K = (I_{SENSE}-I_{OFFSET}) $\times$ [I_{AC} $\times$ (VEAO-0.625)] $^{-1}$; $VEAO_{MAX}$ = 6V

Note3: This parameter, although guaranteed by design, is not 100% production tested.

Typical Performance Characteristics
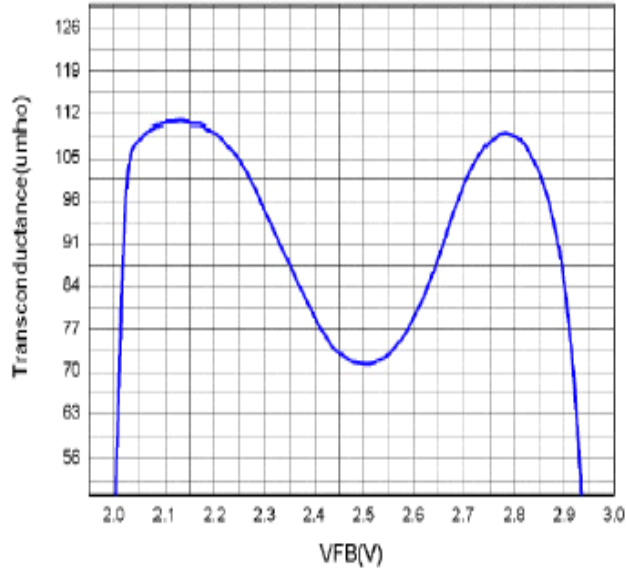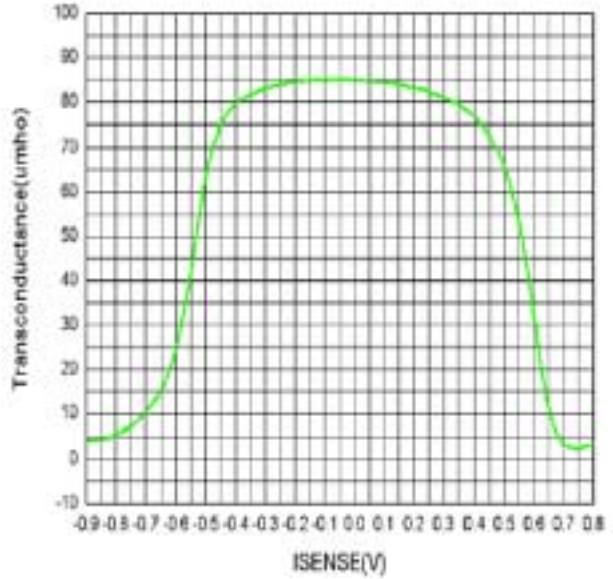

Figure A
Voltage Error Amplifier(gmv) Transconductance

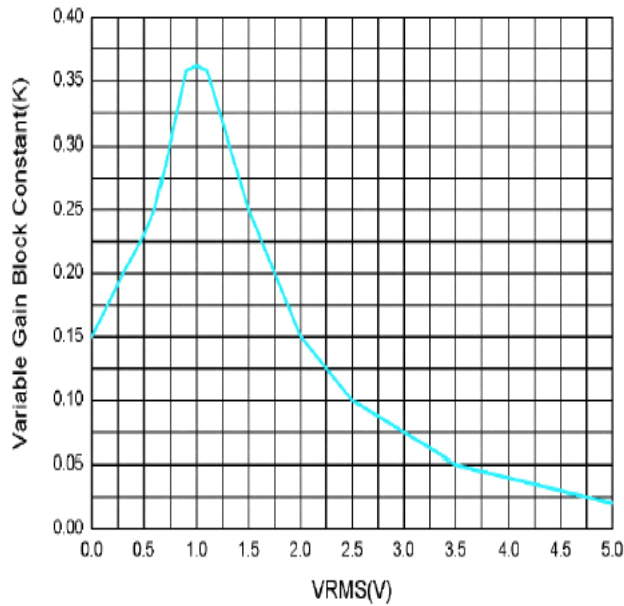**Figure B**
Current Error Amplifier(gmi) Transconductance

Figure C
Gain Modulator Transfer Characteristic (K)

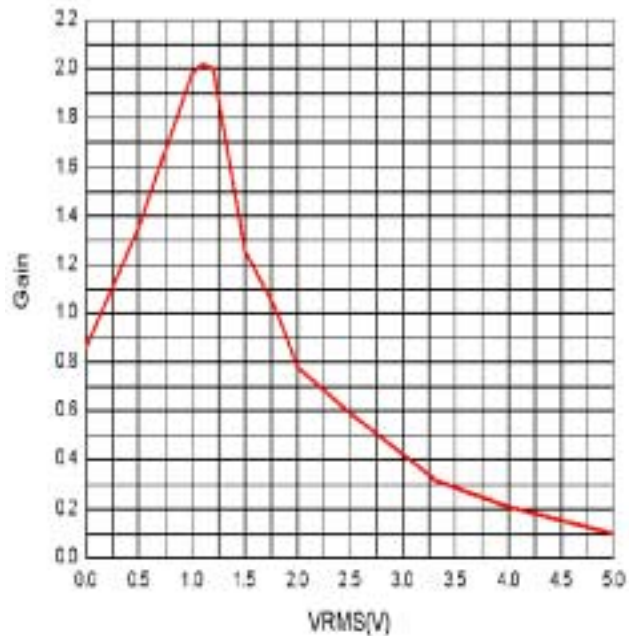$$K = \frac{I_{GAINMOD} - I_{OFFSET}}{I_{AC} \times (6 - 0.625)} mV^{-1}$$

Figure D
GAIN

$$Gain = \frac{I_{SENSE} - I_{OFFSET}}{I_{AC}}$$

Functional Description

The FAN4800 consists of an average current controlled, continuous boost Power Factor Correction (PFC) front end and a synchronized Pulse Width Modulator(PWM) back end. The PWM can be used in either current or voltage mode. In voltage mode, feed forward from the PFC output bus can be used to improve the PWM's line regulation. In either mode, the PWM stage uses conventional trailing edge duty cycle modulation. This patented leading/trailing edge modulation technique results in a higher usable PFC error amplifier bandwidth, and can significantly reduce the size of the PFC DC bus capacitor.

The synchronization of the PWM with the PFC simplifies the PWM compensation due to the controlled ripple on the PFC output capacitor (the PWM input capacitor). The PWM section of the FAN4800 runs at the same frequency as the PFC.

In addition to power factor correction, a number of protection features are built into the FAN4800. These include soft-start, PFC over voltage protection, peak current limiting, brownout protection, duty cycle limiting, and under voltage lockout (UVLO).

Power Factor Correction

Power Factor Correction treats a nonlinear load like a resistive load to the AC line. For a resistor, the current drawn from the line is in phase with and proportional to the line voltage, so the power factor is unity (one). A common class of nonlinear load is the input of most power supplies, which use a bridge rectifier and capacitive input filter fed from the line.

The peak charging effect, which occurs on the input filter capacitor in these supplies, causes brief high amplitude pulses of current to flow from the power line, rather than a sinusoidal current in phase with the line voltage. Such supplies present a power factor to the line of less than one(i.e. they cause significant current harmonics of the power line frequency to appear at their input). If the input current drawn by such a supply (or any other nonlinear load) can be made to follow the input voltage in instantaneous amplitude, it will appear resistive to the

To hold the input current draw of a device drawing power from the AC line in phase with and proportional to the input voltage, a way must be found to prevent that device from loading the line except in proportion to the instantaneous line voltage. The PFC section of the FAN4800 uses a boost mode DC-DC converter to accomplish this. The input to the converter is the full wave rectified AC line voltage. No bulk filtering is applied following the bridge rectifier, so the input voltage to the boost converter ranges (at twice line frequency) from zero volts to the peak value of the AC input and back to zero. By forcing the boost converter to meet two simultaneous conditions, it is possible to ensure that the current drawn from the power line is proportional to the input line voltage.

One of these conditions is that the output voltage of the boost converter must be set higher than the peak value of the line voltage. A commonly used value is 385VDC, to allow for a high line of 270VAC$_{rms.}$ The second condition is that the current drawn from the line at any given instant must be proportional to the line voltage. Establishing a suitable voltage control loop for the converter, which in turn drives a current error amplifier, and switching output driver satisfies the first of these requirements. The second requirement is met by using the rectified AC line voltage to modulate the output of the voltage control loop. Such modulation causes the current error amplifier to command a power stage current that varies directly with the input voltage. To prevent ripple, which will necessarily appear at the output of boost circuit (typically about 10VAC on a 385VDC level), from introducing distortion back through the voltage error amplifier, the bandwidth of the voltage loop is deliberately kept low. A final refinement is to adjust the overall gain of the PFC section to be proportional to $1/VIN^2$, which linearizes the transfer function of the system as the AC input voltage

Since the boost converter topology in the FAN4800 PFC is the current averaging type, no slope compensation is required.

PFC Section

Gain Modulator

Figure 1 shows a block diagram of the PFC section of the FAN4800. The gain modulator is the heart of the PFC, as the circuit block controls the response of the current loop to line voltage waveform and frequency, RMS line voltage, and PFC output voltages. There are three inputs to the gain modulator. These are:

1. A current representing the instantaneous input voltage (amplitude and wave shape) to the PFC. The rectified AC input sine wave is converted to a proportional current via a resistor and is then fed into the gain modulator at I_{AC}. Sampling current in this way minimizes ground noise, as is required in high power switching power conversion environments. The gain modulator responds linearly to this current.

2. A voltage proportional to the long term RMS AC line voltage, derived from the rectified line voltage after scaling and filtering. This signal is presented to the gain modulator at V_{RMS}. The output of the gain modulator is inversely proportional to V_{RMS}^2(except at unusually low values of V_{RMS} where special gain contouring takes over, to limit power dissipation of the circuit components under heavy brownout conditions). The relationship between V_{RMS} and gain is called K, and is illustrated in the Figure C of the Typical Performance Characteristics.

3. The output of the voltage error amplifier, VEAO. The gain modulator responds linearly to variations in this voltage.

The output of the gain modulator is a current signal, in the form of a full wave rectified sinusoid at twice the line frequency. This current is applied to the virtual ground (negative) input of the current error amplifier. In this way the gain modulator forms the reference for the current error loop, and ultimately controls the instantaneous current draw of the PFC from the power line. The general form of the output of the gain modulator is:

$$I_{GAINMOD} = \frac{I_{AC} \times VEAO}{V^2_{RMS}} \times 1V$$

More precisely, the output current of the gain modulator is given by:

$$I_{GAINMOD} = K \times (VEAO - 0.625) \times I_{AC}$$

where K is in units of V^{-1}

Note that the output current of the gain modulator is limited around 228.47µA and the maximum output voltage of the gain modulator is limited to 228.47µA* 3.5K = 0.8V.
This 0.8V will also determine the maximum input power. However, $I_{GAINMOD}$ cannot be measured directly from I_{SENSE}. $I_{SENSE} = I_{GAINMOD}-I_{OFFSET}$ and I_{OFFSET} can only be measured when VEAO is less than 0.5V and $I_{GAINMOD}$ is 0A. Typical I_{OFFSET} is around 60µA.

Selecting R_{AC} for IAC pin

I_{AC} pin is the input of the gain modulator. I_{AC} is also a current mirror input and it requires current input. Selecting a proper resistor R_{AC}, will provide a good sine wave current derived from the line voltage and also help program the maximum input power and minimum input line voltage.
R_{AC}=Vin peak * 7.9K. For example, if the minimum line voltage is 80VAC, the R_{AC}=80*1.414*7.9K=894Kohm.

Current Error Amplifier, IEAO

The current error amplifier's output controls the PFC duty cycle to keep the average current through the boost inductor a linear function of the line voltage. At the inverting input to the current error amplifier, the output current of the gain modulator is summed with a current which results from a negative voltage being impressed upon the I_{SENSE} pin.

The negative voltage on I_{SENSE} represents the sum of all currents flowing in the PFC circuit, and is typically derived from a current sense resistor in series with the negative terminal of the input bridge rectifier.

As stated above, the inverting input of the current error

amplifier is a virtual ground. Given this fact, and the arrangement of the duty cycle modulator polarities internal to the PFC , an increase in positive current from the gain modulator will cause the output stage to increase its duty cycle until the voltage on I_{SENSE} is adequately negative to cancel this increased current. Similarly, if the gain modulator's output decreases, the output duty cycle will decrease, to achieve a less negative voltage on the I_{SENSE} pin.

Cycle-By-Cycle Current Limiter and Selecting Rs

As well as being a part of the current feedback loop, the I_{SENSE} pin is a direct input to the cycle-by-cycle current limiter for the PFC section. If the input voltage at this pin is ever less than -1V, the output of the PFC will be disabled until the protection flip-flop is reset by the clock pulse at the start of the next PFC power cycle.

Rs is the sensing resistor of the PFC boost converter. During the steady state, line input current*Rs equals $I_{GAINMOD}$*3.5K.
Since the maximum output voltage of the gain modulator is $I_{GAINMOD}$ max*3.5K=0.8V during the steady state, Rs*line input current will be limited to below 0.8V as well. Therefore, to choose Rs, we use the following equation:

$$R_S = 0.8V \times (V_{INPEAK})/(2 \times \text{Line Input Power})$$

For example, if the minimum input voltage is 80VAC, and the maximum input RMS power is 200Watt,
R_S = (0.8V * 80V * 1.414)/(2*200)=0.226ohm.

PFC OVP

In the FAN4800, the PFC OVP comparator serves to protect the power circuit from being subjected to excessive voltages if the load changes suddenly. A resistor divider from the high voltage DC output of the PFC is fed to V_{FB}. When the voltage on V_{FB} exceeds 2.78V, the PFC output driver is shut down. The PWM section will continue to operate. The OVP comparator has 280mV of hysteresis, and the PFC will not restart until the voltage at V_{FB} drops below 2.50V. Also, Vcc OVP can serve as a redundant PFC OVP protection. VCC OVP and threshold is 17.9V with 1.5V hysteresis.
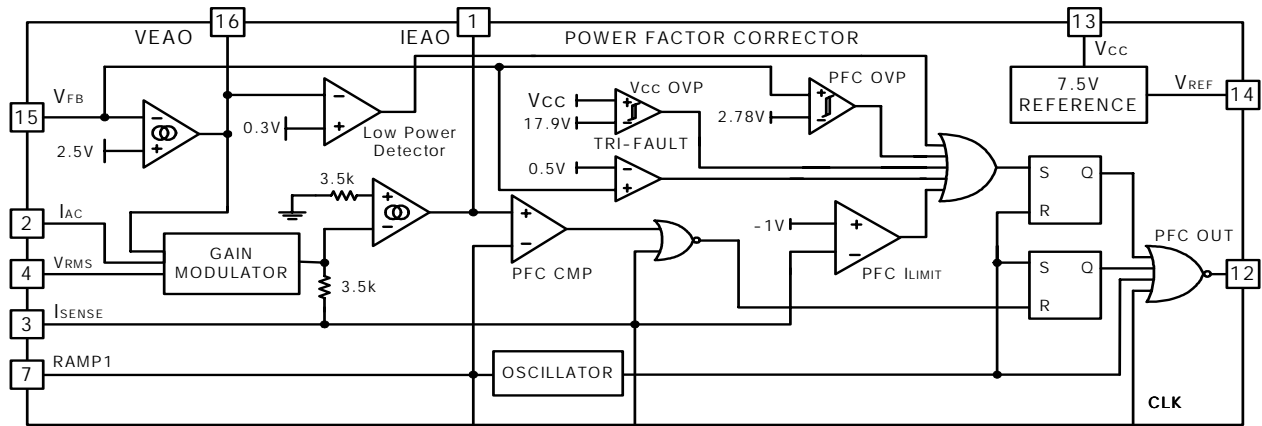
Figure 1. PFC Section Block Diagram

Error Amplifier Compensation

The PWM loading of the PFC can be modeled as a negative resistor because an increase in the input voltage to the PWM causes a decrease in the input current. This response dictates the proper compensation of the two transconductance error amplifiers.

Figure 2 shows the types of compensation networks most commonly used for the voltage and current error amplifiers, along with their respective return points. The current loop compensation is returned to V_{REF} to produce a soft-start characteristic on the PFC: As the reference voltage increases from zero volts, it creates a differentiated voltage on I_{EAO} which prevents the PFC from immediately demanding a full duty cycle on its boost converter.

PFC Voltage Loop

There are two major concerns when compensating the voltage loop error amplifier, V_{EAO}: Stability and transient response. Optimizing interaction between transient response and stability requires that the error amplifier's open loop crossover frequency should be 1/2 that of the line frequency, or 23Hz for 47Hz line (lowest anticipated international power frequency). The gain vs. input voltage of the FAN4800's voltage error amplifier, V_{EAO} has a specially shaped non-linearity so that under steady state operating conditions the transconductance of the error amplifier is at a local minimum. Rapid perturbation in line or load conditions will cause the input to the voltage error amplifier (VFB) to deviate from its 2.5V (nominal) value. If this happens, the transconductance of the voltage error amplifier will increase significantly, as shown in the Figure A of the Typical Performance Characteristics. This raises the gain-bandwidth product of the voltage loop, resulting in a much more rapid voltage loop response to such perturbations than would occur with conventional linear gain characteristics.

The Voltage Loop Gain(S) is given by:

$$= \frac{\Delta V_{OUT}}{\Delta V_{EAO}} \times \frac{\Delta V_{FB}}{\Delta V_{OUT}} \times \frac{\Delta V_{EAO}}{\Delta V_{FB}}$$

$$\approx \frac{P_{IN} \times 2.5V}{V^2_{OUTDC} \times \Delta V_{EAO} \times S \times C_{DC}} \times GM_V \times Z_C$$

where
Z_C : Compensation network for the voltage loop
GM_V: Transconductance of VEAO
P_{IN}: Average PFC input power
V_{ZOUTDC}: PFC boost output voltage; typical designed value is 380V.
C_{DC}: PFC boost output capacitor

PFC Current Loop

The compensation of the current amplifier, I_{EAO}, is similar to that of the voltage error amplifier, V_{EAO}, with the exception of the choice of crossover frequency. The crossover frequency of the current amplifier should be at least 10 times that of the voltage amplifier, to prevent interaction with the voltage loop. It should also be limited to less than $1/6^{th}$ of the switching frequency, e.g. 16.7kHz for a 100kHz switching frequency.

The Current Loop Gain(S) is given by:

$$= \frac{\Delta V_{ISENSE}}{\Delta D_{OFF}} \times \frac{\Delta D_{OFF}}{\Delta I_{EAO}} \times \frac{\Delta I_{EAO}}{\Delta V_{ISENSE}}$$

$$\approx \frac{V_{OUTDC} \times R_S}{S \times L \times 2.5V} \times GM_I \times Z_{CI}$$

where
Z_{CI}: Compensation network for the current loop

GM_I: Transconductance of IEAO

V_{OUTDC}: PFC boost output voltage; typical designed value is 380V. The equation uses the worst condition to

calculate the Z_{CI}
Rs: Sensing resistor of the boost converter

2.5V: Amplitude of the PFC leading modulation ramp

L: boost inductor

A modest degree of gain contouring is applied to the transfer characteristic of the current error amplifier, to increase its speed of response to current loop perturbations.
However, the boost inductor will usually be the dominant factor in overall current loop response.
Therefore, this contouring is significantly less marked than that of the voltage error amplifier. This is illustrated in the Figure A of the Typical Performance Characteristics.
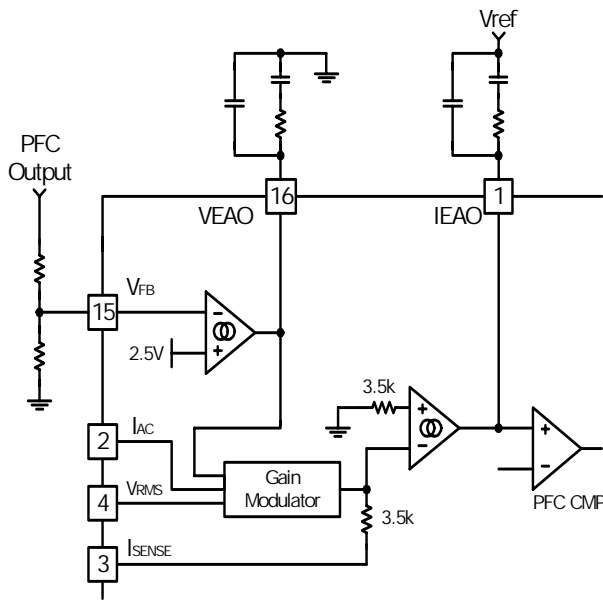

Figure 2. Compensation Network Connection for the Voltage and Current Error Amplifiers

I_{SENSE} filter, the RC filter between Rs and I_{ENSE}:
There are two reasons to add a filter at I_{SENSE} pin:
1) Protection: During start up or in-rush current conditions, it will have a large voltage cross, Rs, which is the sensing resistor of the PFC boost converter. It requires the I_{SENSE} filter to attenuate the energy.

2) To reduce L, the Boost Inductor: The I_{SENSE} filter also can reduce the Boost Inductor value since the I_{SENSE} filter behaves like an integrator before I_{SENSE} pin which is the input of the current error amplifier, IEAO.

The I_{SENSE} filter is an RC filter. The resistor value of the I_{SENSE} filter is between 100ohm and 50ohm because I_{OFFSET} X Rs can generate an offset voltage of IEAO.
Selecting an R_{FILTER} which is equal to 50ohm, will keep the offset of the IEAO less than 5mV. Usually, we

design the pole of I_{SENSE} filter at Fpfc/6, one sixth of the PFC switching frequency. Therefore, the boost inductor can be reduced 6 times without disturbing the stability. Thus the capacitor of the I_{SENSE} Filter, C_{FILTER}, will be around 283nF.
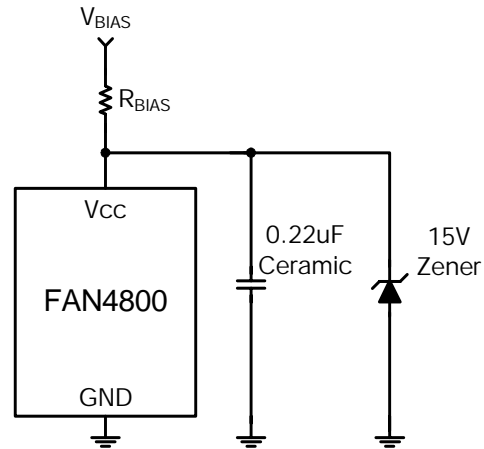

Figure 3. External Component Connection to Vcc

Osillator(RAMP1)
The oscillator frequency is determined by the values of R_T and C_T, which determine the ramp and off-time of the oscillator output clock:

$$f_{OSC} = \frac{1}{t_{RAMP} + t_{DEADTIME}}$$

The dead time of the oscillator is derived from the following equation:

$$t_{RAMP} = C_T \times R_T \times \ln\left(\frac{V_{REF} - 1.00}{V_{REF} - 3.75}\right)$$

at $V_{REF} = 7.5V$ and $t_{RAMP} = C_T * R_T * 0.55$

The dead time of the oscillator may be determined using:

$$t_{DEADTIME} = \frac{2.75V}{12.11mA} \times C_T = 227 \times C_T$$

The dead time is so small ($t_{RAMP} >> t_{DEAD\ TIME}$) that the operating frequency can typically be approximated by:

$$f_{OSC} = \frac{1}{t_{RAMP}}$$

EXAMPLE:

For the application circuit shown in the data sheet, with the oscillator running at:

$$f_{OSC} = 100\text{kHz} = \frac{1}{t_{RAMP}}$$

solving for $C_T * R_T$ yields $1.96 * 10^{-4}$. C_T is 390pF, and R_T is 51.1kohm, selecting standard components values.

The dead time of the oscillator adds to the maximum PWM duty cycle (it is an input to the Duty Cycle Limiter). With zero oscillator dead time, the maximum PWM duty cycle is typically 47%. Take care not to make C_T too large which could extend the maximum duty cycle beyond 50%. This can be accomplished by using a stable 390pF capacitor for C_T.

PWM Section
Pulse Width Modulator

The operation of the PWM section of the FAN4800 is straightforward, but there are several points that should be noted. Foremost among these is the inherent synchronization of PWM with the PFC section of the device, from which it also derives its basic timing. The PWM is capable of current mode or voltage mode operation. In current mode applications, the PWM ramp (RAMP2) is usually derived directly from a current sensing resistor or current transformer in the primary of the output stage, and is thereby representative of the current flowing in the converter's output stage. DC I_{LIMIT}, which provides cycle-by-cycle current limiting, is typically connected to RAMP2 in such applications. For voltage mode operation, and certain specialized applications, RAMP2 can be connected to a separate RC timing network to generate a voltage ramp against which V_{DC} will be compared. Under these conditions, the use of voltage feed-forward from the PFC buss can assist in line regulation accuracy and response. As in current mode operation, the DC I_{LIMIT} input is used for output stage over current protection.

No voltage error amplifier is included in the PWM stage of the FAN4800, as this function is generally performed on the output side of the PWM's isolation boundary. To facilitate the design of opto-coupler feedback circuitry, an offset has been built into the PWM's RAMP2 input that allows V_{DC} to command a zero percent duty cycle for input voltages below typical 0.95V.

PWM Current Limit

The DC I_{LIMIT} pin is a direct input to the cycle-by-cycle current limiter for the PWM section. Should the input voltage at this pin ever exceed 1V, the output flip-flop is reset by the clock pulse at the start of the next PWM power cycle. Besides, when the DC ILIMIT triggers the cycle-by-cycle current, it also softly discharges the voltage of soft-start capacitor. It will limit PWM duty cycle mode. Therefore, the power dissipation will be reduced during the dead short condition.

V_{IN} OK Comparator

The V_{IN} OK Comparator monitors the DC output of the PFC and inhibits the PWM if this voltage on V_{FB} is less than its nominal 2.25V. Once this voltage reaches 2.25V, which corresponds to the PFC output capacitor being charged to its rated boost voltage, the soft start begins.

PWM Control (RAMP2)

When the PWM section is used in current mode, RAMP2 is generally used as the sampling point for a voltage representing the current in the primary of the PWM's output transformer. The voltage is derived either from a current sensing resistor or a current transformer. In voltage mode, RAMP2 is the input for a ramp voltage generated by a second set of timing components (R_{RAMP2}, C_{RAMP2}), that will have a minimum value of zero volts and a peak value of approximately 5V. In voltage mode operation, feed-forward from the PFC output buss is an excellent way to derive the timing ramp for the PWM stage.

Soft Start

PWM start-up is controlled by selection of the external capacitor at SS. A current source of 20mA supplies the charging current for the capacitor, and start-up of the PWM begins at 0.95V. Start-up delay can be programmed by the following equation:

$$C_{SS} = t_{DELAY} \times \frac{20\mu A}{0.95V}$$

where Css is the required soft start capacitance, and the t_{DELAY} is the desired start-up delay.

It is important that the time constant of the PWM soft start allows the PFC time to generate sufficient output power for the PWM section. The PWM start-up delay should be at least 5ms.

Solving for the minimum value of Css:

$$C_{SS} = 5ms \times \frac{20\mu A}{0.95V} = 100nF$$

Use caution when using this minimum soft start capacitance value because it can cause premature charging of the SS capacitor and activation of the PWM section if V_{FB} is in the hysteresis band of the V_{IN} OK comparator at start-up. The magnitude of V_{FB} at start-up is related both to line voltage and nominal PFC output voltage. Typically, a 1.0mF soft-start capacitor will allow time for V_{FB} and PFC_{OUT} to reach their nominal values prior to activation of the PWM section at line voltages between 90Vrms and 265Vrms.

Generating Vcc

After turning on the FAN4800 at 13V, the operating voltage can vary from 10V to 17.9V. The threshold voltage of the Vcc OVP comparator is 17.9V. and its hysteresis is 1.5V. When Vcc reaches 17.9V, PFC OUT will be low, and the PWM section will not be disturbed. There are two ways to generate Vcc. One way is to use auxiliary power supply around 15V, and the other way is to use bootstrap winding to self-bias the FAN4800 system. The bootstrap winding can be either taped from the PFC boost choke or from the transformer of the DC-to-DC stage.

The ratio of the bootstrap's winding transformer for the bootstrap should be set between 18V and 15V. A filter network is recommended between Vcc(pin 13)and bootstrap winding. The resistor of the filter can be set as following.

$$R_{FILTER} \times I_{vcc} \sim 2V, I_{vcc} = I_{op} + (Q_{PFCFET} + Q_{PWMFET})$$
$$\times f_{sw} \quad I_{op} = 2.5mA(typ.)$$

If anything goes wrong, and Vcc goes beyond 17.9V, the PFC gate(pin 12) drive goes low and the PWM gate drive (pin 11) remains working. The resistor's value must be chosen to meet the operating current requirement of the FAN4800 itself (5mA, max.) in addition to the current required by the two gate driver outputs.

EXAMPLE:
To obtain a desired VBIAS voltage of 18V, a VCC of 15V, and the FAN4800 driving a total gate charge of 90nC at 100kHz (e.g. 1 IRF840 MOSFET and 2 IRF820 MOSFET), the gate driver current required is:

$$I_{GATEDRIVE} = 100kHz \times 90nC = 9mA$$
$$R_{BIAS} = \frac{V_{BIAS} - V_{CC}}{I_{CC} + I_G}$$
$$R_{BIAS} = \frac{18V - 15V}{5mA + 9mA}$$
$$Choose R_{BIAS} = 214\Omega$$

Bypass the FAN4800 locally with a 1.0 mF ceramic capacitor. In most applications, an electrolytic capacitor of between 47mF and 220mF is also required across the part , both for filtering and as a part of the start-up bootstrap circuitry.

Leading/Trailing Modulation

Conventional PWM techniques employ trailing edge modulation in which the switch turns on right after the trailing edge of the system clock. The error amplifier output is then compared with the modulating ramp up. The effective duty cycle of the trailing edge modulation is determined during the on-time of the switch. Figure 4 shows a typical trailing edge control scheme.

In the case of leading edge modulation, the switch is turned off exactly at the leading edge of the system clock. When the modulating ramp reaches the level of the error amplifier output voltage, the switch is turned on. The effective duty-cycle of the leading edge modu-

lation is determined during off-time of the switch. Figure 5 shows a leading edge control scheme.

One of the advantages of this control technique is that it requires only one system clock. Switch 1(SW 1) turns off and switch 2(SW2) turns on at the same instant to minimize the momentary no-load period, thus lowering ripple voltage generated by the switching action. With such synchronized switching, the ripple voltage of the first stage is reduced. Calculation and evaluation have shown that the 120Hz component of the PFC's output ripple voltage can be reduced by as much as 30% using the leading edge modulation method.
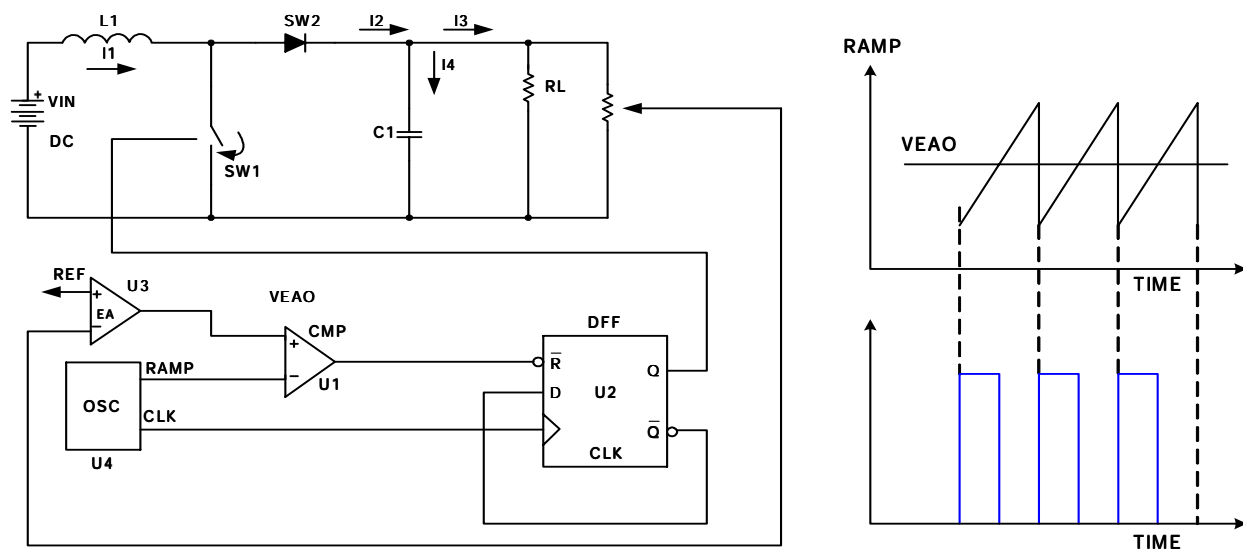

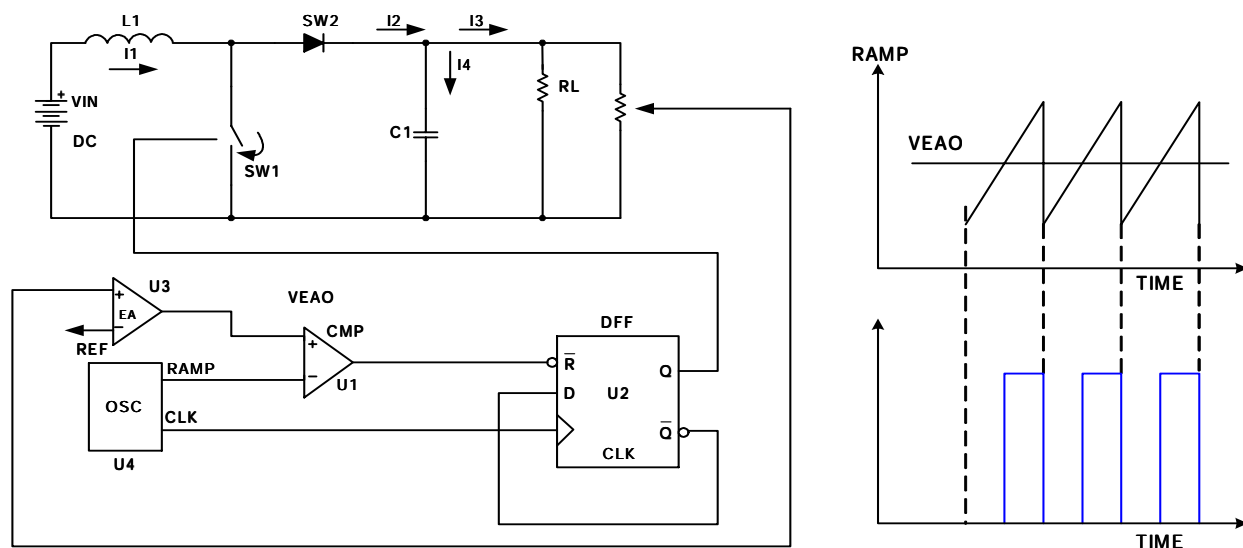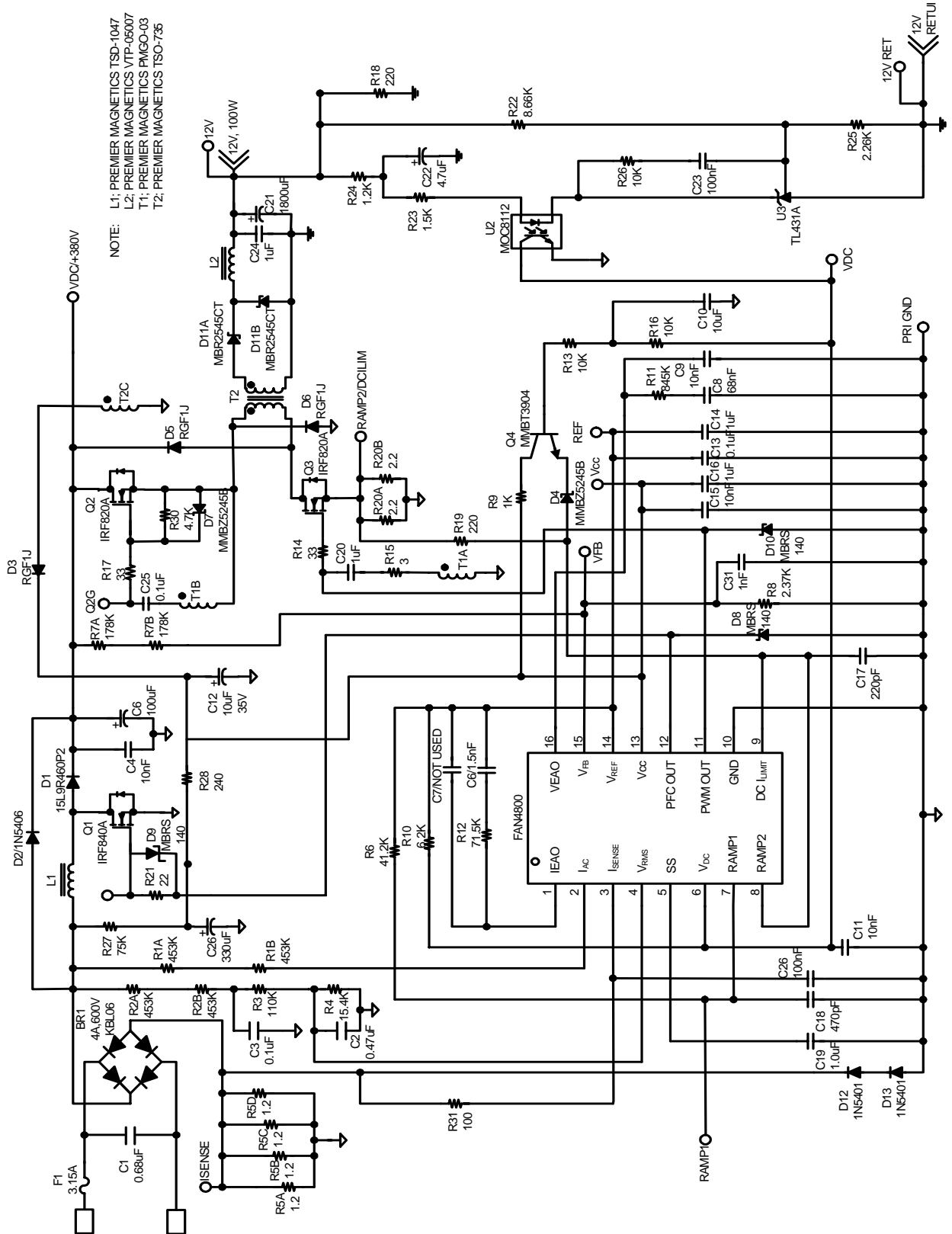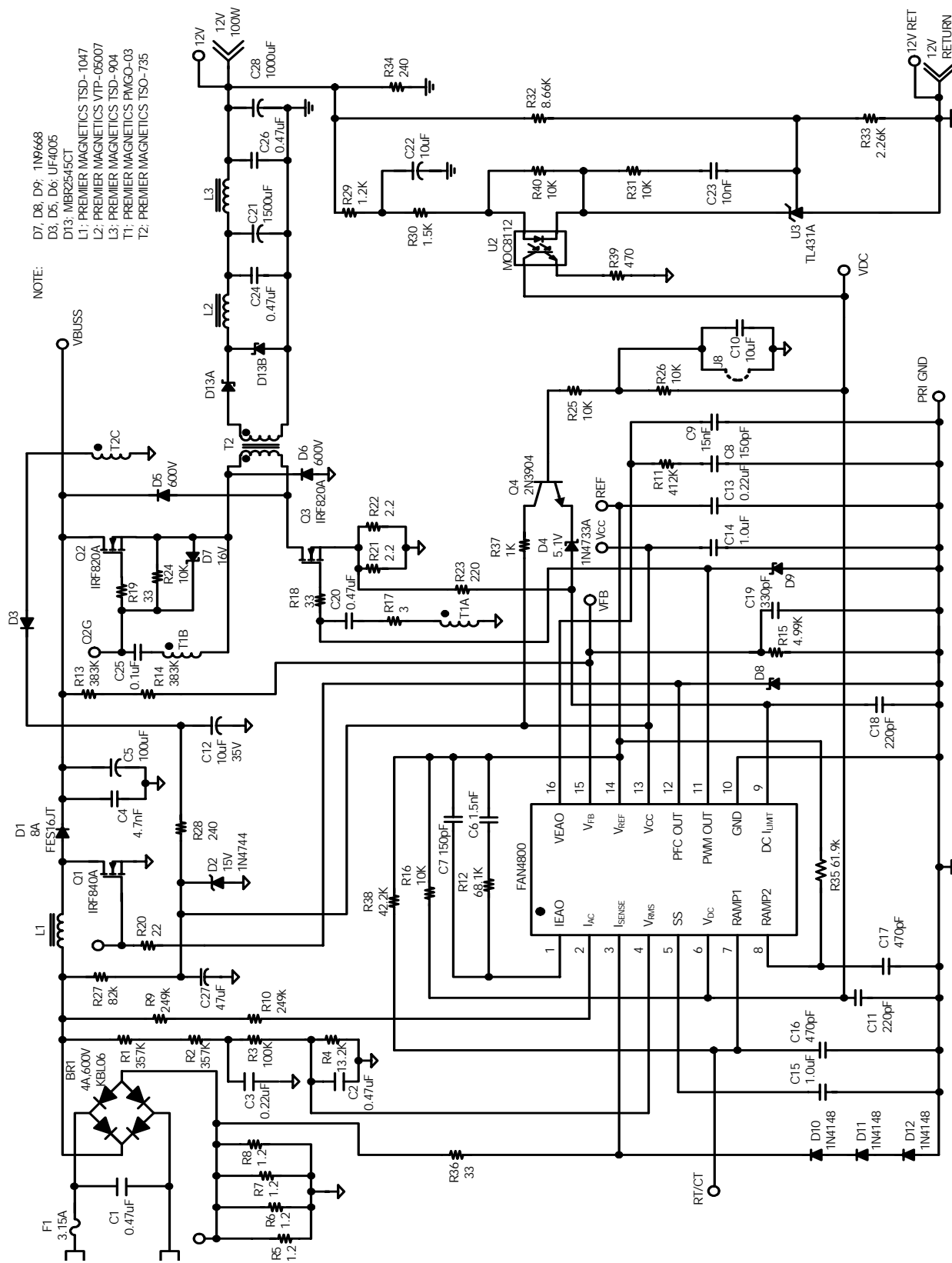Figure 4. Typical Trailing Edge Control Scheme

Figure 5. Typical Leading Edge Control Scheme
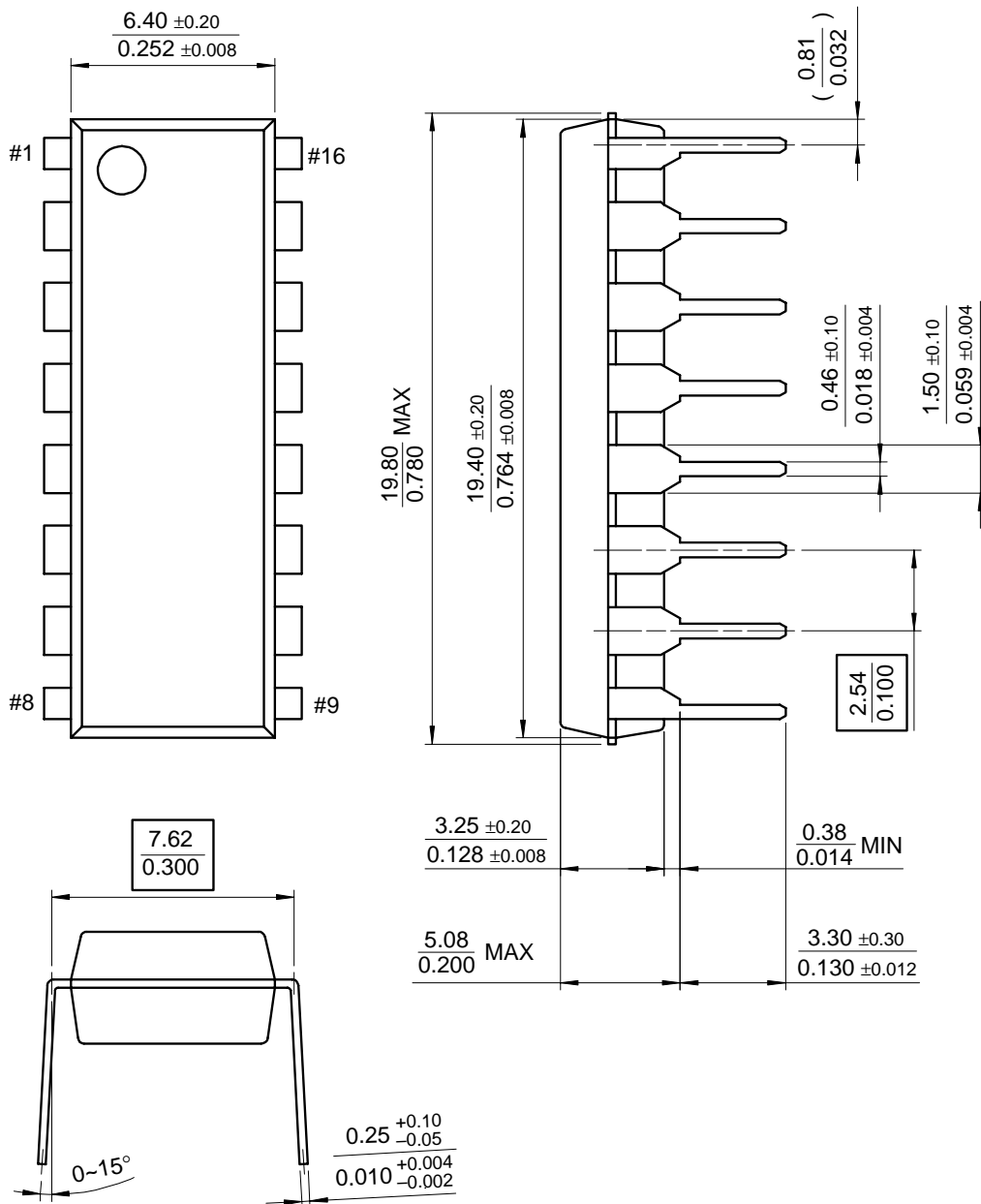
Application Circuit (Current Mode)

NOTE:
L1; PREMIER MAGNETICS TSD-1047
L2; PREMIER MAGNETICS VTP-05007
T1; PREMIER MAGNETICS PMGO-03
T2; PREMIER MAGNETICS TSO-735

12V RETUI

12V RET

R18 220

R22 8.66K

R25 2.26K

12V

12V, 100W

C21 1800uF

C24 1uF

L2

R24 1.2K

C22 4.7uF

R23 1.5K

R26 10K

C23 100nF

U2 MOC8112

U3; TL431A

VDC

D11A MBR2545CT

D11B MBR2545CT

T2

D5 RGF1J

D6 RGF1J

RAMP2/DCILIM

R20B 2.2

Q4 MMBT3904

R13 10K

R16 10K

C10 10uF

PRI GND

C9 10nF

C8 68nF

R11 845K

REF

C14 C13 C16 0.1uF 1uF

Q3 IRF820A

R20A 2.2

R9 1K

Vcc

C15 C16 10nF 10nF

Q2 IRF820A

R30 4.7K

D7 MMBZ5245B

R14 33

C20 1uF

R15 3

R19 220

D4 MMBZ5245B

T1A

VFB

D10 MBRS 140

C31 1nF

R8 2.37K

R17 33

C25 0.1uF

T1B

D3 RGF1J

R7A 178K

Q2G

R7B 178K

D8 MBRS 140

C17 220pF

T2C

VDC/+380V

C12 10uF 35V

C6 100uF

C4 10nF

R28 240

D1 15L9R460P2

Q1 IRF840A

D9 MBRS 140

R21 22

L1

D2/1N5406

R27 75K

R1A 453K

C26 330uF

R1B 453K

C11 10nF

C26 100nF

BR1 4A,600V KBL06

R2A 453K

R2B 453K

R3 110K

R4 15.4K

C3 0.1uF

C2 0.47uF

C18 470pF

C19 1.0uF

D12 1N5401

D13 1N5401

R5D 1.2

R5C 1.2

R5B 1.2

R5A 1.2

R31 100

F1 3.15A

C1 0.68uF

ISENSE

RAMP1

FAN4800

16	15	14	13	12	11	10	9
VEAO	V_FB	V_REF	Vcc	PFC OUT	PWM OUT	GND	DC I_LIMIT
IEAO	I_AC	I_SENSE	V_RMS	SS	V_DC	RAMP1	RAMP2
1	2	3	4	5	6	7	8

C7/NOT USED

C6/1.5nF

R6 41.2K

R10 6.2K

R12 71.5K

Application Circuit (Voltage Mode)

Mechanical Dimensions
Package

16-DIP

6.40 ±0.20 / 0.252 ±0.008

#1   #16

#8   #9

19.80 / 0.780 MAX

19.40 ±0.20 / 0.764 ±0.008

(0.81 / 0.032)

0.46 ±0.10 / 0.018 ±0.004

1.50 ±0.10 / 0.059 ±0.004

2.54 / 0.100

3.25 ±0.20 / 0.128 ±0.008

0.38 / 0.014 MIN

5.08 / 0.200 MAX

3.30 ±0.30 / 0.130 ±0.012

7.62 / 0.300

0~15°

0.25 +0.10 −0.05 / 0.010 +0.004 −0.002

Ordering Information

Product Number	Package	Operating Temperature
FAN4800IN	16-Pin PDIP	-40°C ~ +125°C